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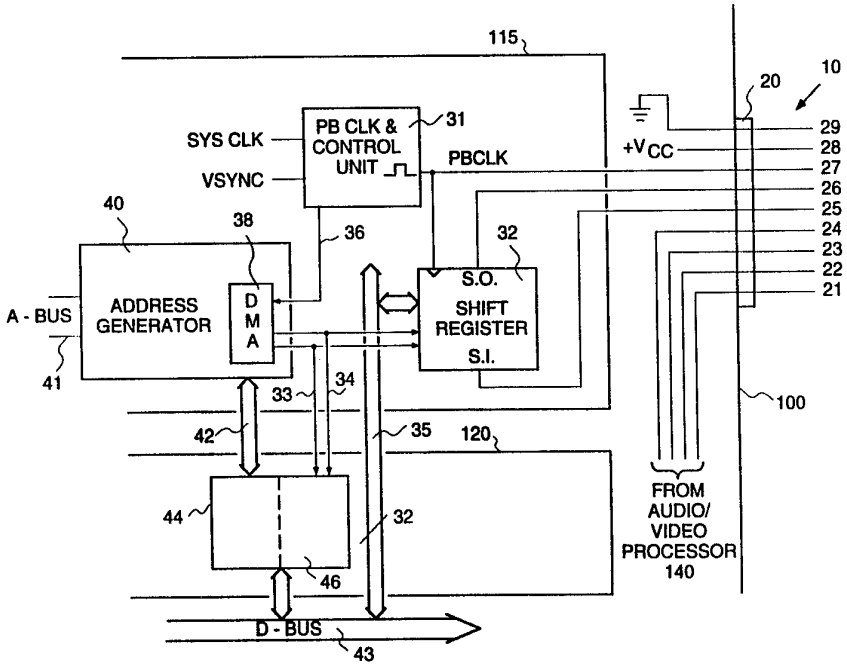
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(57) Abstract

A player bus (10) providing bidirectional transmission of digital data. Interface devices are connected along the bus in a daisy chained manner and data transmission is performed serially. The transmission of audio signals corresponding to a displayed video image is also provided as is a clock signal (27) providing vertical and horizontal synchronization (31) to devices on the bus. An IR link (16) may be provided within the bus for wireless transmission.

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PLAYER BUS APPARATUS AND METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is related to:

PCT Patent Application Serial No. _____, entitled AUDIO/VIDEO COMPUTER ARCHITECTURE, by inventors Mical et al., filed concurrently herewith, Attorney Docket No. MDI04222, and also to U.S. Patent Application Serial No. _____, bearing the same title, same inventors and also filed concurrently herewith;

PCT Patent Application Serial No. _____, entitled RESOLUTION ENHANCEMENT FOR VIDEO DISPLAY USING MULTI-LINE INTERPOLATION, by inventors Mical et al., filed concurrently herewith, Attorney Docket No. MDI03050, and also to U.S. Patent Application Serial No. _____, bearing the same title, same inventors and also filed concurrently herewith;

PCT Patent Application Serial No. _____, entitled METHOD FOR GENERATING THREE DIMENSIONAL SOUND, by inventor David C. Platt, filed concurrently herewith, Attorney Docket No. MDI04220, and also to U.S. Patent Application Serial No. _____, bearing the same title, same inventor and also filed concurrently herewith;

PCT Patent Application Serial No. _____, entitled METHOD FOR CONTROLLING A SPRYTE RENDERING PROCESSOR, by inventors Mical et al., filed concurrently herewith, Attorney Docket No. MDI03040, and also to U.S. Patent Application Serial No. _____,

bearing the same title, same inventors and also filed concurrently herewith;

PCT Patent Application Serial No. _____, entitled SPRYTE RENDERING SYSTEM WITH IMPROVED CORNER CALCULATING ENGINE AND IMPROVED POLYGON-PAINT ENGINE, by inventors Needle et al., filed concurrently herewith, Attorney Docket No. MDI04232, and also to U.S. Patent Application Serial No. _____, bearing the same title, same inventors and also filed concurrently herewith;

PCT Patent Application Serial No. _____, entitled METHOD AND APPARATUS FOR UPDATING A CLUT DURING HORIZONTAL BLANKING, by inventors Mical et al., filed concurrently herewith, Attorney Docket No. MDI04250, and also to U.S. Patent Application Serial No. _____, bearing the same title, same inventors and also filed concurrently herewith;

PCT Patent Application Serial No. _____, entitled IMPROVED METHOD AND APPARATUS FOR PROCESSING IMAGE DATA, by inventors Mical et al., filed concurrently herewith, Attorney Docket No. MDI04230, and also to U.S. Patent Application Serial No. _____ , bearing the same title, same inventors and also filed concurrently herewith; and

PCT Patent Application Serial No. _____, entitled PLAYER BUS APPARATUS AND METHOD, by inventors Needle et al., filed concurrently herewith, Attorney Docket No. MDI04270, and also to U.S. Patent Application Serial No. _____, bearing the same title, same inventors and also filed concurrently herewith.

The related patent applications are all commonly assigned with the present application and are all incorporated herein by reference in their entirety.

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates to multi-media computers. More specifically, the present invention relates to interfaces between a multi-media computer and an interactive interface device.

Description of the Related Art

The advent of computer technology has brought the use of computers into the home for several purposes including their use as educational tools and for their entertainment value. With constant advancements in computer technologies the capability of computer has increased and progress is being made in the development of multi-media computers. The term "multi-media" when applied to computers refers to those computers which process data in at least two media, for example, both video and audio. Technologies relating to multi-media computer systems are relatively new and apparatus which permit a user to interface with the computer in a manner that takes advantage of the increased performance brought by multi-media machines are currently being developed and their presence in the prior art is rare.

Although the present invention is within the realm of multi-media computers, it is particularly applicable to interactive home entertainment and education systems. Accordingly, and in view of the dearth of multi-media interface art, an analysis of interface apparatus for home entertainment systems and related devices is now presented. This analysis will first examine the physical structure of prior interface arrangements and then examine various interface devices.

Several video game entertainment systems and their arrangement of interface or "player" devices are known in the art. They usually consist of an external bus to which are connected one or more joysticks or keypads or similar devices. These devices permit a user to interface with a video image projected on a display, such as a television or computer monitor. A singular serial connection of a device to a system is known in the art as is a limited serial bus which connects both a mouse and keyboard.

In two well known embodiments that are generally representative of the state of the prior art, a maximum of two interface devices can be connected to the system, one through each of two ports. In one of these two embodiments, an adaptor device may be connected to the two ports to permit a total of four devices to interface to the system.

One drawback to this arrangement is the limitation that only 4 players can participate at any one time. A further disadvantage is that 5 (or 6) separate lines are required to permit those 4 players to play, one from the processor to console, possibly one from the two ports to the adaptor and one from the adaptor to each of 4 players. The result is a "rat's nest" of wire which leads to confusion among players as to who's playing device is who's and creates a safety hazard to those attempting to walking through the playing area, normally a living room or family room. Ready removal and replacement of this plurality of wires in a storage area, be it the closet or under the couch, may also be problematic.

A further nuisance associated with video games is a sort of noise pollution in which a household is filled with noises associated with the video images.

The sounds include, among others, crashes, screaming, explosions and crude music, each of which may become annoyingly repetitive. A need exists in the art to overcome these problems.

There are several types of interface devices and their makeup is dependent on both the function to be performed by the interface and the type of media implicated, primarily video and audio for purposes of the present invention. In addition to joysticks and specifically configured keypads, video devices include rudimentary stereoscopic glasses which permit 3-D viewing of a video image, a pointing device or gun and a method of orienting same, a mouse, a steering wheel, etc. With respect to audio, the speaker of a television or those of a receiver connected in the television's audio path are usually used. There are also several other types of interface devices and a random selection of these other types may be seen at a local video arcade. Though such devices may be known in the art, they have not been implemented in the home entertainment context.

One reason that these other devices have not been implemented in home video entertainment context is that current home entertainment systems lack sufficient processor power to achieve the desired special effects. A related reason is that the limited processing capabilities limit the volume and diversity of interface devices which can be connected over an external bus. Since, however, processing power is continually increasing, a need exists for an interface bus which permits the connection of a significantly large number of interface devices and a plurality of different types of interface devices.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an external bus for a multi-media computer that permits the connection of a plurality of different types of interface devices.

It is another object of the present invention to provide an external bus that permits connection to a significantly large number of devices.

It is still another object of the present invention to provide such an external bus with a wireless connection to the multi-media computer and to arrange the bus in an orderly fashion.

And it is yet another object of the present invention to provide an external bus that is capable of delivering audio signals to interface devices that support a sound function.

These and related objects of the present invention may be achieved through use of the player bus apparatus and method disclosed herein. A player bus in accordance with the present invention includes several signal lines which provide an audio signal, data, power, a ground signal and a clock signal. The audio signal lines may be in mono or stereo and in the case of the latter, a right side and a left side signal are propagated on the bus with respective grounds. The data signal lines include a serial data out line to the devices and a serial data in line for receiving data from the devices. The clock signal is used for synchronous transmission of data signals. A digital data ground signal is also provided.

The audio signals are provided by internal connection to an audio processor. Digital data is transferred by a DMA channel in between the serial data bus and a dedicated location in the system memory of

the video system to which the external bus is connected. A video processor writes to and reads from the dedicated memory location to process data to and from the bus.

Devices on the bus are daisy-chained together which means that they are connected in a serial, continuous fashion in which a first device is connected to the video entertainment system, a second device is connected to the first device, a third device is connected to the second device and so on.

An IR link is also provided which permits wireless communication within the bus.

Through use of such an external bus, a plurality of different types of interface devices can be connected to a video entertainment system and in numbers greatly exceeding those of the prior art levels. The daisy-chain arrangement permits easy connection and removal of devices as well as simple storage and avoidance of the rat's nest problems discussed above. Implementation of an external bus providing the above will be better understood after review of the following best mode of carrying out the invention with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood by reference to the figures of the drawings wherein like numbers denote like parts throughout.

Fig. 1 is a block diagram of a consumer home multi-media system.

Fig. 2 is a schematic/block diagram of a preferred embodiment of the external bus of the present invention integrated into the consumer home multi-media system of Fig. 1.

Fig. 3 is a diagram of a hypothetical arrangement of interface devices on the external bus.

Fig. 4 is a schematic/block diagram of an arbitrary interface device illustrating connection to the external bus.

Fig. 5 is a schematic diagram for a stereoscopic glasses interface device.

Fig. 6 illustrates a timing relationship relevant to the device of Figure 5.

DETAILED DESCRIPTION

An external bus in accordance with the present invention is used, among other purposes, to transmit data signals between a consumer interactive multi-media computer and a plurality of interface or "player" devices connected to the external bus. For that reason, an overview of such a multi-media computer is presented first to facilitate a better understanding of the environment in which the present invention may be practiced. A detailed description of the external bus and how it is integrated into such a multi-media computer is provided thereafter.

Referring to Fig. 1, a block diagram of a multi-media computer, hereinafter referred to as "video image processing and display system" 100 to which is attached the player bus 10 of a preferred embodiment is shown. A key feature of such a system 100 is that it is relatively low in cost and yet it provides mechanisms for handling complex image scenes in real time and displaying them at relatively high resolution.

Except where otherwise stated, all or most parts of system 100 are implemented on a single printed circuit board and the circuit components reside within one or a plurality of integrated circuit (IC) chips mounted to

the board. Furthermore, except where otherwise stated, all or most of the circuitry is implemented in CMOS (complementary metal-oxide-semiconductor) technology. An off-board power supply (not shown) is used to deliver electrical power.

The system 100 includes a real-time image data processing unit (IPU) 110, a video address manipulator 115 having internal address and data buses, a system memory unit 120 having multiple independently-addressable storage banks, an audio/video processor 140, a audio/video output circuit 152 and a display unit 160 which may be a home television. The player bus 10 provides connection to a plurality of interface devices, such as a plurality of game units 11-13 or a joystick 15, etc., which are described in more detail below, permitting users to interact with the system 100. An expansion bus 190 is also provided for the connection of CD ROM drives and other hardware.

The image data processing unit (IPU) 110 is driven by a system processor clock generator 102 (approximately 50-60MHz) operating in synchronism with, but at a higher frequency than an address manipulator clock generator 108 (typically 12.2727 MHz for NTSC) which is used to clock address signals from the address manipulator 115 to system memory 120. IPU 110 includes a RISC type 25MHz ARM60 microprocessor (not shown) available from Advanced RISC Machines Limited of Cambridge, U.K. A plurality of sprite-rendering engines (not shown) and direct memory access (DMA) hardware (not shown) are also provided within the IPU 110.

The IPU 110 accesses binary-coded data (e.g., 125) stored within the system memory 120 and modifies the stored data at a sufficiently high-rate of speed to

create the illusion for observer 170 that real-time animation is occurring in the high-resolution image 165 displayed on video display unit 160. In many instances, a user will be interactively affecting the animated image 165 by operating game units 11-13 or the joystick 15 or other input means, described below, back signals 178 over the player bus 10 representing the user's real-time responses to the image data processing unit (IPU) 110.

IPU 110 is operatively coupled to the system memory 120 such that the IPU 110 has read/write access to various control and image data structures stored within system memory 120 either on a cycle-steal basis or on an independent access basis. For purposes of the disclosed invention, the internal structure of IPU 110 is immaterial. Any means for loading and modifying the contents of system memory 120 at sufficient speed to produce an animated low-resolution image data structure 125 of the type described below will do.

The system memory 120 in one embodiment has the capacity to store 2 megabytes of data but it can be expanded to store 16 megabytes of data. (A byte is understood to consist of eight bits of data.) Two megabytes is a preferred, but not an absolute minimum quantity. The system will work with a system memory of larger or smaller capacity. System memory access time should be small enough to meet the demands of the address manipulator clock generator 108 and system processor clock 102.

Physically, the system memory 120 is split into left and right independently addressable banks 120L,120R where each bank has its own address port and 16-bit wide data port. This gives hardware devices, such as the CLUT 200 and CCU 250, simultaneous access

to two separately addressable 16-bit "halfwords" within system memory 120. In most instances, such as when the image data processing unit (IPU) 110 is accessing data within system memory 120, the same address is applied to both banks of the system memory 120, and accordingly, the system memory 120 functions as a unitary 32-bit wide word-storing system. When the resolution-enhancing subsystem 150 is fetching data out of system memory 120, however, the left-bank address word AB_0 can be different from the right-bank address word AB_1. They can also be the same when desired.

System memory 120 is programmed to contain image-defining data in a variety of system memory address regions, including the low-resolution, current frame-buffer region (cFB) 125. The system memory 120 also contains image-rendering control data in other regions (not shown), instruction code for execution by the IPU 110 in yet other regions (not shown) and color palette for a CLUT download (not shown). In addition to current frame-buffer region (cFB) 125, the system memory 120 will often contain one or more alternate frame-buffer regions, such as the previous frame buffer (pFB) 126, storing low-resolution image data of similar structure to that stored in the current frame-buffer region (cFB) 125. The size of each frame buffer is 2 bytes (16 bits) x 320 bytes per line x 240 lines = 153600 bytes.

If desired, system memory 120 can also store high-resolution image data (not shown) and the stored high-resolution image data can be transmitted as is to audio/video processor 140.

To enhance access time, system memory 120 is divided into "pages" and each page is 512 x 32 (one word) bits in size. Since system memory 120 in the

present embodiment has 1 megabyte of memory, there are 512 pages. The pages are allocated such that they conceptually form a stack of 512 pages, at least a portion of which is equally split between the left bank and the right bank. A row address is decoded to select one of the 512 pages and a column address is decoded to select one of the 512 words. The selected 32 bit word is then placed on the appropriate system bus. The procedure in which data is transferred from system memory 120 to a system wide bus is described in more detail in PCT Patent Application Serial No. _____ , entitled AUDIO/VIDEO COMPUTER ARCHITECTURE, by inventors Mical et al., filed concurrently herewith, Attorney Docket No. MDIO4222, and also to U.S. Patent Application Serial No. _____, bearing the same title, same inventors and also filed concurrently herewith.

The system 100 has two system wide buses: an S-bus and a D-bus which pass control signals and data between components in system 100. The D-bus is utilized primarily for the transmission of data (including instructions) between the IPU and system memory and is connected to the internal data bus in the address manipulator 115. Data transmission may be either under the control of a CPU in the IPU or by a DMA channel in the address manipulator 115. The S-bus is used for the transmission of several types of data and control signals, primarily from the system memory 120 to the audio/video processor 140.

During each read of video image data from system memory 120, two pixel defining halfword signals, Rx(LRo) and Px(LR1), may be place on to the S-bus via respective system memory output buses in response to serial clock signals LSC, RSC from the address

manipulator. These pixel-defining half-words are transmitted over the S-bus to audio/video processor 140.

In the audio/video processor 140 the video data may either be expanded in the CLUT 200 or bypass the CLUT 200. Interpolation to enhance resolution may or may not be performed on the output from the CLUT 200, depending on control signals to the interpolator 150. Upon output from the audio/video processor 140, the video data is transmitted to the audio/video output circuit 152 from where it is sent to the display 160.

The audio/video processor 140 also processes audio data in conjunction with the processed video data.

In the above described manner, the system 100 processes video data for display or the monitor 165 and corresponding audio signals. It is also possible, and in fact likely, that the processor 110 will receive input data from the plurality of devices or the player bus 10 and modify the display 165 in response to this data. The processor 110 also sends data to the devices on the player bus 10 for initialization and to perform a design function. How this transfer of data is implemented is now presented along with a detailed description of the player bus. The overall physical structure of the player bus is described first, followed by specifics on operation such as initialization and data transmission.

Referring to Fig. 2, a block diagram of the player bus 10 and elements of the system 100 which have a functional relation to the player bus 10 are shown. The player bus 10 consists of nine signal lines 21-29 which form an interactive connection between the system 100 and a plurality of interface devices, a few of which are shown for exemplary purposes in Fig. 3. The

player bus 10 is comprised of nine signal lines 21-29. Signal lines 21-24 are four signal lines which emanate from the audio/video processor 140 for transmitting left side audio, left side audio ground, right side audio and right side audio ground. Signal line 25 is a serial data in line for transmitting data from any of the plurality of interface devices to the system 100. Signal line 26 is a serial data out line for transmitting digital data from the system 100 to any of the plurality of interface devices. Signal line 27 is the player bus clock line on which the player bus clock signal propagates. The player bus clock (PBClk) is used to clock digital data to and from the plurality of interface devices. Signal line 28 is a power supply line and signal line 29 is digital ground.

The audio signal lines 21-24 transmit audio signals in much the same way as they are propagated to audio speakers provided with a monitor, such as in a television, however, the current and perhaps the voltage levels may be reduced from that delivered to a standard television unit due to the reduced physical dimensions of the signal lines 21-24. Arranging the audio lines as part of an interactive bus provides several advantages. One is that it permits the use of personal audio speaker units, such as head phones and thereby permits a plurality of players to interactively participate in a video presentation with accompanying analog signals, while not filling the surrounding environment with the sounds accompanying the video presentation. In this manner, it is possible for a group of players to play, for example, a video game, each wearing head phones, so that other people in the room or the house are not disturbed by the sounds of the video game. The presence of audio signals in

personal listening devices also permits more realistic simulation in video representations of situations where one would normally wear a personal listening device, for example, in the cockpit of a jet fighter aircraft.

Fig. 2 also illustrates the functional aspects of digital data transmission. Serial data input line 25 is connected to a serial-to-parallel, parallel-to-serial shift register 32. This shift register 32 is unique in that it provides simultaneous loading and unloading. It is used in the present invention instead of two individual shift-in and shift-out registers because, amongst other reasons, it reduces the amount of die area taken up for the shift-in/shift-out function. Input data from any of the interface devices is input serially from line 25 to a serial input of the register 32. Data is output to the devices over line 26 which is connected to a serial output of shift register 32. In response to a player bus clock signal, data is transferred sequentially, one bit at a time, from signal line 25 to the serial input of register 32 and from the serial output of register 32 to signal line 26. When 32 bits have been transferred, a simultaneous parallel shift, under the control of DMA channel 38 takes place in which 32 bits are unloaded from register 32 over the internal data bus 35 and D-bus to the system memory 120 and data is loaded from system memory to the register 32 over the same path. This transfer is achieved generally as follows.

The shift register 32 is connected to the address manipulator internal bus 35 that is connected to the D-bus 43 which is, in turn, connected to system memory 120, as shown conceptually. Data unloaded from the register 32 is written to a data out location 44 in system memory 120 and data to be loaded into the

register 32 is read from data location 46. Memory location 44 and 46 are shown as being contiguously arranged, but this in not necessary. The data-out and data-in locations 44 and 46 are defined by the IPU 110 and implemented by the DMA channel 38.

The DMA channel 38 contains a DMA channel arbitrator (not shown) and interfaces with the address generator 40 of the address manipulator 115 which is, in turn, connected to an address bus 41. To effectuate a parallel shift, the DMA channel 38 receives a DMA request from the PB clock and control unit 31 when such a transfer is required. The DMA channel 38 also contains 3 registers (not shown). One register contains the base address of the data-out location 44, another holds the base address of the data-in location 46 and a third holds the number of 32 bit words to transfer. The base addresses of the data-out and data-in locations 44 and 46 are mapped to the IPU and may be modified by the IPU. The IPU 110 reads from and writes to the memory locations once per field.

When a 32 bit parallel shift is required, the PB clock and control unit transmits a DMA request to the DMA arbitrator over line 36. Once control of the relevant buses is obtained, an enable is sent over line 33 to write a 32 bit word from the register 32 to data-in location 46. A read enable is then sent over line 34 to load shift register 32 with the next 32 bit word from data-out location 44.

The PB control unit 31 receives vertical and horizontal synchronization signals and a clock signal from the processor clock 102. A counter/decoder (not shown) is used to process the input clock signal to produce a square wave synchronous with the horizontal synchronization signal (H sync) that has two cycles per

horizontal scan line. The resultant signal is the PB clock signal (PBClk) propagated to shift register 32 and over signal line 27 to the plurality of interface devices. There are 240 scan lines in a low resolution, pre-interpolation image. One bit of serial data is transferred from the system 100 to data out line 26 and from data in line 25 to the system 100 each PBClk. Since there are two player bus cycles per scan line and 240 scan lines, a maximum data transfer per field is would appear to be 480 bits. The first 16 scan lines, however, are used to synchronize all of the devices on the bus 10 and are therefore not available for data transmission, reducing the number of bits which can be sent per field to 480 - (2x16) = 448.

Once initialization has been complete, which will be described in more detail below, the bus operates generally as follows. During scan lines 1-8, the player bus clock line 27 is held high. During scan lines 9-16, the player bus clock is held low. This long clock is used to synchronize all interface devices to the vertical blanking period. The transition between lines 8 and 9 is used to load a device's data into its' respective shift register for subsequent input over data-in line 26 to the system, as discussed in more detail below. On scan line 17, the DMA channel 38 is enabled by the PB control unit 31 over line 36. The PB control unit 31 has a counter (not shown) which determines a scan line count by counting a number of clock cycles. Once enabled by the CPU, the DMA channel 38 will first read out the context of the shift register 32. Then it transfers the next 32 bit word of output data into the parallel input port of register 32. Once loaded, the player bus clock system will simultaneously shift out 32 serial bits of data from

shift register 32 and shift in 32 new bits during the next 16 scan lines (lines 17-32). At the completion of the 32 bit serial shift, the control unit 31 will inform the DMA channel 38 over signal line 36 that a new word pair is ready for transfer to and from memory buffer 45, which is, incidentally, a random access memory. When the DMA channel 38 indicates that all words in the data out buffer have been transferred an interrupt is generated from the DMA channel 38 to the CPU and the last 32 bit data word is serially shifted out onto the player bus and 32 new bits of data are shifted in. Note that the shifted in data will not be read until the next field and will at that time be useless because the field to which it applies has already been processed.

The direction of the shift is LSB bit first and MSB bit last, which means that the 32 bits of data shifted out onto the bus are bit 0 to 31, in that order. This is the same order in which the data is received at the interface devices. LSB first with the leading bits possibly falling out the end of the bus. The data from interface devices is similarly shifted LSB first, with possible trailing nulls being ignored.

At bus initialization, the IPU could send 60 bytes of all zeros out and read the unknown data in until at least eight zeros in a row have been read. The incoming data is then examined by the IPU to determine the nature of the devices connected to the player bus. Interface devices on the bus 10, therefore, must except an all zero command as either harmless or as an initialization request. Once the bus has been analyzed to determine what interface devices are attached thereto, software running in system 100 can then

construct the format of input and output data to be used by the bus 10.

Referring again to Fig. 2, the data bus 10 is connected to a standard ten pin D female connector 20 in which 9 of the signal lines are used (the 10th may duplicate digital ground) and operates generally under the following conditions. The Vcc line 28 has a maximum current of 250 mA. The left and right side audio signals have a greater than 100 KΩ load resistance. The data input line 26 has an approximately 470 KΩ load impedance and an approximately 100 pF load capacitance. The data out signal line 25 has a 10 KΩ drive impedance. The clock signal is slew rate controlled and has a low impedance driver. Digital data signals are driven by high impedance drivers 10kΩ and terminated with high capacitance loads (100 pf min, 300 pf max) near the driver (shown in Fig. 4). This will place rise and fall times between approximately 2-6 microseconds. The clock signal transition is high at the start of the scan line, relative to horizontal synchronization for the beginning of a scan line. The clock will transition for exactly the correct number of data bits (plus one) and remain low at the end of the transfer process.

The clock signal is strongly generated in the system 100 and passes through each interface device (as shown in Fig. 4) without buffering. This is done to provide each interface device down the bus 10 a valid timing relationship to horizontal and vertical synchronization. The clock signal is generated from the video timing of the audio/video processor 140.

The audio signals are high impedance (600ohm drivers) and are intended to drive small amplifiers in the player devices that support the audio function.

Referring to Fig. 3, a hypothetical player bus showing a plurality of individual interface devices is shown. The make-up of the bus 10 and those devices shown in Fig. 3 is arbitrary and depends on the desired interface. Devices shown in Fig. 3 are presented merely as an example of different types of devices and it is in no way intended to limit the present invention to those devices shown, which include a key pad 14, a joystick 15, a hand held unit 11 with corresponding ear phones 11a and stereoscopic glasses 11b, an IR pod 16, and a game store card 17. The IR link 16 functions as a wireless data transmitter and receiver and, therefore, permits a separation within the bus, for example, between the television stand and a coffee table so that people can move unhampered about the room. The IR link 16 is shown between stereoscopic glasses 11b and game store 17, but may be located anywhere, usually towards the head of the bus 10. The transmission of data over an IR link is well known. The presence or absence of IR light is used to represent binary logic states. Note that in one implementation audio signals are not transmitted by the IR link and, therefore, devices downstream will not receive audio signals.

The game store unit 17 is essentially a memory unit which a participant may use to store the current state of a game being played, so that the game can be continued from where it was stopped at a later time. The unit 17 may either contain memory and store the current game state therein, or have a mechanism for transferring the game state to a floppy disk or memory

card or other memory device that may be separated from the unit 17. A memory card permits a user, among other options, to store a game state and continue on another machine. An unidentified interface device 18 is also provided to represent other types of interface devices that may be added to the bus 10.

Note also that although these devices are shown external to the system 100 along the bus 10, it is conceivable that some devices, for example, an IR link or a CD player remote control receiver or a front panel switch/display system, could be installed in the player bus 10 path, internal to the system 100, and contained within the system 100 casing. There would be no operational difference between such devices and other player bus devices.

Since the above described arrangement permits 448 bits to be transferred per field and the minimum bit transfer per device is 8 bits, a maximum of approximately 56 devices can be on the bus at one time. This number would be reduced for devices that use more than 8 bits for data transmission. A hypothetical device arrangement for the player bus 10 at maximum capacity is 8 joysticks (8 x 8 bits), 8 guns (8 x 32 bits), 8 glasses (8 x 8 bits) and 8 remotely controlled motorized attack vehicles (8 x 8 bits). Having conceptually illustrated a random group on interface devices, a description of the initialization process is now presented followed by an illustrative description of the physical connection between some of these devices and the bus 10.

Initialization and device identification are important to proper operation of the player bus 10 and function generally as follows. Each of the player devices has an ID code embedded in its response data.

An ID code is mapped by software in the system to the number of input and output bits for the device identified. Since the ID code is embedded, it is received by the system 100 both at initialization and when data is being read in under normal operation. In this manner, it is possible to reconfigure the system (add or delete devices) without re-initializing and without adversely affecting those device already on the line.

During an initialization sequence, a string of zeros is shifted out from the system 100. A requirement for all of the player devices is that they see a string of zeros either as an initialization or don't cares. As this data is being shifted out, a string of data from each of the devices, loaded during the load signal and containing an ID code and perhaps data, is being shifted in. The string of zeros shifted on to the bus functions primarily as harmless data to be shifted out as device data is shifted in, but may also serve to reset some bus devices such as stereoscopic glasses, IR links, robots, etc.

The first 4 bits of data stream received by the system 100 from each device is that device's basic identification code (ID code). The embedding of an ID code in the data stream functions as follows for a joystick 15. The basic joystick 15 will have 8 bits of data that are (inverted): down, up, right, left, switch-2, switch-1, fire-2 and fire-1, although switch-2, switch-1, fire-2 and fire-1 may have other names or represent other functions. Using the inability of the joystick to indicate both up and down at the same time, the ID codes for a basic joystick are 01QQ, 10QQ and 11QQ, where QQ is 01, 10 or 11. All other devices start with 00QQ. All joysticks are incapable of

generating 00 for their first 2 bits, regardless of the pressure applied to any combination of the joystick or switches. Further identification can be had by using 0001 to indicate stereoscopic glasses, 0010 to indicate a gun, steering wheel, mouse or keyboard, and 0011 for other types of expansion devices which will require additional bits for identification. With regard to the escape function, the 1100 sequence indicates escape for the joystick. In all other devices, the escape function is indicated by the bit immediately following the 4 bit identification code. A string of zeros indicates the end of input data into the system 100 device.

Referring to Fig. 4, a schematic view of a joystick interface device 15 is shown. Signal lines 21-29 which constitute the player bus 10 are input from the system 100 to the joystick 15 at header 51. Signals on these lines are processed, as discussed below, and header 52 provides output connection (except for the data-in line 25) to subsequent interface devices. A standard joystick device may include a plurality (four) of switches 53 and a joystick. The relevant electrical aspects of the joystick are represented by reference numeral 54 and include up, down, left and right. The eight signals from switches 53 and the joystick 54 are loaded in parallel to shift register 55, during the transition between lines 8 and 9 of the long clock signal discussed above. An RC time constant is provided to prevent the load signal from being activated during normal data transmission, beginning at line 17.

The PBClk signal, line 27, is input to the preset input of a D latch 56 to produce an inverted output signal PBClk\. The PBClk signal is also input to D

latch 57 which is used to serially latch data-in on data-input line 25, and to D latch 58 which serially latches output data on output line 26. The PBClk\ signal is connected to the clock input of shift register 55 and to D latch 59 which outputs data to subsequent devices. Thus, on a positive edge of PBClk, data is latched in from line 25 at latch 57 and in from line 26 at latch 58. On the falling edge of PBClk, which is the rising edge of PBClk\, data to the system 100 is serially shifted out of register 55 and data to subsequent devices is shifted out from latch 59. Each of the latches 56-59 should have a schmidt trigger clock input.

Referring again to shift register 55, such a register is provided in all devices which input data to the system 100. After initialization the system 100 knows what devices are on the bus, what their order is and how many bits (the number of bits loaded in the shift register) are input by each. After the load signal each of the shift registers is loaded with data from its' respective interface device. The data, from all of the shift register, is then serially shifted as one continuous stream of bits to the system 100.

An optional audio amplifier 60 with volume control and earphones 61 (or other listening device) may also be provided for those devices that support the sound function. The audio signal lines 21-24 and Vcc, line 28, are connected as shown. With respect to the audio function, both left and right (stereo) may be provided. If, however, stereo is not desired, than the audio/video processor 140 can transmit mono signals of a first sound track over one line and of a second sound track over the other line so that two players hear a

different sound track relative to their game situations.

Referring to Fig. 5, a schematic diagram for a stereoscopic glasses device 11b is shown. The D latches 66 and 67 perform the same functions as latches 56 and 57 described with reference to Fig. 4. The shift 65 performs the same function as shift register 55, the loading of device data and the embedded ID code, and D latch 68 receives output data from data out line 25 in the same manner as D latch 58. The stereoscopic glasses 11b also contain additional circuitry that will be described after a discussion of the functions performed by that circuitry.

Referring to Fig. 6, a diagram representing desired and actual stereoscopic signals is presented. In one embodiment of stereoscopic glasses, the left eye and right eye are alternatingly permitted to view an image which is modified in synchronism with the left and right eye strobe to give slightly differing perspectives of the image, thereby creating the 3-D effect. Ideally, the transition between the left eye and right eye strobes 76 and 77 (of Fig. 5) would be a square wave. In reality, however, it is not possible to obtain a square wave due to rise time and fall time limitations. The dashed line in Fig. 6, represents the strobe signal of the prior art. Upon the occurrence of a transition 90 between left eye and right eye, a strobe signal indicating the appropriate state change is transmitted to the stereoscopic glasses. A significant delay, which includes signal propagation delay and the time required for a glasses view cover to change state, is experienced after the transistor 90. A similarly caused delay occurs at transition 91. The result is a lack of synchronization between the

projected image and left/right eye movement in the glasses 11b.

The mechanism of Fig. 6 overcomes this problem by adding a delay of approximately 1-3/4 transitions (7/8th of a cycle) between the occurrence of a square wave transition and the creation of a strobe signal. Referring again to Fig. 5, this delay is achieved by the use of two registers 70 and 75. Register 70 induces a delay of one transition, register 75 is enabled by the output of a counter and induces the remaining delay.

The output of data out latch 68 is input to a serial-in, parallel or serial-out shift register 69. Data is serially shifted through this register and the output of the most significant bit is shifted out over line 25 to the subsequent device. On the occurrence of a load signal, data in register 69 is shifted in parallel to register 70 which is essentially an 8 bit parallel latch. The load also resets a counter mechanism comprised of two counters 73 and 74 configured to count down. These counters 73 and 74 are clocked by PBCLK\ and when a count is reached that provides a best fit rise time curve (less than one transition), the output of the counter 74 enables D-latch register 75 which transmits the appropriate strobe signals over left eye and right eye lines 76 and 77, respectively. In this manner, strobe signals are provided which perform a best fit transition between left and right eye. Although the strobe for each transition begins almost one full period late, the delay is of no consequence due to the alternating nature of the left and right eye transitions.

It is important to note that an alternative to operating in 3-D mode, it is possible to synchronize

both the left and right eye of one pair of stereoscopic glasses to Field 0, synchronize both the left and right eye of another pair of stereoscopic glasses to Field 1 and project an image in Field 0 different from that projected in Field 1. This results in the two players seeing different images, for example, from the cockpits of their respective crafts.

The stereoscopic glasses 11b may also contain an audio amplifier 80 and earphones 81 to support the audio function.

With respect to other devices, they may include a gun or other type of pointing device. A gun is basically a photo cell for detecting high intensity light. As an electron beam scans across and down a monitor screen, the greatest intensity of light at any moment is produced at the pixel the beam is impinging upon at that moment. In prior art devices, it has been difficult to determine the exact position at which the beam is pointing (the position at which the electron beam is impinging upon the monitor). How this problem is overcome is now described.

A gun for use with the player bus 10 is provided with V sync and H sync through the player bus clock. The receipt of H sync by the gun permits the gun to know exactly what line it is on when it detects the point of highest intensity. Furthermore, a counter or similar device is provided in the gun, using techniques known in the art, to provide a count along a horizontal scan line that indicates the exact point along the line where the gun detected the electron beam. In this manner, both a vertical and horizontal indication are generated by the gun, resulting in a high level of accuracy not obtainable in prior art devices.

While the invention has been described in connection with specific embodiments thereof, it will be understood that it is capable of further modification, and this application is intended to cover any variations, uses, or adaptations of the invention following, in general, the principles of the invention and including such departures from the present disclosure as come within known or customary practice in the art to which the invention pertains and as may be applied to the essential features hereinbefore set forth, and as fall within the scope of the invention and the limits of the appended claims.

CLAIMS

What Is Claimed Is:

1. In a consumer interactive multi-media system, having an image processing unit, a system memory and an audio/video processing and output unit for processing video image data to generate a video image and for projecting said video image on a display, an external bus apparatus for the connection of a plurality of interactive interface devices to the system, comprising:

means for propagating digital data bidirectionally between said plurality of interactive interface devices in said system, wherein at least a portion of data propagated from at least one of said interface devices is processed by said processing unit to affect said projected image;

clock signal generating and propagating means for propagating said clock signal to said plurality of interface devices, said clock signal clocking the propagation of said digital data in synchronism with a vertical blanking period of said image projected on said display; and wherein

said bus is formed by sequentially connecting said plurality of devices to one another in a daisy-chained manner extending outwardly from said system, such that said bus forms a substantially singular bus path.

2. The apparatus of claim 1, further comprises:

means for propagating audio signals corresponding to an image projected on said display.

3. The apparatus of claim 1, wherein said means for bidirectionally propagating said digital data comprises:

a serial data out signal line for serially transmitting data from said system to said plurality of interface devices; and

a serial input line for serially transmitting data from any of said plurality of interface devices to said system.

4. The apparatus of claim 3, further comprises:

serial-to-parallel, parallel-to-serial shifting means connected to both of said serial output line and said serial input line for simultaneously unloading data from the input signal line and loading data to the output signal line, the use of said shifting means resulting in a reduction in the physical die area required to perform a shift in and shift out of data.

5. The apparatus of claim 1, wherein said clock signal is also in synchronization with horizontal scan line generation.

6. The apparatus of claim 1, wherein identifying data for at least one of said plurality of interactive interface device is embedded in serial data from that device.

7. The apparatus of claim 1, wherein each of said plurality of interactive interface devices is removably connected in said daisy-chained sequence.

8. The apparatus of claim 1, further comprises:

wireless linking means for providing a wireless link within the external bus.

9. The apparatus of claim 9, wherein said wireless linking means comprises an IR linking means.

10. The apparatus of claim 1, wherein at least one of said plurality of said devices comprises game store means for storing a state of a game playable on said system.

11. The apparatus of claim 10, wherein said game store means comprises means for storing a game state on a removable storage medium.

12. The apparatus of claim 1, wherein as least one of said plurality of devices includes gun means, having photo detector means for detecting an electron beam impinging upon said display, said gun means receiving horizontal synchronization over said external bus to permit a determination of a vertical position of said impinging electron beam and having means for determining a horizontal position of said impinging electron beam along a scan line.

13. The apparatus of claim 1, wherein one of said plurality of devices includes stereoscopic glasses means in which left and right side view covers of said glasses means are opened and closed in synchronism with at least a first and second field of said image;

wherein control signals to open and close said view covers are delayed such that they arrive early for a subsequent occurrence of a desired opening or closing to form a best fit relationship between the

implementation of said control signals and the desired opening and closing of said view covers, thereby overcoming problems associated with rise and fall times.

14. In a consumer interactive multi-media system, having an image processing unit, a system memory and an audio/video processing and output unit for processing video image data to generate a video image and for projecting said video image on a display, an external bus apparatus for the connection of a plurality of interactive interface devices to the system, comprising:

means for propagating digital data bidirectionally between said plurality of interactive interface devices in said system, wherein at least a portion of data propagated from at least one of said interface devices is processed by said processing unit to affect said projected image;

clock signal generating and propagating means for propagating said clock signal to said plurality of interface devices, said clock signal clocking the propagation of said digital data in synchronism with a vertical blanking period of said image projected on said display; and

means for propagating audio signals corresponding to an image projected on said display.

15. The apparatus of claim 14, wherein said bus is formed by sequentially and removably connecting said plurality of interface devices to one another in a daisy-chained manner extending outwardly from said system, such that said bus forms a substantially singular bus path.

16. The apparatus of claim 14, wherein said means for bidirectionally propagating said digital data comprises:

a serial data out signal line for serially transmitting data from said system to said plurality of interface devices;

a serial input line for serially transmitting data from any of said plurality of interface devices to said system; and

serial-to-parallel, parallel-to-serial shifting means connected to both of said serial output line and said serial input line for simultaneously unloading data from the input signal line and loading data to the output signal line, the use of said shifting means resulting in a reduction in the physical die area required to perform a shift in and shift out of data.

17. The apparatus of claim 14, wherein said clock signal is also in synchronization with horizontal scan line generation.

18. The apparatus of claim 14, wherein identifying data for at least one of said plurality of interactive interface devices is embedded in serial data from that device.

19. The apparatus of claim 14, further comprises:

wireless linking means for providing a wireless link within the external bus.

20. The apparatus of claim 14, wherein at least one of said plurality of said devices comprises game

store means for storing a state of a game playable on said system.

21. The apparatus of claim 14, wherein said game store means comprises means for storing a game state on a removable storage device.

22. The apparatus of claim 14, wherein as least one of said plurality of devices includes gun means, having photo detector means for detecting an electron beam impinging upon said display, said gun means receiving horizontal synchronization over said external bus to permit a determination of a vertical position of said impinging electron beam and having means for determining a horizontal position of said impinging electron beam along a scan line.

23. The apparatus of claim 14, wherein one of said plurality of devices includes stereoscopic glasses means in which left and right side view covers of said glasses means are opened and closed in synchronism with at least a first and second field of said image;

wherein control signals to open and close said view covers are delayed such that they arrive early for a subsequent occurrence of a desired opening or closing to form a best fit relationship between the implementation of said control signals and the associated opening and closing of said view covers, thereby overcoming problems associated with rise and fall times.

24. An external bus for use with a video imaging system, comprising:

means for propagating digital data bidirectionally between a plurality of interactive interface devices and said system, wherein at least a portion of data propagated from one of said plurality of interface devices affects an image projected by said system;

clock signal generating and propagating means for propagating said system clock signal to said plurality of interactive interface devices in synchronism with a vertical blanking period of said projected image for clocking the propagation of said digital data along said bus; and

means for propagating audio signals corresponding to an image projected on said display;

wherein said bus is formed by sequentially connecting said plurality of interface devices to one another in a daisy-chained manner extending outwardly from said system.

25. The apparatus of claim 1, wherein said clock signal is also in synchronization with creation of horizontal scan line generation.

26. The apparatus of claim 1, wherein each of said plurality of interactive interface devices is removably connected in said daisy-chained sequence.

27. The apparatus of claim 1, further comprises:

wireless linking means for providing a wireless link within the external bus.

28. The apparatus of claim 1, wherein at least one of said plurality of said devices comprises game store

means for storing a state of a game playable on said system.

29. The apparatus of claim 10, wherein said game store means comprises means for storing a game state on a removable storage device.

30. The apparatus of claim 1, wherein as least one of said plurality of devices includes gun means, having photo detector means for detecting an electron beam impinging upon said display, said gun means receiving horizontal synchronization over said external bus to permit a determination of a vertical position of said impinging electron beam and having means for determining a horizontal position of said impinging electron beam along a scan line.

31. The apparatus of claim 1, wherein one of said plurality of devices includes stereoscopic glasses means in which left and right side view covers of said glasses means are opened and closed in synchronism with at least a first and second field of said image;

wherein control signals to open and close said view covers are delayed such that they arrive early for a subsequent occurrence of a desired opening or closing to form a best fit relationship between the implementation of said control signals and the desired opening and closing of said view covers, thereby overcoming problems associated with rise and fall times.

32. In a consumer interactive multi-media system, having an image processing unit, a system memory and an audio/video processing and output unit for processing

video image data to generate a video image and for projecting said video image on a display, a method for forming and operating an external bus for the connection of a plurality of interactive interface devices to said system, comprising the steps of:

bidirectionally propagating digital data between said plurality of interactive interface devices wherein at least a portion of said data propagated from one of said interface devices affects said projected image;

clocking the propagation of digital data along said bus in synchronism with a vertical synchronization and a horizontal synchronization signal; and

connecting said plurality of interface devices in a daisy chained manner such that said bus has a substantially singular bus path extending outwardly from said system.

33. The method of claim 32, further comprises the step of:

propagating audio signals corresponding to an image projected on said display.

34. The method of claim 33, wherein said step of bidirectionally propagating digital data comprises the step of:

propagating said digital data serially.

35. The method of claim 32, further comprises the step of:

embedding an ID code for one of said plurality of interactive interface devices in output data from that device.

36. The method of claim 32, further comprises the step of:

wirelessly linking a first portion of said bus in communication with said system to a second portion of said bus.

37. The apparatus for claim 32, including the step of providing game store means as one of said plurality of interactive interface devices for performing the step of:

storing a game state on a removable storage medium.

38. The method of claim 32, further comprises the steps of:

providing a photo detector means for detecting the impinging of an electron beam on said display; and

determining a vertical and a horizontal position of a location at which said electron beam is impinged upon said display.

39. The method of claim 32, further comprises the steps of:

providing stereoscopic glasses as one of said plurality of interactive interface devices; and

delaying control signals to open and close view covers of said glasses such that said signals arrive early for a subsequent occurrence of a desired opening or closing to form a best fit relationship between the implementation of said control signals and the desired opening and closing of said view covers, thereby overcoming problems associated with rise and fall times.

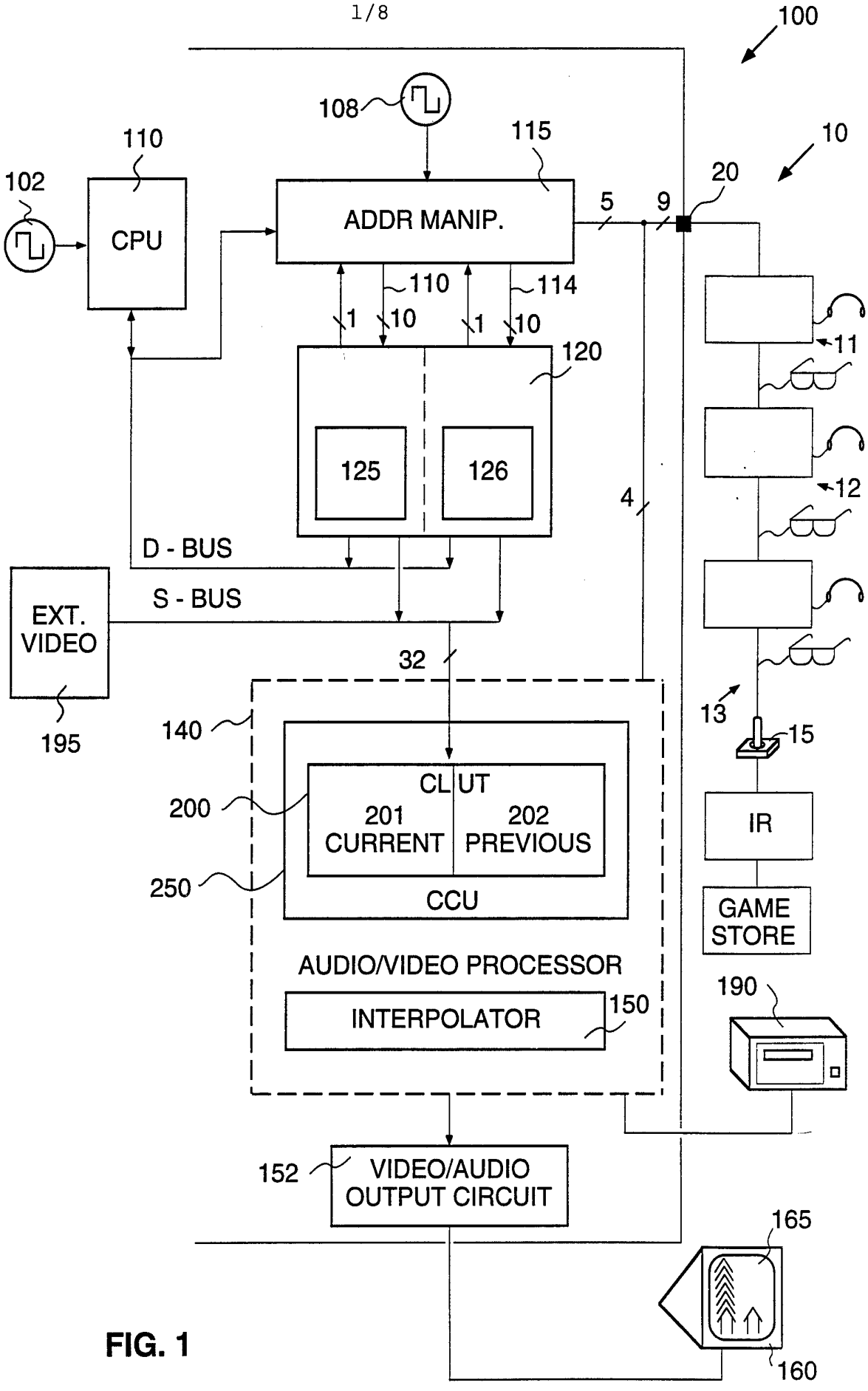

100
108
110
115
10
102
CPU
ADDR MANIP.
20
5
9
110
114
1
10
1
10
120
125
126
11
12
4
D - BUS
S - BUS
EXT. VIDEO
195
32
13
15
140
200
250
CLUT
201 CURRENT
202 PREVIOUS
CCU
IR
GAME STORE
AUDIO/VIDEO PROCESSOR
INTERPOLATOR
150
190
152
VIDEO/AUDIO OUTPUT CIRCUIT
165
160

FIG. 1

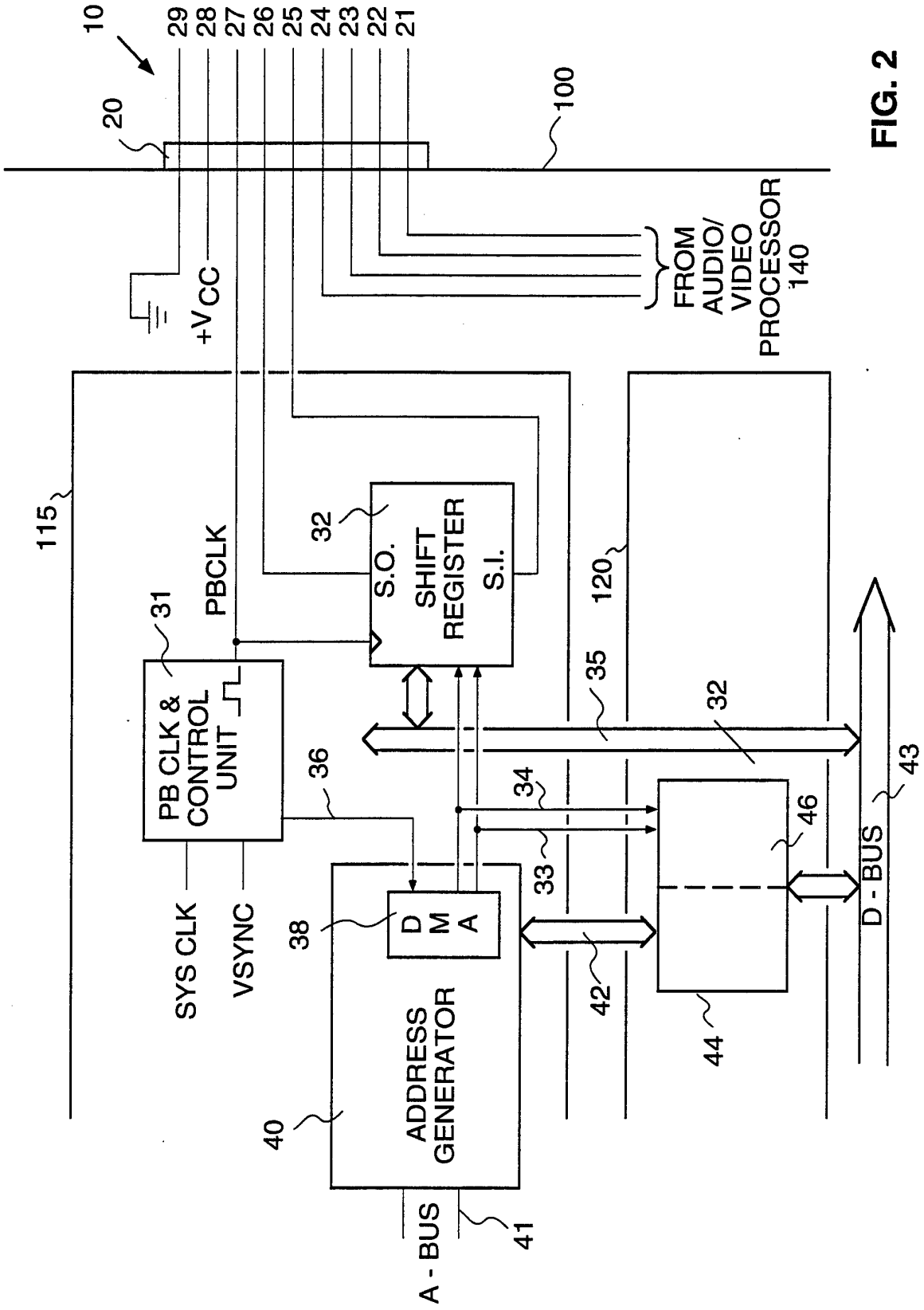

10
29
28
27
26
25
24
23
22
21
20
100
FROM AUDIO/ VIDEO PROCESSOR 140
+VCC
115
PBCLK
32
S.O.
SHIFT REGISTER
S.I.
120
31
PB CLK & CONTROL UNIT
35
32
36
34
46
43
D - BUS
33
SYS CLK
VSYNC
38
D M A
42
44
40
ADDRESS GENERATOR
A - BUS
41

FIG. 2

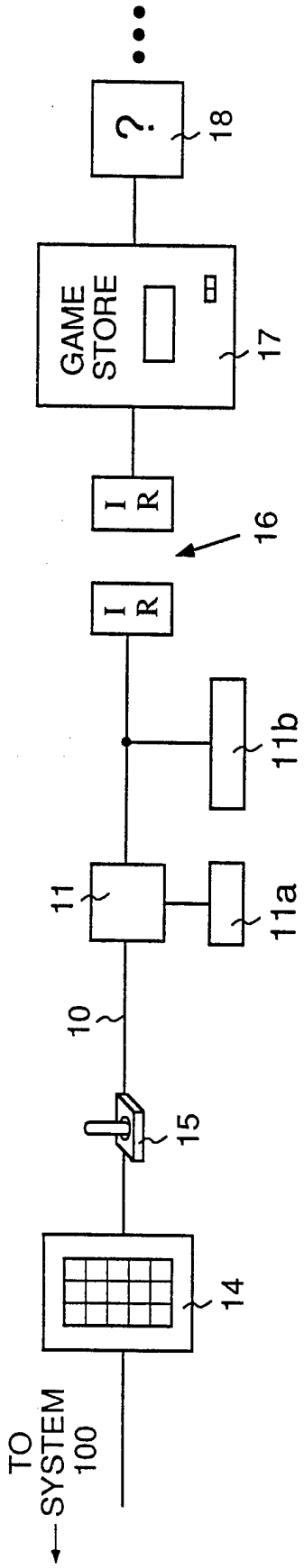


FIG. 3

FIG. 4'

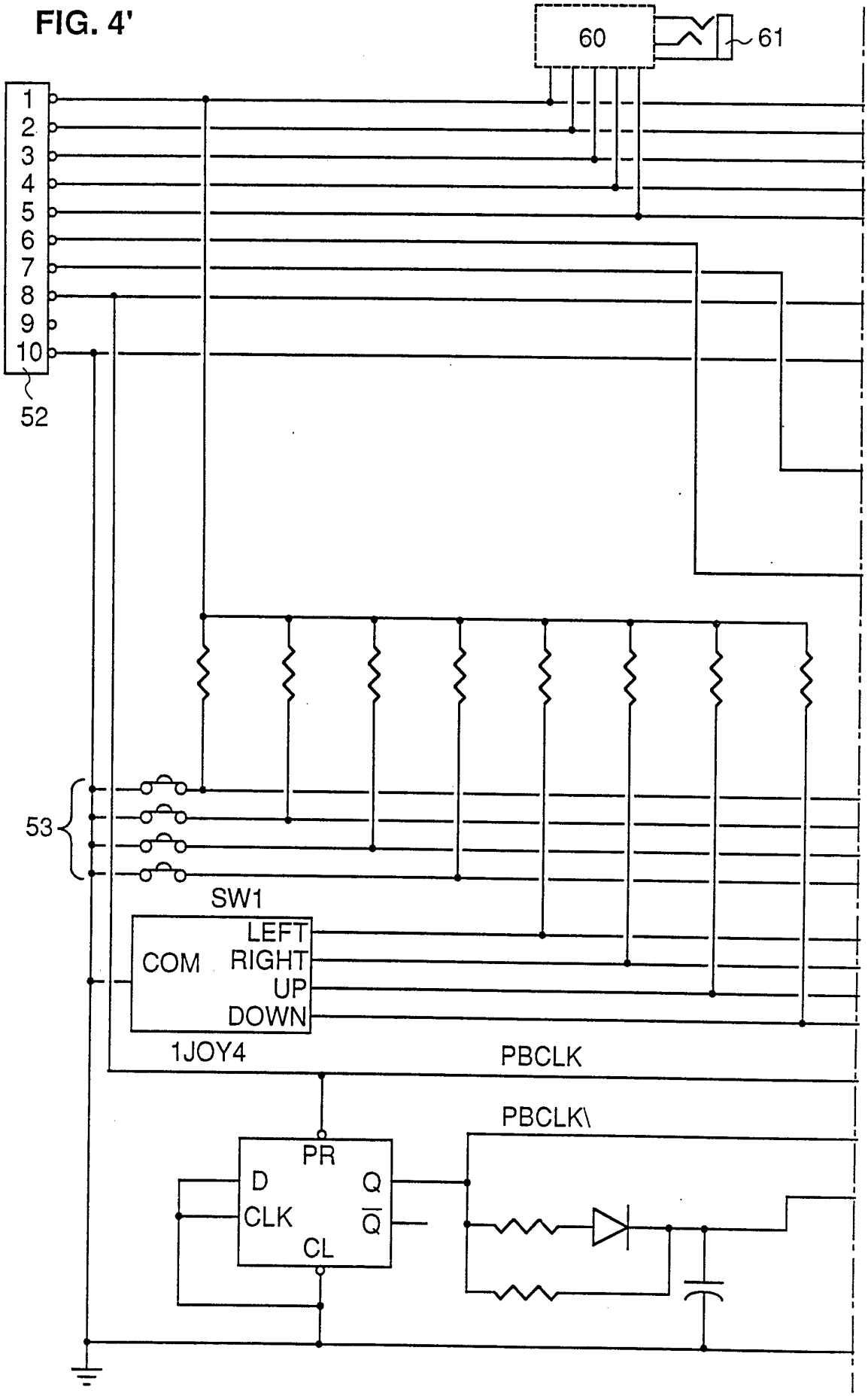
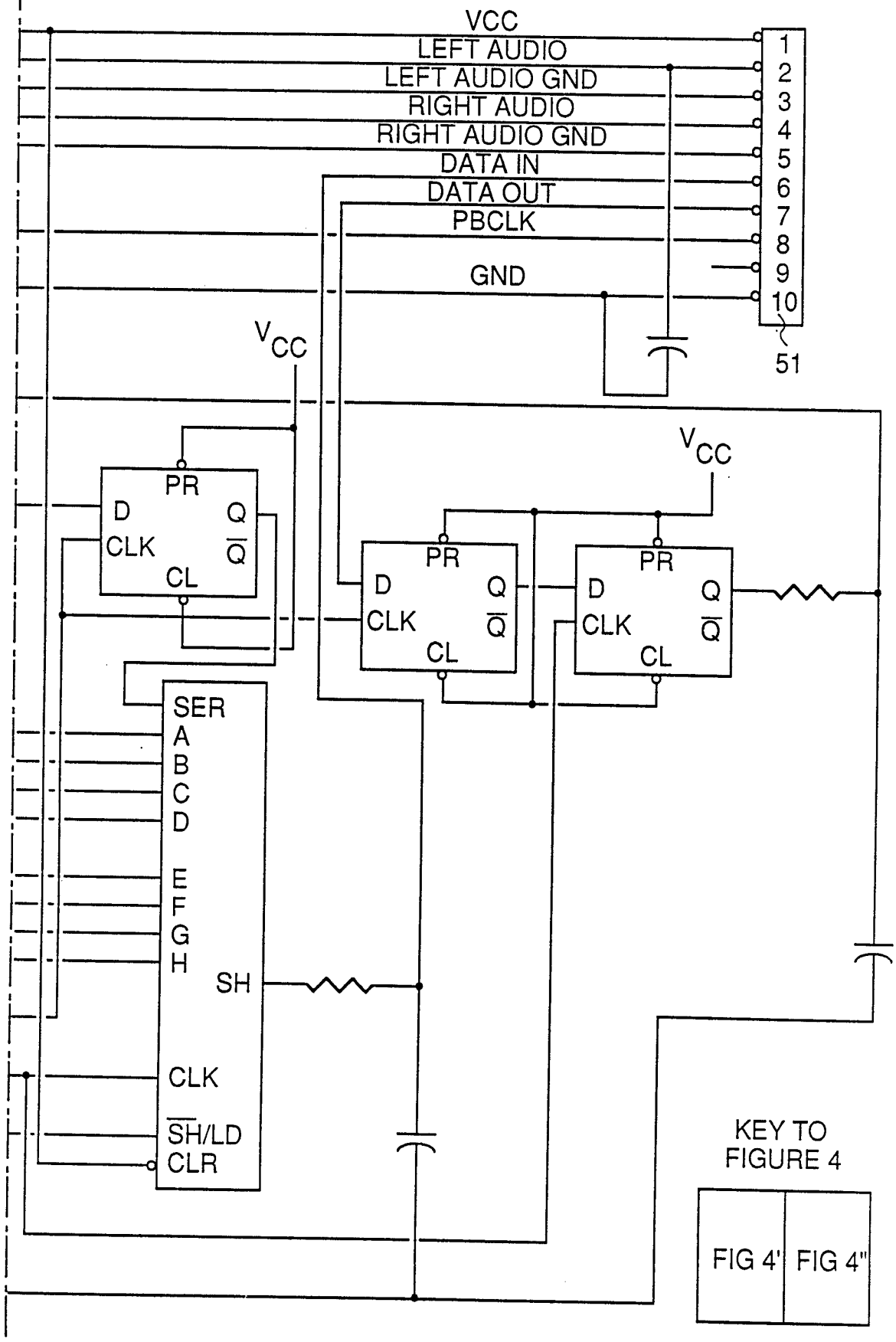

60
61
1
2
3
4
5
6
7
8
9
10
52
53
SW1
COM
LEFT
RIGHT
UP
DOWN
1JOY4
PBCLK
PBCLK\
PR
D
CLK
CL
Q
$\overline{Q}$

FIG. 4"


VCC
LEFT AUDIO
LEFT AUDIO GND
RIGHT AUDIO
RIGHT AUDIO GND
DATA IN
DATA OUT
PBCLK
GND
1
2
3
4
5
6
7
8
9
10
51
V_{CC}
V_{CC}
PR
D
Q
CLK
$\overline{Q}$
CL
PR
D
Q
CLK
$\overline{Q}$
CL
PR
D
Q
CLK
$\overline{Q}$
CL
SER
A
B
C
D
E
F
G
H
SH
CLK
$\overline{SH}$/LD
CLR
KEY TO
FIGURE 4
FIG 4'
FIG 4"

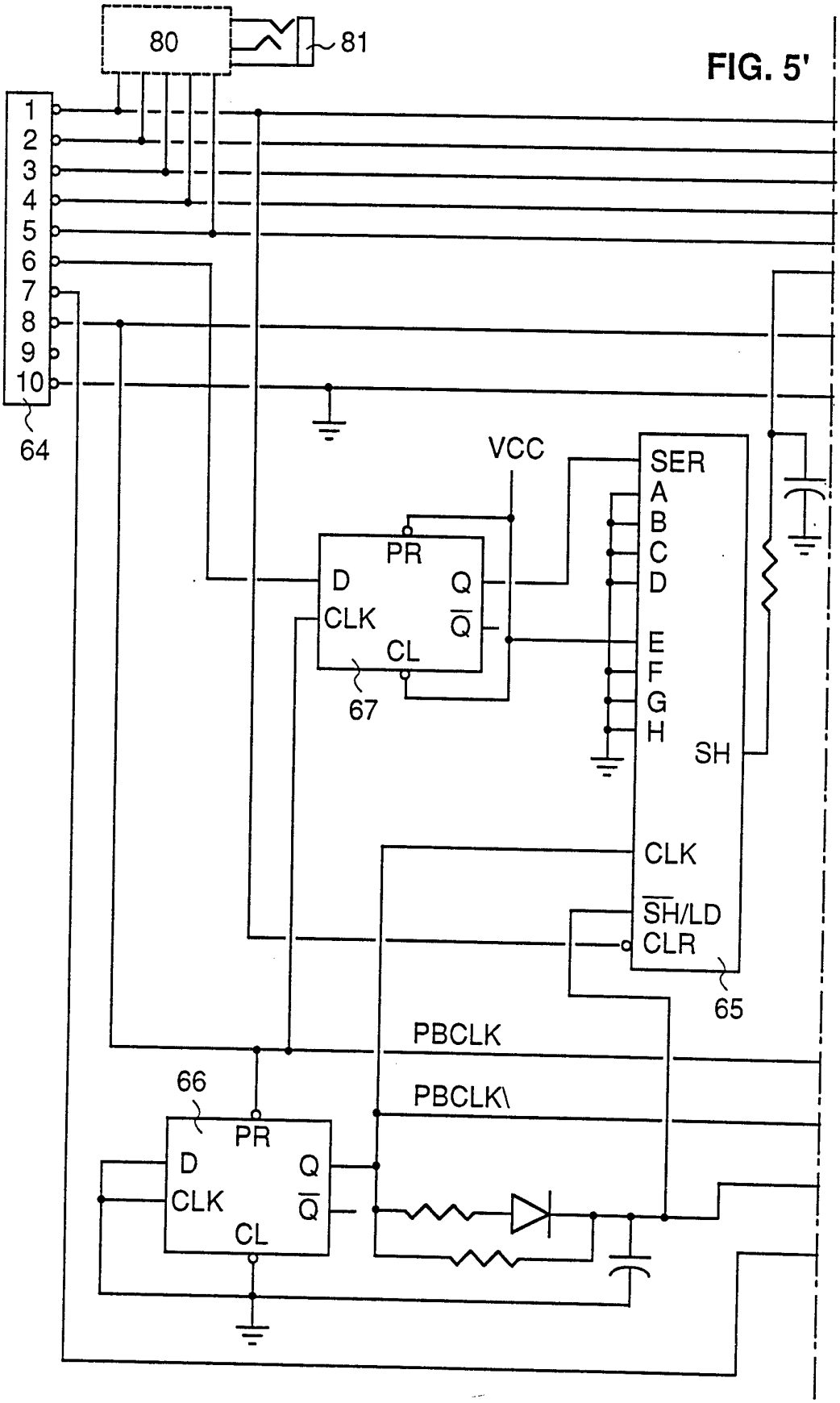
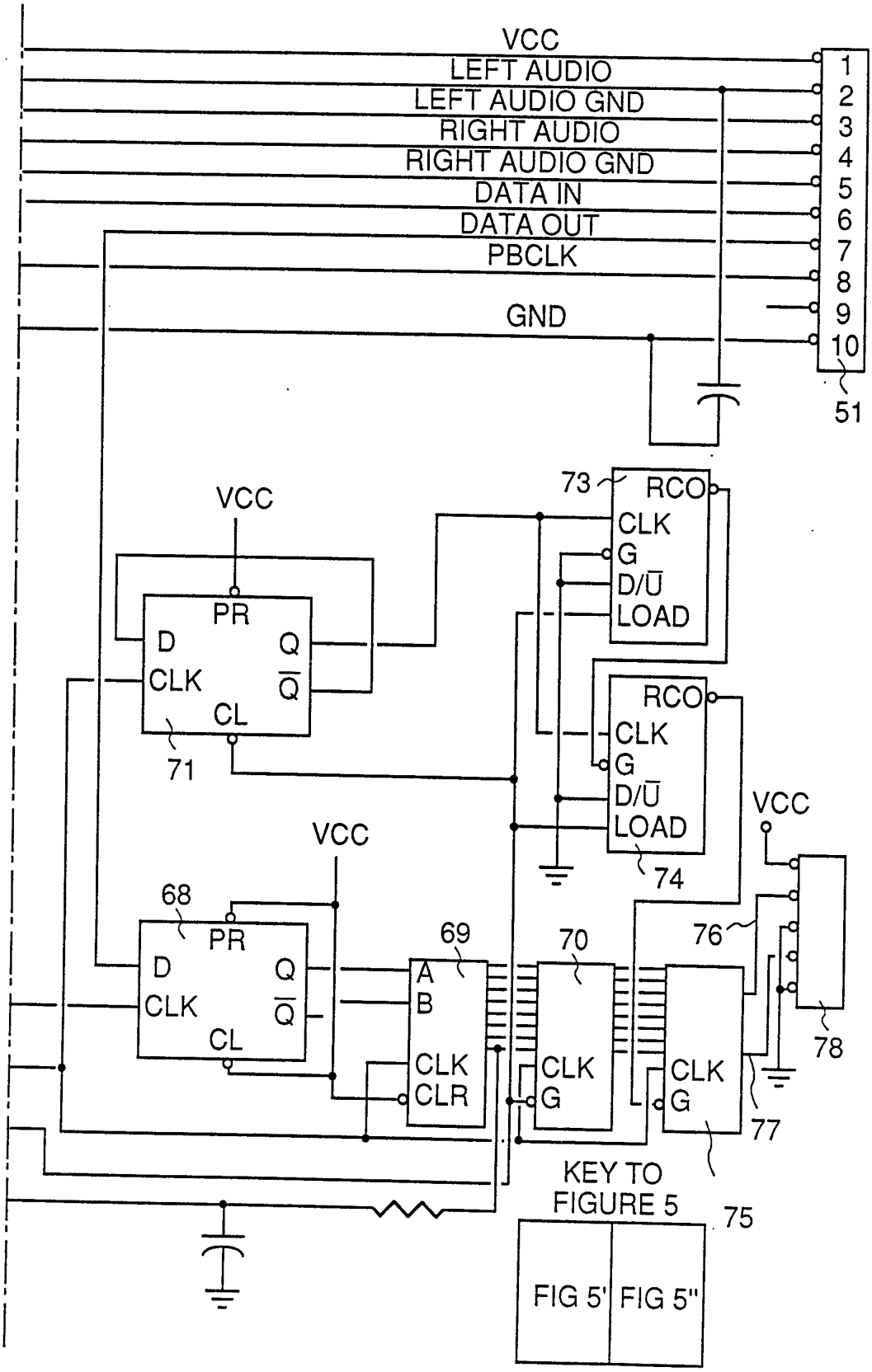

80
81
1
2
3
4
5
6
7
8
9
10
64
VCC
PR
D
CLK
CL
Q
Q
67
SER
A
B
C
D
E
F
G
H
SH
CLK
SH/LD
CLR
65
PBCLK
PBCLK\
66
PR
D
CLK
CL
Q
Q

FIG. 5'

FIG. 5"


VCC
LEFT AUDIO
LEFT AUDIO GND
RIGHT AUDIO
RIGHT AUDIO GND
DATA IN
DATA OUT
PBCLK
GND
1
2
3
4
5
6
7
8
9
10
51
VCC
PR
D
Q
CLK
Q
CL
71
73
RCO
CLK
G
D/U
LOAD
RCO
CLK
G
D/U
LOAD
74
VCC
VCC
68
PR
D
Q
CLK
Q
CL
69
A
B
CLK
CLR
70
CLK
G
CLK
G
77
76
78
KEY TO
FIGURE 5
75
FIG 5'
FIG 5"

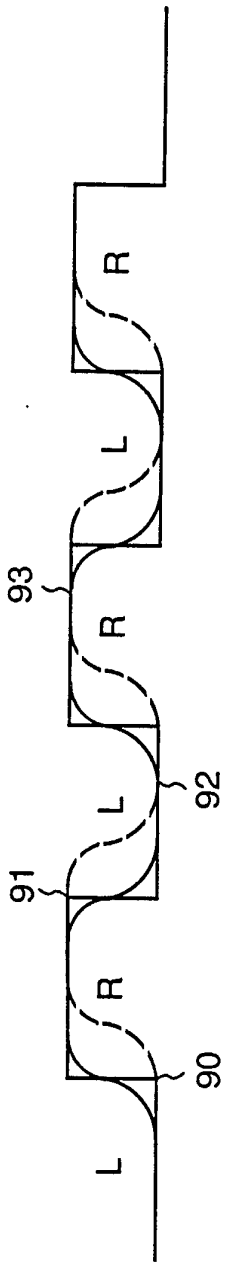


FIG. 6

INTERNATIONAL SEARCH REPORT

PCT/US92/09384

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G06F 15/20
US CL :395/152
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/153, 154, 155, 163; 340/707, 721; 358/88

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5,046,023 (Katsura et al) 03 September 1991, See figures 1-4, 8-9, 42 and 46; column 7, line 59 to column 17, line 45; column 29, lines 1-39.	1 - 6 , 1 4 , 1 6 - 18,24,25,32-35
A	US, A, 4,974,074 (Tenma) 27 November 1990, See figure 1, columns 1-5.	5,13,17,23, 25,31,39
A	US, A, 4,734,756 (Butterfield et al) 29 March 1988, See figures 1-6, 10; column 3, line 15 to column 4; column 6, line 1 to column 15, line 3.	7,15,27,13, 23,31,39

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of the actual completion of the international search 24 DECEMBER 1992	Date of mailing of the international search report 25 JAN 1993
Name and mailing address of the ISA/ US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer For KEE TUNG NGUYEN NGOC-HO INTERNATIONAL DIVISION Telephone No. (703) 308-2898

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/09384

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,647,966 (Phillips et al) 03 March 1987, See figures 4 and 5, columns 4-6.	12,22,30,38

B FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

APS
L1 148 S MULTIMEDIA?
L2 875 S DAISY CHAIN?
L3 1 S L1 AND L2
L4 58523 S PROPAGAT?
L5 11696 S INTERFAC? AND L4
L6 8027 S TRANSM? AND L5
L7 3079 S SYNCHRON? AND L6
L8 1320 S SERIAL AND PARALLEL AND L7
L9 8 S L8 AND L1
L10 1668 S STEREOSCOP?
L11 22 S L10(2W)GLASS?
L12 0 S L11 AND L1
L13 14 S L1 AND L5
L14 24 S SERIAL AND PARALLEL AND L1