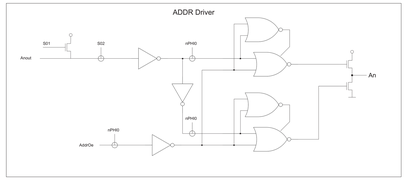
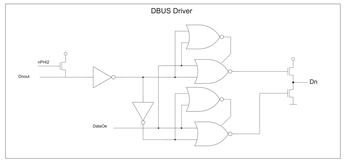
ATARI ANTIC Revision E NTSC reconstructed schematics

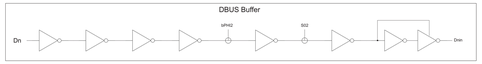
by Jorge Cwik vapi.fxatari.com
Version 1.1

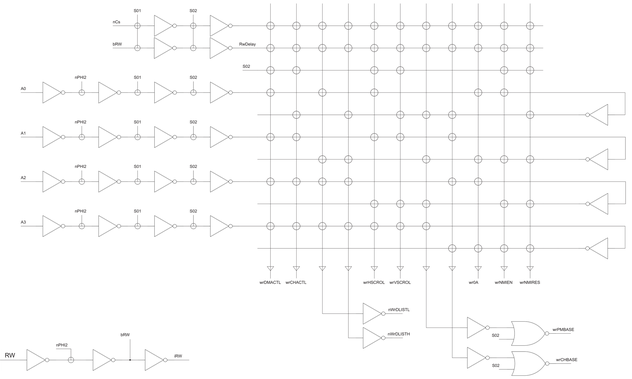
The logic of these schematics was reverse engineered from the actual chip die layout.

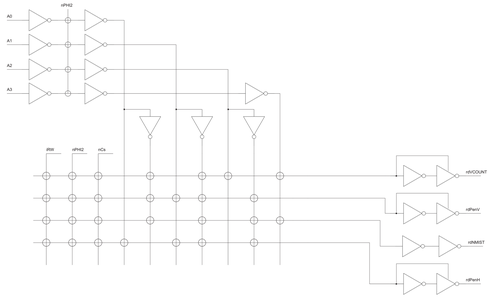
Reconstructed layout drawings are also available.


ADDR Driver
S01
S02
nPH0
Aout
An
nPH0
nPH0
AddrOe


DBUS Driver
nPH2
Dout
Dn
DataOe


DBUS Buffer
Dn
Din
S02
sPH2


S01
S02
nCs
sRW
RwDelay
A0
A1
A2
A3
nPH2
wrCMACTL
wrCHACTL
wrVSCROL
wrVSCROL
wrSA
wrMAREN
wrMARES
wrVCOLSTL
wrVBLOLSTH
wrFMBASE
wrCHBASE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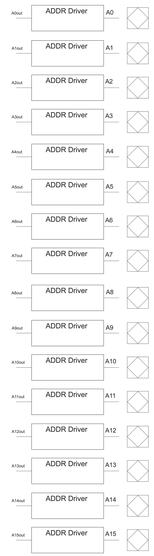
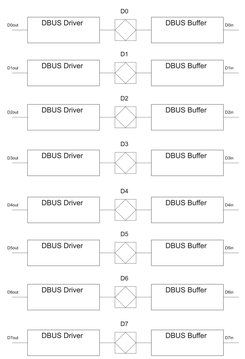
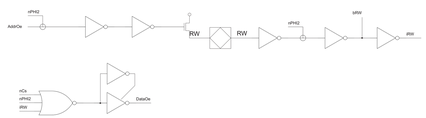
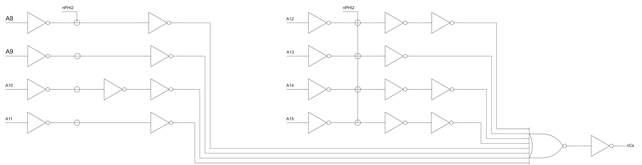
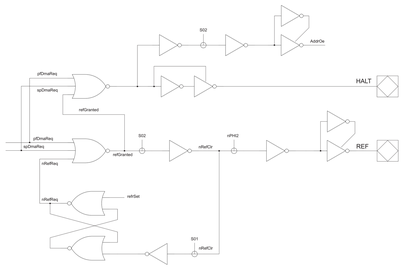
A1
A2
A3
nPH2
sRW
nPH2
nCs
nVCOUNT
nPHrrV
nINMIST
nPHmH

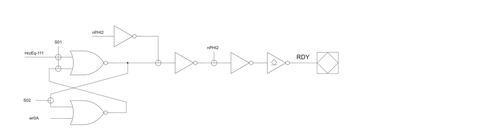

A0out
A0
A1out
A1
A2out
A2
A3out
A3
A4out
A4
A5out
A5
A6out
A6
A7out
A7
A8out
A8
A9out
A9
A10out
A10
A11out
A11
A12out
A12
A13out
A13
A14out
A14
A15out
A15
ADDR Driver

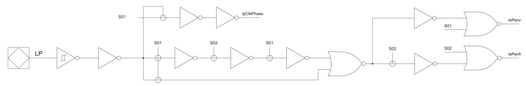

D0
D1
D2
D3
D4
D5
D6
D7
D0out
D1out
D2out
D3out
D4out
D5out
D6out
D7out
DBUS Driver
DBUS Buffer
D0in
D1in
D2in
D3in
D4in
D5in
D6in
D7in

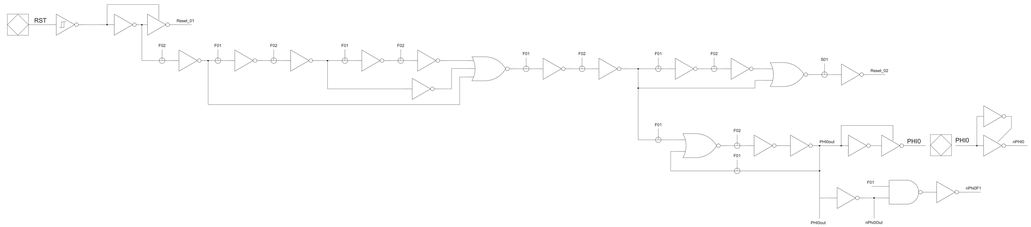

nPH2
AddrOe
RW
RW
nPH2
sRW
sRW
nCs
nPH2
sRW
DataOe

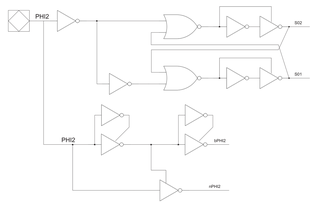

A8
A9
A10
A11
nPH2
A12
A13
A14
A15
nPH2
nCs

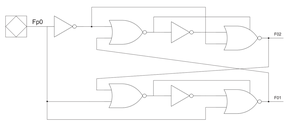

S02
AddrOe
HALT
pfDmaReq
spDmaReq
refGranted
pfDmaReq
spDmaReq
nRefReq
S02
refGranted
nRefOr
nPH2
REF
nRefReq
refSet
S01
nRefOr

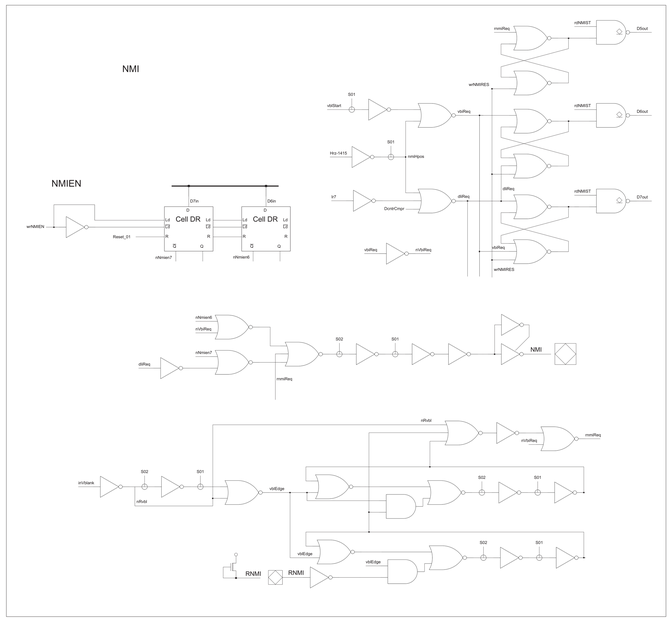

nPH2
HoldLo-11
S01
nPH2
RDY
S02
wrSA


LP
S01
S01
S02
S01
S01
S02
S02
bCkPhase
bPanv
bPanh

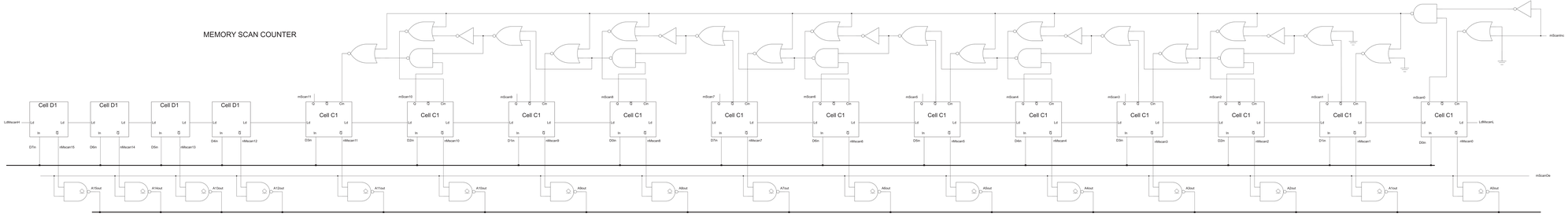

RST
Reset_01
F02
F01
F02
F01
F02
F01
F02
F01
F02
S01
Reset_02
F01
F02
PHI0out
PHI0
PHI0
nPHI2
F01
nPHI2F1
F01
PHI0out
nPHI0Out


PHI2
S02
S01
PHI2
sPH2
nPH2

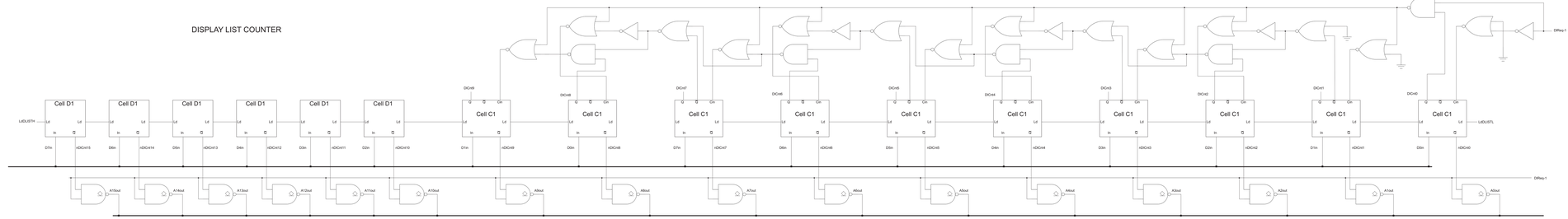

Fp0
F02
F01


NMI
nInmReq
nINMIST
DOout
wrNMIRES
vbISlwt
S01
vbReq
nINMIST
DOout
Hz-1415
S01
vmiHpos
vbReq
bY7
DuInbCmpr
nINMIST
DOout
vbReq
nVbReq
wrNMIRES
NMIEN
wrNMIEN
Reset_01
DTin
Cell DR
nNmiwr7
DOin
Cell DR
nNmiwr8
nNmiwr6
nVbReq
diReq
S02
S01
NMI
nNmiwr7
diReq
nmiReq
nRstV
nVbReq
nmiReq
srVblank
S02
S01
nRstI
vbEdge
S02
S01
vbEdge
S02
S01
vbEdge
RNMI
RNMI

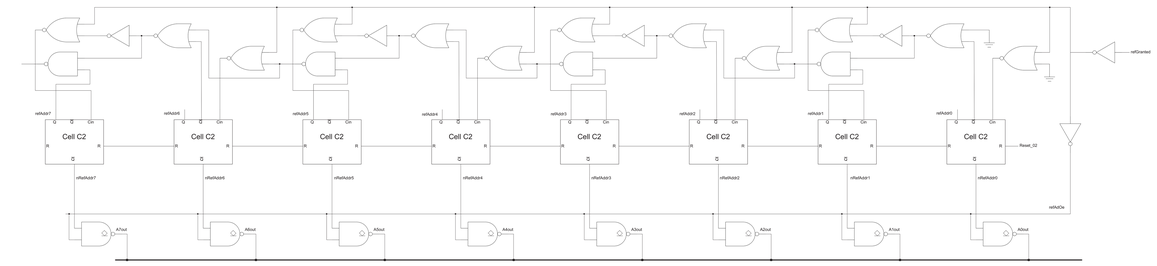
MEMORY SCAN COUNTER



DISPLAY LIST COUNTER

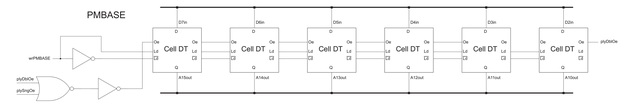


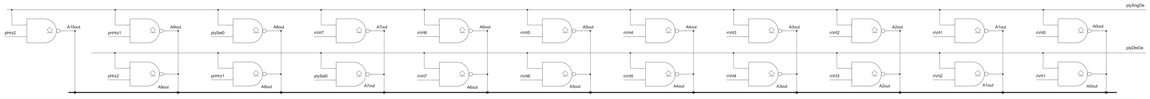
REFRESH ADDR COUNTER



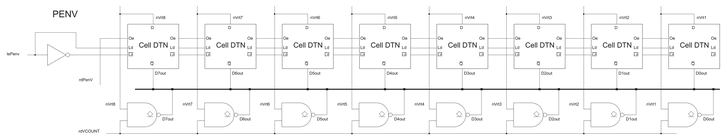
CHBASE

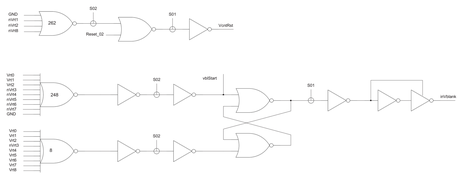
PMBASE

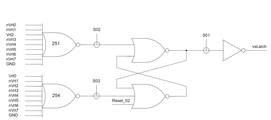


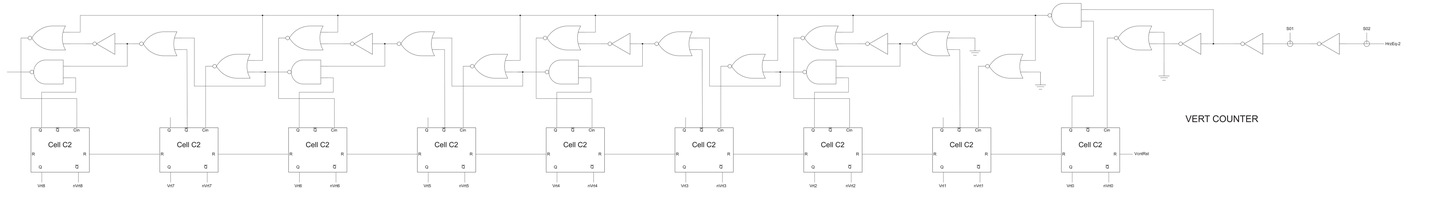


PENV

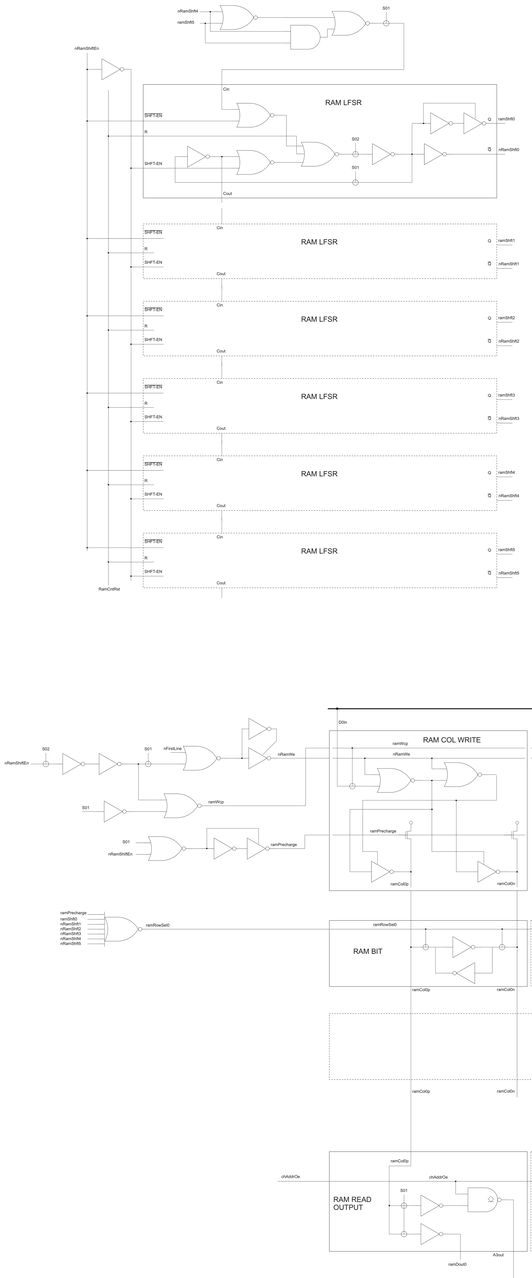








INTERNAL RAM



PLAYER MISSILE
AND DISPLAY LIST
CONTROL

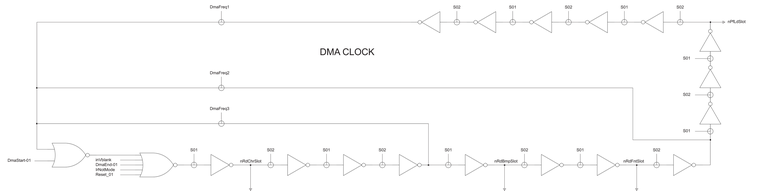
DMACTL
HIGH BITS

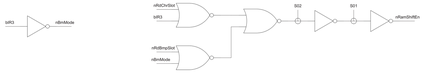
DELTA COUNTER

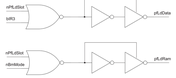
VSCROL

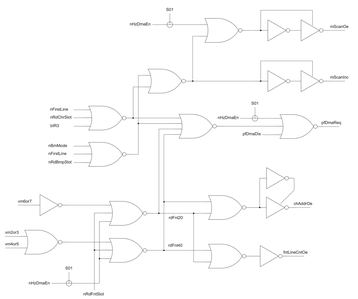
INSTRUCTION
REGISTER

DMA CLOCK

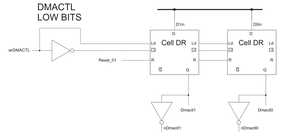


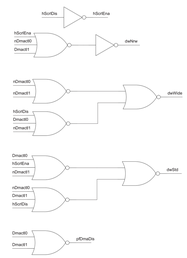




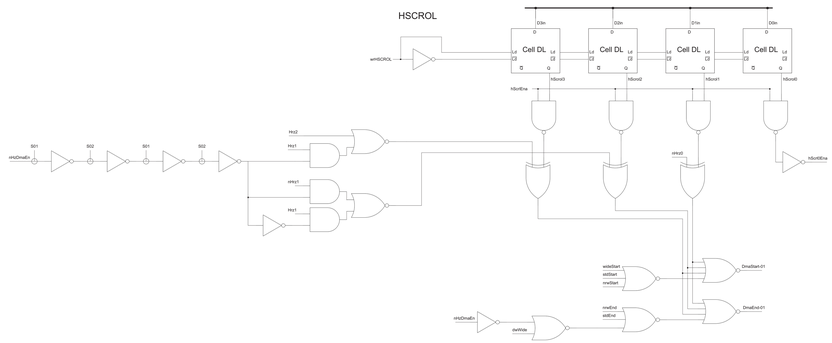


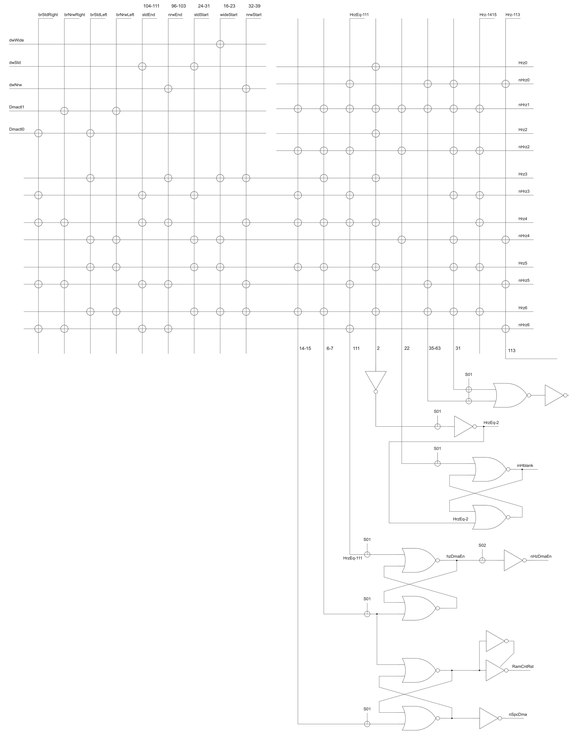
DMACTL LOW BITS



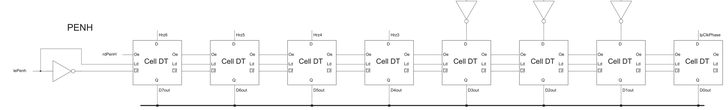


HSCROL

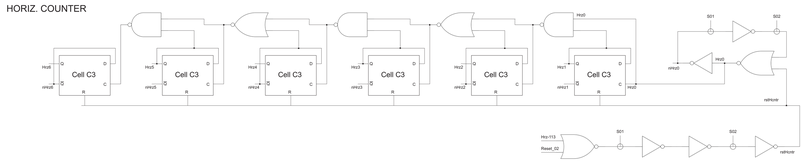


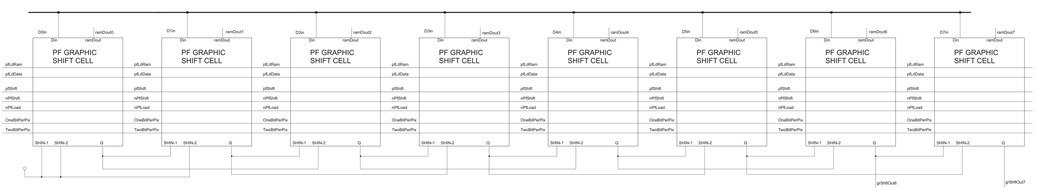


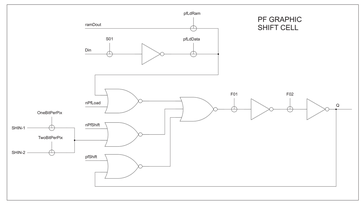
PENH

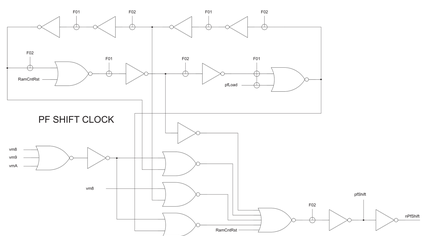
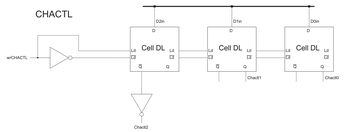
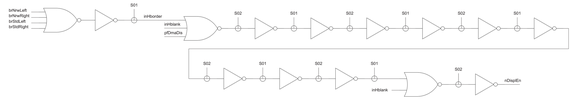
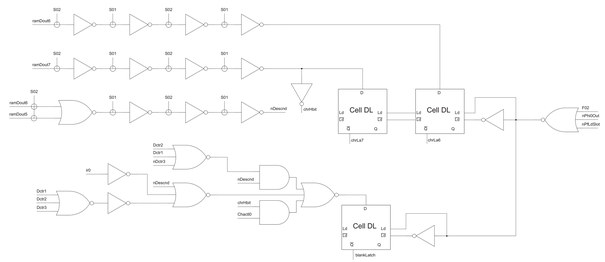
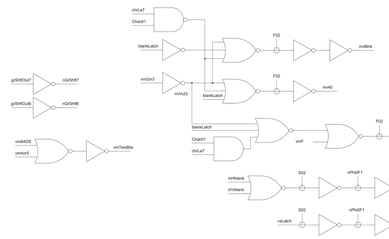
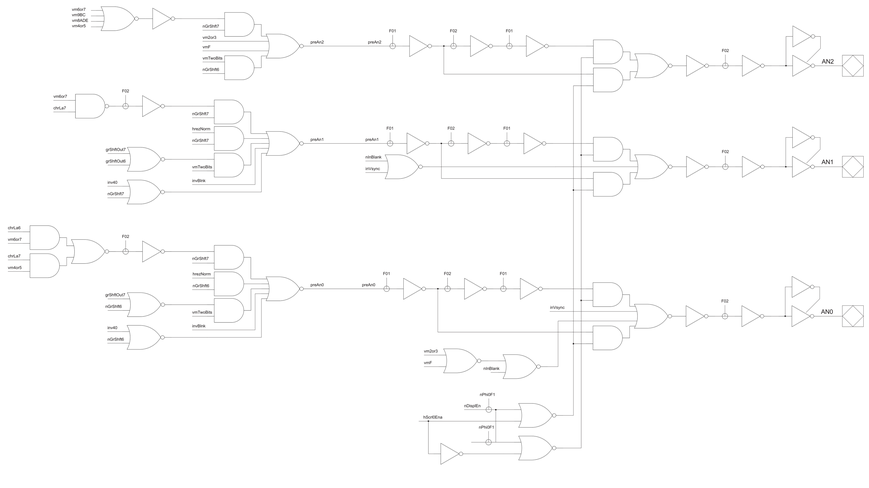
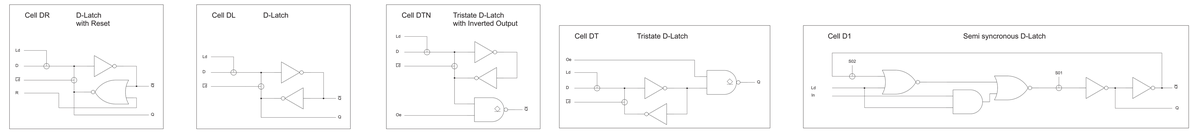
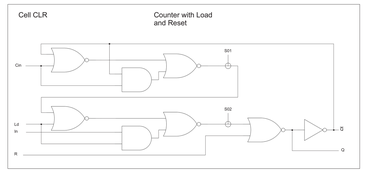
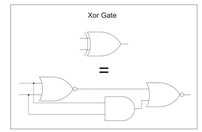
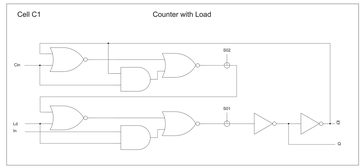
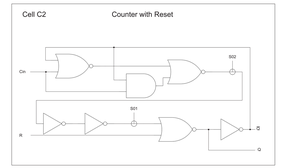
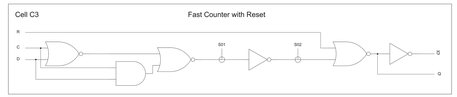


HORIZ. COUNTER









GTIA INTERFACE