Radio Shack®

Service Manual

26-3022

TRS-80®

COLOR COMPUTER
DISK INTERFACE

Catalog Number 26-3022

CUSTOM MANUFACTURED IN U.S.A. BY RADIO SHACK A DIVISION OF TANDY CORPORATION

SYSTEM DESCRIPTION

The TRS-80 Color Computer Disk Interface utilizes the WD1793 disk controller chip to provide a double density interface for mini-floppy disk drives. This interface will support up to four drives with 35 tracks per drive. The Interface also contains an 8K x 8 ROM which contains the assembly code for Disk Basic.

Figure 1 is a block diagram of the Disk Interface. The 8K x 8 ROM is connected directly to the processor address and data busses and is located at hex C000. An 8-bit register is also connected to the data bus. This register allows the processor to have command over eight disk interface control signals. Logic is also provided for clock generation, device selection, and processor halt/restart operation.

To fully understand the operation of the Color Computer Disk Interface it is necessary to refer to the data sheets for the WD1791, the WD1691, and the WD2143. The part numbers to use when ordering these data sheets are found in the Parts Lists in the back of this manual.

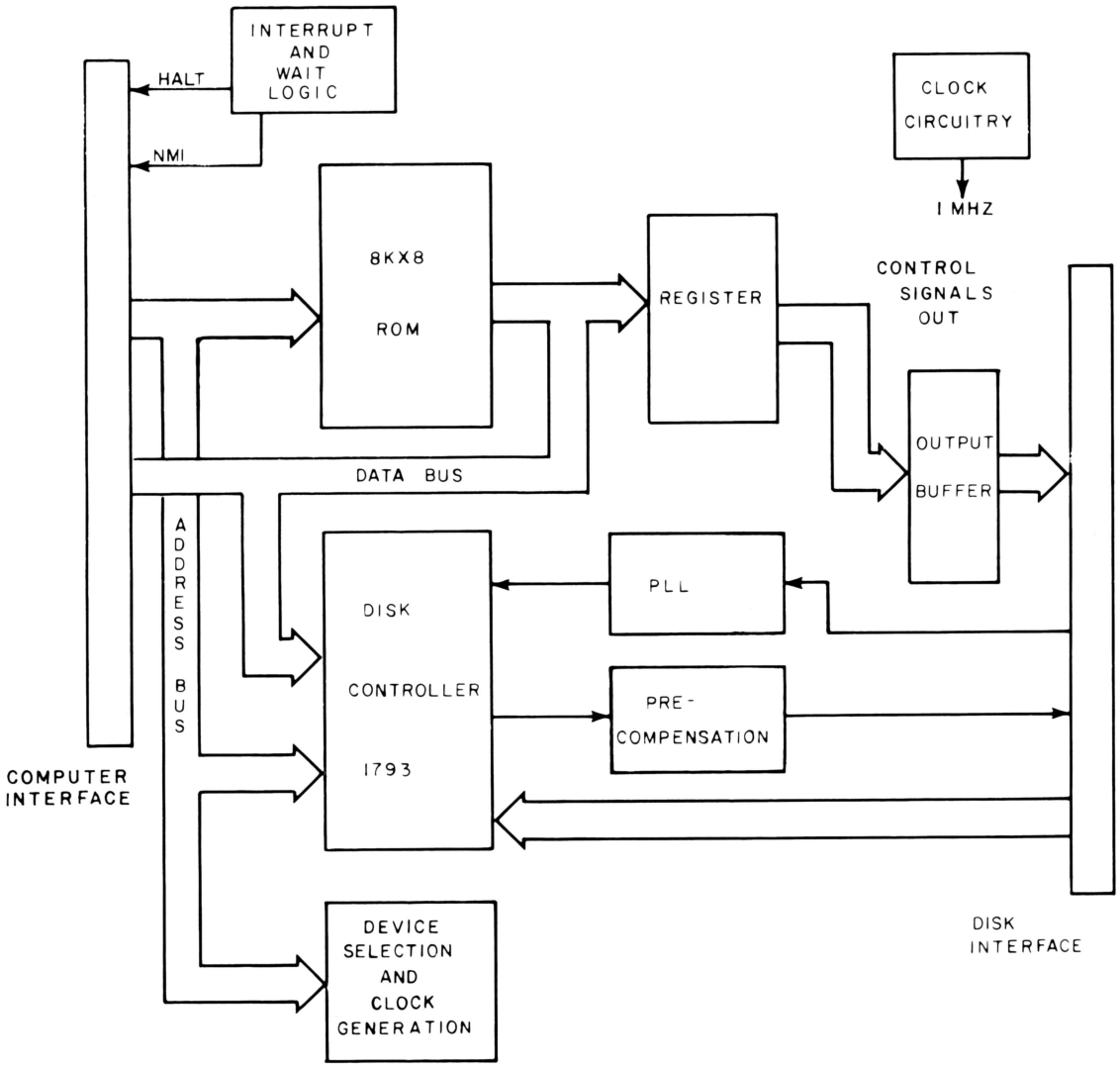


FIGURE 1. BLOCK DIAGRAM

DISASSEMBLY

1. Carefully peel back the product label to expose the screw positioned in the middle of the case top and remove this screw.

2. Gently pry the case loose at the ends with a small screwdriver.

3. Remove the two screws fastening the PC board to the case bottom and remove the RF shield from the board by carefully prying off the tri-mount fasteners.

ASSEMBLY

1. Reconnect the RF shield to the PC board so that the shiny side of the shield is away from the board. Be sure that the corner edges are folded under the shield and the fasteners are at the P2 end of the board. The flat end of the fasteners should be on the shield side of the board.

2. Place the PC board in the case bottom and install the two 1/4" screws.

3. Match up the hole in the middle of the case top with the plastic boss in the case bottom and snap the case together.

4. Replace the 1/2" screw in the case top and carefully press down the product label.

THEORY OF OPERATION

Clock Generation

The master clock frequency used on the Disk Interface board is 4 MHz. The clock circuit uses a series resonant 4 MHz crystal, Y1, and two gates from a 74LS04 hex inverter, U6. Appropriate resistor and capacitor values are added to produce a 4 MHz oscillator circuit. A third inverter gate is used to buffer the clock before it is fed into a 74LS74 chip, U1. This IC is used as a divide-by-4 counter to yield a 1 MHz clock used by the WD1793.

Computer Interface

The disk interface to the processor is composed of four parts: an 8K x 8 ROM, a control register, the WD1793, and the halt-interrupt logic. The 8K x 8 ROM simply adds the disk I/O commands to Extended Color BASIC. The control register allows the processor to enable double density and precompensation, select and start one of four drives, and enable or disable the wait logic. The function of each bit of the control register is shown in the Disk Memory Map, Figure 2.

The WD1793 contains four registers which may be accessed by the processor. These are the status/command register, the track register, the sector register, and the data register. The status register keeps track of any error which has occurred and tells the WD1793 what operation to perform. The track register keeps a record of the current track and is automatically incremented or decremented by the WD1793. The sector register should be loaded with the desired sector during a read or write operation. The data register is used during any read or write operation for transfer of data between the processor and the disk drive. For a detailed description of these registers, please consult the WD1793 data sheet.

HEX ADDRESS	DISK CONTROLLER USAGE
FF40	BIT 0 = DRIVE SELECT 1 BIT 1 = DRIVE SELECT 2 BIT 2 = DRIVE SELECT 3 BIT 3 = MOTOR ON BIT 4 = START PRECOMPENSATION BIT 5 = DOUBLE DENSITY ENABLE BIT 6 = DRIVE SELECT 4 BIT 7 = WAIT ENABLE
FF48	1793 STATUS/COMMAND REGISTER
FF49	1793 TRACK REGISTER
FF4A	1793 SECTOR REGISTER
FF4B	1793 DATA REGISTER

FIGURE 2. COLOR DISK INTERFACE MEMORY MAP

To allow the CPU to keep up with the double density interface, the data request line from the WD1793 is gated with halt enable from the control register. The resulting signal is used to control the processor halt input. The interrupt request from the WD1793 is gated with the double density enable signal from the control register and this line is used to generate a non-maskable interrupt to the CPU.

With the HALT/NMI logic, a disk read operation will operate as follows. First the CPU loads the FDC command register with the desired read operation. Next, the double density enable and halt enable control bits, D5 and D7, are set. The CPU is then immediately halted until the data register contains the first byte of data. When this data is received, the data request line of the WD1793 goes high removing the CPU from the halt state. The CPU then loads the byte of data from the WD1793 and stores it in memory. After the WD1793 data register has been accessed, the data request line goes low and the CPU is again halted. This halt and load process continues until the WD1793 generates an interrupt to indicate that the read command has been completed. This interrupt clears the halt enable control bit, D7, and breaks the CPU out of the tight read and store loop. A write operation is similar with the exception that the halt occurs after a data byte has been loaded into the data register.

Disk Communication

The major read, write, and step functions of the disk interface are performed by the WD1793. This chip will provide every major disk interface function for a single density interface with the exception of deriving a clock from the incoming data stream. However, for a double density interface, three support chips are required. These three chips are U12, a WD1691; U14, a WD2143; and U11, a 74LS629. The WD2143 is a four phase clock generator chip. The 74LS629 is a voltage controlled oscillator chip. The WD1691 ties these chips together to provide precompensation and phase-locked clock generation for the double density interface.

Precompensation is used in the double density interface for tracks greater than 21. When precompenstion is needed, the FD1793 sets either the EARLY or LATE signal high. This information is used by the WD1691 to select one of three clock phases from the WD2143. (The fourth phase is used to reset the strobe input to the clock chip.) The second phase of the clock is used for EARLY and phase three is used for LATE. A timing diagram of this sequence is shown in the WD1691 data sheet.

To read the incoming data from the disk, the WD1793 requires a clock which is synchronized with the data. This function is achieved by a phase lock loop. The 74LS629 provides a stable voltage controlled oscillator and is adjusted to free-run at 2 MHz. This 2 MHz signal is divided by 8 in the WD1691 phase comparator for a frequency of 0.25 MHz, roughly equal to the incoming clock from the disk. However, the phase comparator controls the voltage input to the 'LS629 to force the clock to exactly match the incoming data stream.

For a more detailed description of the phase lock loop, please refer to the WD1691 data sheet.

Drive Interface

The remaining circuitry of the Disk Interface is used to condition signals connected to the drive. All of the output signals are buffered by a 7416 gate, U3, an open-collector inverter. The input signals are terminated by three 150 ohm pull-up resistors, R14, R3, and R2. The read and write data signals are pulse-width adjusted with the write signal set at 450 ns, and the read signal set at 200 ns.

ADJUSTMENTS

The disk interface has three potentiometers which require adjustment: R15, R8, and R16. To adjust R15 and R8, the interface should be in the idle condition (no command currently in operation). Adjust R15 for a 1.4V level on pin 2 of U11. Adjust R8 to provide a 2 MHz square wave at pin 16 of U12.

R16 controls the amount of write precompensation and must be adjusted while executing a continuous write command. This potentiometer should be adjusted to yield pulses 200 ns wide at pin 4 of U12.

COLOR COMPUTER DISK INTERFACE
PARTS LIST

SYMBOL	DESCRIPSTION	MAN PART NO.	R.S. PART NO.
	Capacitors		
C1	180pF, 50V, ceramic	8301184	----------
C2	180pF, 50V, ceramic	8301184	----------
C3	0.1uF, 50V, mono. axial	8374104	ACC104QJCA
C4	0.022uF, 50V, cramic	8303224	ACC223QJCP
C5	0.1uF, 50V, mono. axial	8374104	ACC014QJCA
C6	0.022uF, 50V, ceramic	8303224	ACC223QJCP
C7	470pF, 50V, ceramic	8301474	ACC471QJCP
C8	100pF, 50V, ceramic	8301104	ACC101QJCP
C9	180pF, 50V, ceramic	8301184	
C10	0.1uF, 50V, mono. radial	8384104	ACC104QJAP
C11	100pF, 50V, ceramic	8301104	ACC101QJCP
C12	0f.1uF, 50V, mono. axial	8374104	ACC104QJCA
C13	0.022uF, 50V, ceramic	8303224	ACC223QJCP
C14	62pF, 50V, ceramic	8300603	----------
C15	180pF, 50V, ceramic	8301184	----------
C16	0.022uF, 50V, ceramic	8303224	ACC223QJCP
C17	0.47uF, 100V, polyester	8354475	----------
C18	0.022uF, 50V, ceramic	8303224	ACC223QJCP
C19	10uF, 16V, elect. axial	8316101	----------
C20	0.022uF, 50V, ceramic	8303224	ACC223QJCP
C21	100pF, 50V, ceramic	8301104	ACC101QJCP
C22	10uF, 16V, elect. axial	8316101	----------
C23	0.022uF, 50V, ceramic	8303224	ACC223QJCP
C24	0.022uF, 50V, ceramic	8303224	ACC223QJCP
C25	0.1uF, 50V, mono. axial	8374104	ACC104QJCA
C26	0.022uF, 50V, ceramic	8303224	ACC223QJCP
C27	0.1uF, 50V, mono. axial	8374104	ACC104QJCA
C28	0.022uF, 50V, ceramic	8303224	ACC223QJCP
C29	470pF, 50V, ceramic	8301474	ACC471QJCP
	Crystal		
Y1	4 MHz, series resonant	8409010	AMX2804
	Integrated Circuits		
U1	74LS74, dual D flip-flop	8020074	AMX3558
U2	7416, hex inverter	8000016	AMX4228
U3	7416, hex inverter	8000016	AMX4228
U4	74LS00, quad 2-in NAND	8020000	AMX3550
U5	74LS04, hex inverter	8020004	AMX3552
U6	74LS04, hex inverter	8020004	AMX3552
U7	74LS221, dual one-shot	8020221	AMX3810
U8	MCM14174B, hex D flip-flop	8030174	----------
U9	74LS02, quad 2-in NOR	8020002	AMX3551
U10	MC14013B, D flip-flop	8030013	----------
U11	74LS629, dual VCO	8020629	AMX4663
U12	WD1691, floppy support logic	8040691	AMX4471
U13	WD1793B, floppy formatter	8030793	AXX3041
U14	WD2143-01, four-phase clock	8040143	AMX4472

U15	MCM68A364, 64K ROM	8045364	AMX4895

Resistors

R1	150 ohm, 1/4W, 5%	8207115	AN0142EEC
R2	150 ohm, 1/4W, 5%	8207115	AN0142EEC
R3	150 ohm, 1/4W, 5%	8207115	AN0142EEC
R4	1.5K, 1/4W, 5%	8207215	AN0206EEC
R5	6.8K, 1/4W, 5%	8207268	AN0262EEC
R6	910 ohm, 1/4W, 5%	8207191	AN0192EEC
R7	910 ohm, 1/4W, 5%	8207191	AN0192EEC
R8	50K, trim pot	8279350	AP7168
R9	47K, 1/4W, 5%	8207347	AN0340EEC
R10	10K, 1/4W, 5%	8207310	AN0281EEC
R11	47K, 1/4W, 5%	8207347	AN0340EEC
R12	10K, 1/4W, 5%	8207310	AN0281EEC
R13	47 ohm, 1/4W, 5%	8207047	----------
R14	150 ohm, 1/4W, 5%	8207115	AN0142EEC
R15	100K, trim pot	8279410	----------
R16	1K, trim pot	9279210	AP0835
R17	750 ohm, 1/4W, 5%	8207175	AN0185EEC
R18	3.9K, 1/4W, 5%	8207239	AN0237EEC
R19	220 ohm, 1/4W, 5%	8207122	----------
R20	220 ohm, 1/4W, 5%	8207122	----------

MISCELLANEOUS

Description	Quantity	Man. Part No.	R.S. Part No.
Data Sheet, WD1691			MS-260106lH
Data Sheet, WD179X-02			MS-260106lJ
Data Sheet, WD2143			MS-260106lL
Socket, 14-pin DIP	8	8509008	--------
Socket, 16-pin DIP	3	8509003	AJ6581
Socket, 18-pin DIP	1	8509006	AJ6701
Socket, 20-pin DIP	1	8509009	AJ6760
Socket, 24-pin DIP	1	8509001	AJ6579
Socket, 40-pin DIP	1	8509002	AJ6580
Case Top	1	8719149	--------
Case Bottom	1	8719150	--------
Cable, ext. disk interface	1	8709205	--------
Fastener, tri-mount	2	8559033	--------
Label, cartridge ID	1	8789494	--------
Shield, RFI	1	8729079	--------
Screw, #6-19 x 1/2", PFH	1	8569111	--------
Screw, #6-19 x 1/4", PPH	2	8569077	--------

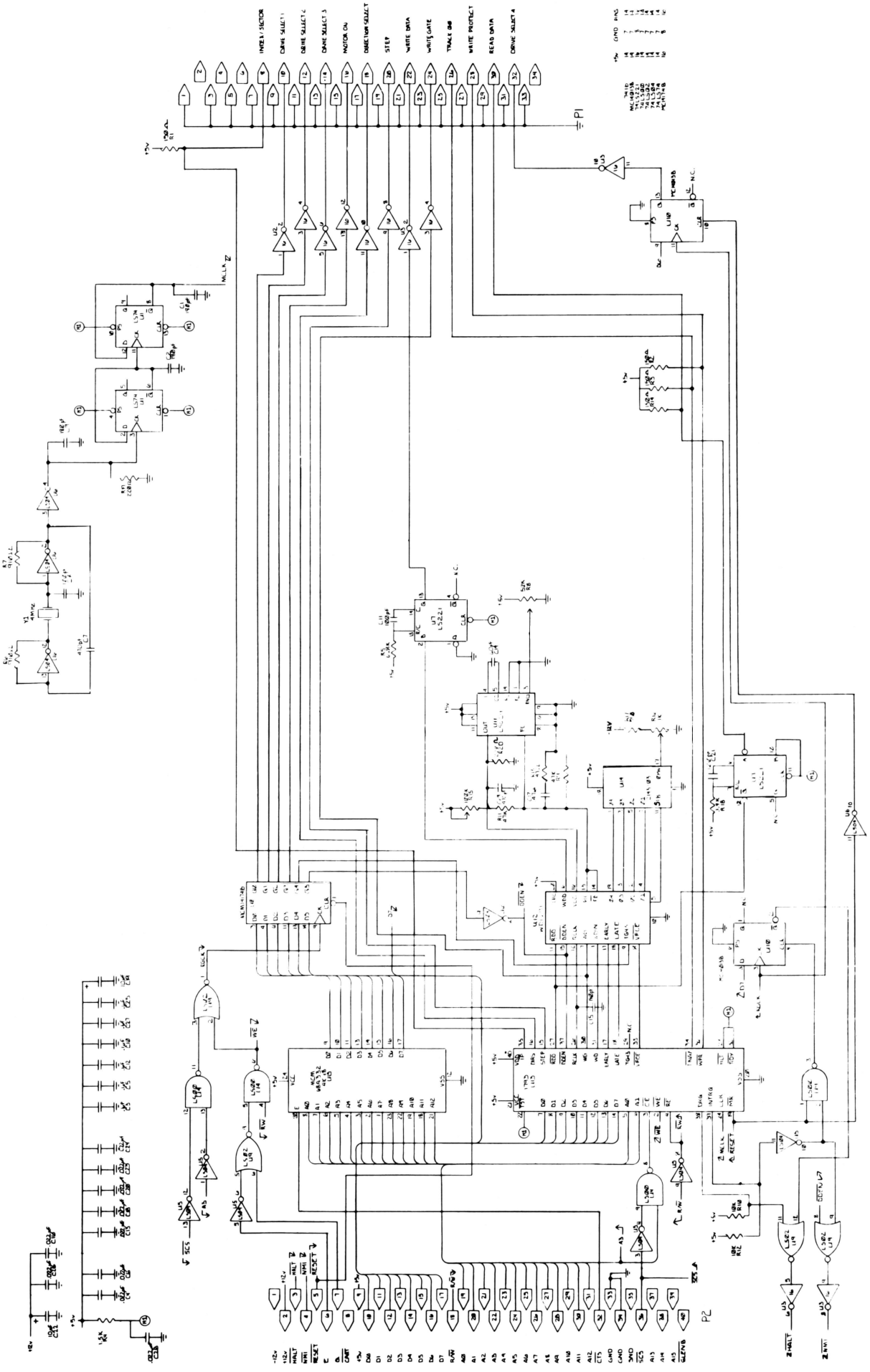
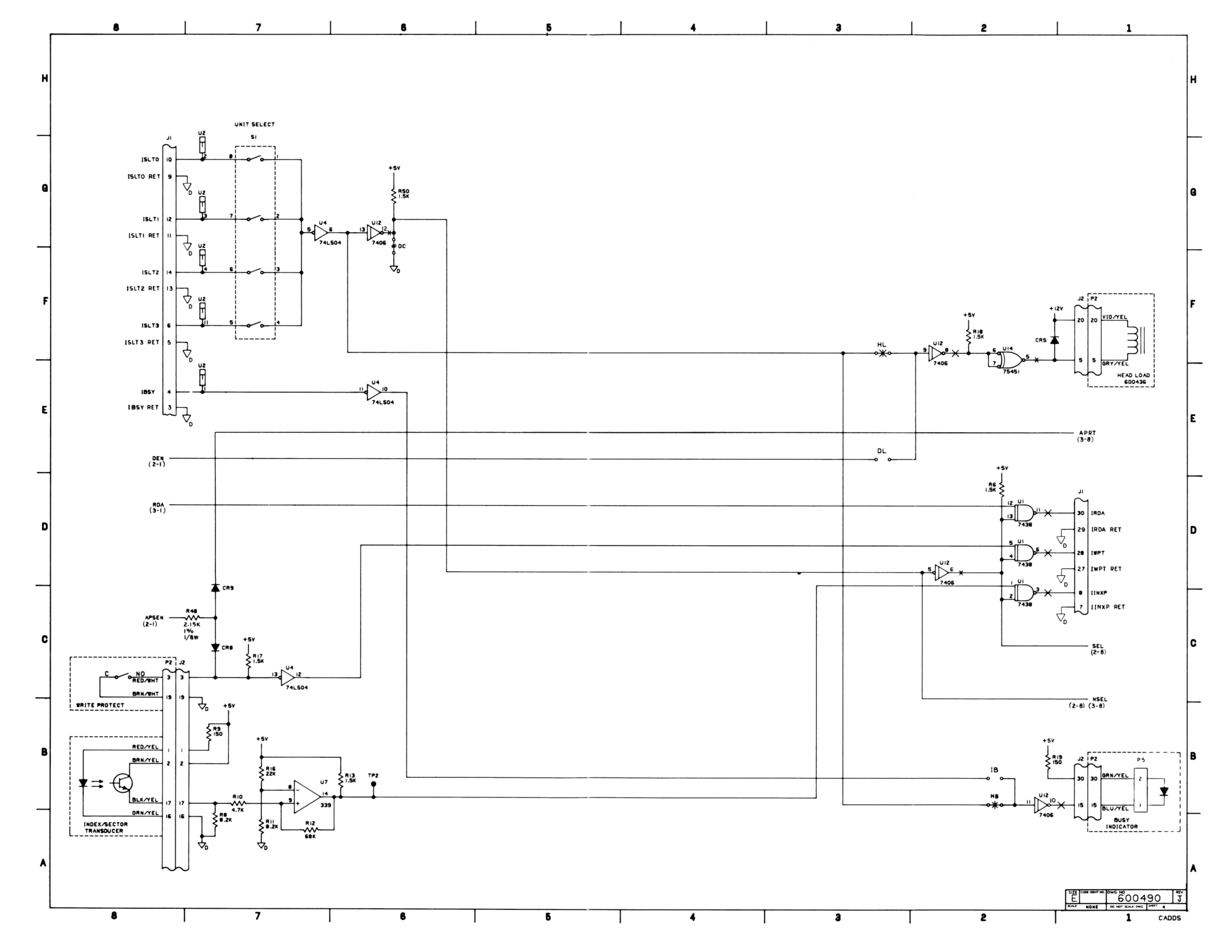


FIGURE 3. SCHEMATIC DIAGRAM



SIZE	CODE IDENT NO	DWG NO	REV
E		600490	J
SCALE: NONE	DO NOT SCALE DWG	SHEET 4	

CADDS

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