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TRS-80® COLOR COMPUTER TECHNICAL REFERENCE MANUAL

Information for Programmers and Technicians

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TRS-80™ COLOR COMPUTER TECHNICAL REFERENCE MANUAL

Radio Shack®
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FORT WORTH, TEXAS 76102

Color Computer Technical Reference Manual:
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ADI-492R2	MC6847
ADI-847	MC6809E
ADI-595	MC6883
DS9435R1	MC6821
DS-9522	MC1372

This manual was written by Dale Chatham,
and edited by Sandra Williams

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SECTION I

INTRODUCTION

SYSTEM DESCRIPTION

The primary functions of the Color Computer are performed by five 40-pin Large Scale Integration (LSI) chips plus Random Access Memory (RAM) and Read Only Memory (ROM). These five chips are indicated on the Block Diagram (Figure 1) by CPU, SAM, VDG, and two PIA's. With only these five chips plus RAM, ROM, and a power supply, the Color Computer would operate and provide a composite video output. However, to allow communication with the outside world, I/O interfaces must be added.

The main component of any computer system is the Central Processor Unit (CPU). It is the duty of the CPU to provide or request data and select the proper address for this data. In addition, the CPU is capable of performing a limited set of mathematical and logical operations on the data.

ROM has the duty of providing the CPU with a predefined set of instructions. Without ROM, the CPU would run wild and randomly execute instructions. In normal operation, the CPU jumps to the start address in ROM after the reset switch has been pressed, and then performs the reset program to set up all of the programmable devices. Following this, the BASIC instruction set residing in ROM is in control of the CPU.

RAM provides storage for the programs and/or data currently being executed. In addition, this same RAM is used to generate the video display. Normally, no conflict will be observed because the program will use one portion of RAM and the display will use another. During normal usage, the BASIC interpreter located in ROM will control the execution of programs located in RAM.

A central component in the Color Computer is the dynamic RAM controller chip (SAM). This chip provides refresh and address multiplexing for the RAM. It also provides all of the system timing and device selection.

The video display generator (VDG) provides virtually the entire video interface on one chip, and allows several different alphanumeric and graphic modes. This mode of operation of the VDG is controlled by one of two peripheral interface adapters (PIA's) used in the Color Computer. With this information and RAM data, the VDG generates composite video and color information for the modulator circuitry.

The remaining circuitry in the Color Computer is devoted to Input/Output (I/O) communication. The most important part of this circuitry is the keyboard which allows the operator to enter information. Other I/O circuits are provided to allow joystick inputs, cassette input and output, and RS232 input and output.

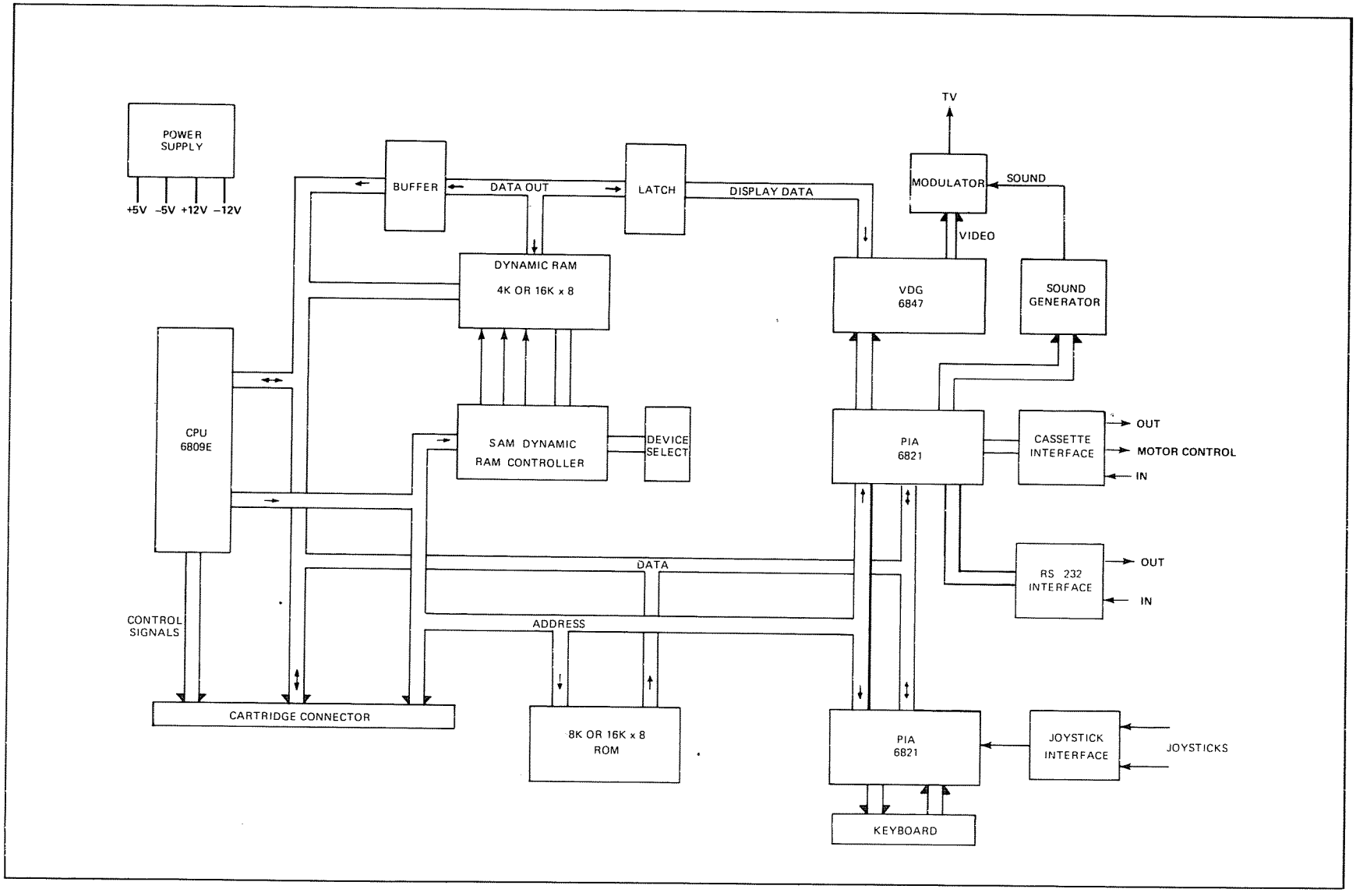


FIGURE 1. COLOR COMPUTER BLOCK DIAGRAM

MEMORY MAP

The first page of the Memory Map (page 5) shows the breakdown of the large blocks of memory in the Color Computer. One variable in this block is the video display which may be located anywhere in the memory. BASIC normally locates the video display at the Hexidecimal addresses Ø4ØØ - Ø5FF.

The next two pages of the Map explain the addressing for the PIA's. In general, the even numbered memory locations are the I/O registers and the odd numbered memory locations are the controll registers. Bit two of the control registers determines what is addressed at the even numbered memory locations. If this bit is set high (logic 1) the data I/O register is addressed. If it is set low the data direction register is addressed. Normally the data direction register is addressed only during initialization to allow configuration of the data inputs and outputs. (By clearing bit 2 and writing to the even numbered memory location one address below, each bit of the PIA may be set as an input or an output. A 1 in the data direction register sets the bit as an output and a Ø sets the bit as an input.)

The addresses from FFCØ-FFDF are the control registers for the SAM address multiplexer chip. There are no data lines to the SAM chip therefore two addresses are used to control each register. In general, writing any data to an even numbered memory location will clear the register and writing any data to an odd numbered memory location will set the register. Addresses FFCØ-FFC5 control the display mode. To select a certain display mode, both these registers and the PIA controlling the VDG chip must be set to the proper mode. However, it is also possible to set the SAM registers to one mode and the PIA controlling the VDG to another mode, and obtain a useful video mode. These cross modes are explained in more detail in the Video Interface section.

However, it is also possible to set the SAM registers to one mode and the PIA controlling the VDG to another mode, and obtain a useful video mode. These cross modes will be discussed in more detail in the Video Interface section.

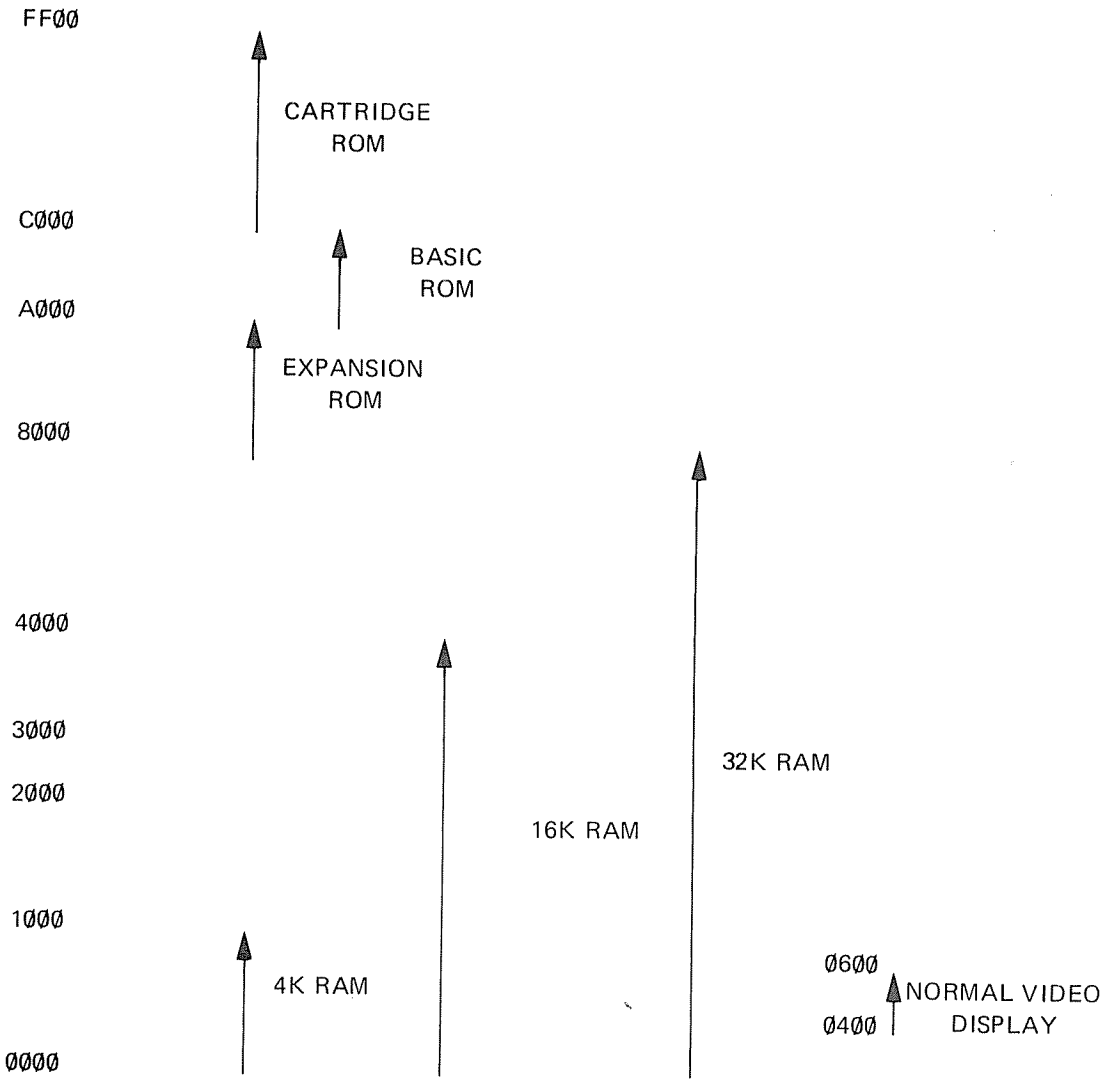
Addresses FFC6-FFD3 control the display starting address. If all of the registers are cleared, the display will begin at ØØØØ. Normally register F2 will be set causing the display to start at Ø4ØØ. This feature of the SAM chip allows the display to be paged through all of the RAM. Register P1 controls a feature which is not used in the Color Computer. Therefore, it should be cleared at all times.

Addresses FFD6-FFD9 control the clock speed of the CPU. The Color Computer is designed to operate at Ø.89 MHz.

Addresses FFDA-FFDD control the memory size set up of the SAM chip. These addresses select 4K, 16K, or 32K of RAM in the Color Computer. This memory size option should be changed only by the reset routine in BASIC. Changes at other times may erase the contents of RAM. Register TY, at addresses FFDE - FFDF, should be cleared at all times.

The final series of addresses in the Color Computer are the interrupt and reset vectors. Whenever the CPU receives a reset or interrupt it will load the address at the indicated location and begin execution at the new location. The dual set of addresses are listed because the vectors are mapped into the top of the BASIC ROM (BFF2-BFFF), i.e., if the CPU reads FFFF it will actually read the contents of BFFF.

COLOR COMPUTER MEMORY MAP



COLOR COMPUTER MEMORY MAP (cont'd)

FFØØ – FFØ3 PIA U8

FFØØ
- BIT Ø = KEYBOARD ROW 1 and right joystick switch
- BIT 1 = KEYBOARD ROW 2 and left joystick switch
- BIT 2 = KEYBOARD ROW 3
- BIT 3 = KEYBOARD ROW 4
- BIT 4 = KEYBOARD ROW 5
- BIT 5 = KEYBOARD ROW 6
- BIT 6 = KEYBOARD ROW 7
- BIT 7 = JOYSTICK COMPARISON INPUT

FFØ1
- BIT Ø, BIT 1: Control of the Horizontal sync clock (63.5 microseconds) Interrupt Input
  - Ø=IRQ* to CPU Disabled
  - 1=IRQ* to CPU Enabled
  - Ø=Flag set on the falling edge of HS
  - 1=Flag set on the rising edge of HS
- BIT 2 = Normally 1: Ø=Changes FFØØ to the data direction register
- BIT 3 = SEL 1: LSB of the two analog MUX select lines
- BIT 4 = 1 Always
- BIT 5 = 1 Always
- BIT 6 Not Used
- BIT 7 = Horizontal sync interrupt flag

FFØ2
- BIT Ø= KEYBOARD COLUMN 1
- BIT 1= KEYBOARD COLUMN 2
- BIT 2= KEYBOARD COLUMN 3
- BIT 3= KEYBOARD COLUMN 4
- BIT 4= KEYBOARD COLUMN 5
- BIT 5= KEYBOARD COLUMN 6
- BIT 6= KEYBOARD COLUMN 7
- BIT 7= KEYBOARD COLUMN 8

FFØ3
- BIT Ø, BIT 1: Control of the field sync clock 16.667 Ms Interrupt Input
  - Ø=IRQ* to CPU Disabled
  - 1=IRQ* to CPU Enabled
  - Ø= sets flag on falling edge FS
  - 1= sets flag on rising edge FS
- BIT 2 = NORMALLY 1: Ø= changes FF02 to the data direction register
- BIT 3 = SEL 2: MSB of the two analog MUX select lines
- BIT 4 = 1 Always
- BIT 5 = 1 Always
- BIT 6 Not Used
- BIT 7 = Field sync interrupt flag

COLOR COMPUTER MEMORY MAP (Cont'd)

FF20 – FF23 PIA U4

FF20

- BIT Ø = CASSETTE DATA INPUT
- BIT 1 = RS-232 DATA OUTPUT
- BIT 2 = 6 BIT D/A LSB
- BIT 3 = 6 BIT D/A
- BIT 4 = 6 BIT D/A
- BIT 5 = 6 BIT D/A
- BIT 6 = 6 BIT D/A
- BIT 7 = 6 BIT D/A MSB

FF21

- BIT Ø, BIT 1 = Control of the CD RS-232 status Input
  - Ø = FIRQ* to CPU Disabled
  - 1 = FIRQ* to CPU Enabled
  - Ø = set flag on falling edge CD
  - 1 = set flag on rising edge CD
- BIT 2 = Normally 1: Ø = changes FF20 to the data direction register
- BIT 3 = Cassette Motor Control: Ø = OFF 1 = ON
- BIT 4 = 1 Always
- BIT 5 = 1 Always
- BIT 6 Not Used
- BIT 7 = CD Interrupt Flag

FF22

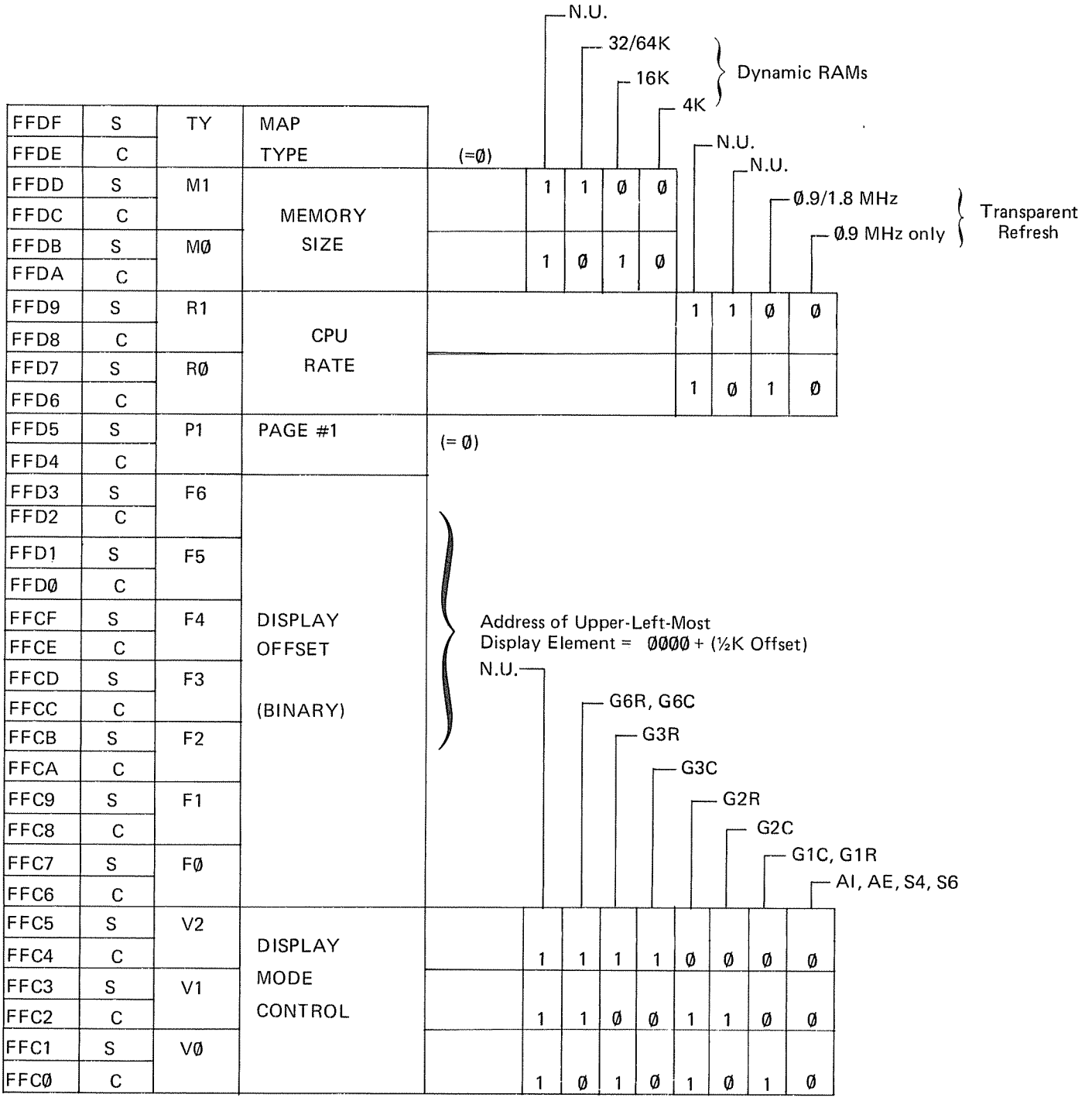
BIT Ø = RS-232 DATA INPUT		
BIT 1 = SINGLE BIT SOUND OUTPUT		
BIT 2 = RAM SIZE INPUT	LOW = 4K	HIGH = 16K
BIT 3 = VDG CONTROL OUTPUT		CSS
BIT 4 = VDG CONTROL OUTPUT		GMØ & $\overline{\text{INT}}$/EXT
BIT 5 = VDG CONTROL OUTPUT		GM1
BIT 6 = VDG CONTROL OUTPUT		GM2
BIT 7 = VDG CONTROL OUTPUT		$\overline{\text{A}}$/G

FF23

- BIT Ø, BIT 1 = Control of the Cartridge Interrupt Input
  - Ø = FIRQ* to CPU Disabled
  - 1 = FIRQ* to CPU Enabled
  - Ø = sets flag on falling edge CART*
  - 1 = sets flag on rising edge CART*
- BIT 2 = Normally 1: Ø = changes FF22 to the data direction register
- BIT 3 = Six BIT Sound Enable
- BIT 4 = 1 Always
- BIT 5 = 1 Always
- BIT 6 = Not Used
- BIT 7 = Cartridge Interrupt Flag

FF40 – FFBF NOT USED

COLOR COMPUTER MEMORY MAP (Cont'd)



FFDF	S	TY	MAP
FFDE	C		TYPE
FFDD	S	M1	MEMORY SIZE
FFDC	C		
FFDB	S	MØ	
FFDA	C		
FFD9	S	R1	CPU RATE
FFD8	C		
FFD7	S	RØ	
FFD6	C		
FFD5	S	P1	PAGE #1
FFD4	C		
FFD3	S	F6	DISPLAY OFFSET (BINARY)
FFD2	C		
FFD1	S	F5	
FFDØ	C		
FFCF	S	F4	
FFCE	C		
FFCD	S	F3	
FFCC	C		
FFCB	S	F2	
FFCA	C		
FFC9	S	F1	
FFC8	C		
FFC7	S	FØ	
FFC6	C		
FFC5	S	V2	DISPLAY MODE CONTROL
FFC4	C		
FFC3	S	V1	
FFC2	C		
FFC1	S	VØ	
FFCØ	C		

COLOR COMPUTER MEMORY MAP (Cont'd)

FFFF OR BFFF		RESET VECTOR LSB
FFFE OR BFFE		RESET VECTOR MSB
FFFD OR BFFD		NMI VECTOR LSB
FFFC OR BFFC		NMI VECTOR MSB
FFFB OR BFFB		SWI1 VECTOR LSB
FFFA OR BFFA		SWI1 VECTOR MSB
FFF9 OR BFF9		IRQ VECTOR LSB
FFF8 OR BFF8		IRQ VECTOR MSB
FFF7 OR BFF7		FIRQ VECTOR LSB
FFF6 OR BFF6		FIRQ VECTOR MSB
FFF5 OR BFF5		SWI2 VECTOR LSB
FFF4 OR BFF4		SWI2 VECTOR MSB
FFF3 OR BFF3		SWI3 VECTOR LSB
FFF2 OR BFF2		SWI3 VECTOR MSB

FFF1 – FFEØ NOT USED

SECTION II

DISASSEMBLY/ASSEMBLY

DISASSEMBLY

1. Make sure all cables (also power cord) are disconnected. Place the Color Computer face down on a padded or non-scratching surface and remove the seven screws from the Case Bottom. (Because the screws are positioned so deeply, you may not be able to actually remove them until the Computer is turned face up.)

2. Carefully place the Computer face up and lift off the Case Top and set it aside.

3. Carefully lift the Keyboard off the plastic bosses and remove the Keyboard Cable.

4. Remove the Top Cover Shield and set it aside. You may have to remove the top cover of the modulator (U5) to get the shield off.

5. Remove the three screws supporting the transformer assembly (two on transformer, one on the board) and disconnect all jumper cables.

6. Remove the ten screws fastening the CPU PC Board and lift the Board off its plastic bosses.

7. Remove the Ground Plane and Insulator from the back of the PC Board by using a screwdriver or other small, thin tool to pry off all sixteen fasteners from the rear of the Board.

REASSEMBLY

1. Replace the Ground Plane and its Insulator on back of the PC Board and install the sixteen fasteners. You may need some pliers to close the tips together and then insert.

2. Replace the PC Board onto the plastic bosses. Be sure that the ends of the Power Cord are pulled through the square cutout in the Board where the transformer is positioned.

3. Fasten the PC Board in place using ten #6 x 1/2" screws.

4. Connect the transformer jumper cables, E1 through E4 and the Power Cord jumpers, E6 - white, E5 - green, and E7 - black.

5. Position the Transformer assembly and attach jumper cable E8. Fasten using two #6 x 1 1/2" screws (on transformer) and one #6 x 1/2" screw (on board).

6. Replace the Top Cover Shield.

7. Reconnect the Keyboard Cable and Cable Shield if used. Replace the Keyboard onto the plastic bosses in the case bottom.

8. Replace the Case Top onto the Case Bottom and carefully turn the entire unit over (face down).

9. Replace the seven screws in the Case Bottom (two #6 x 7/8" toward the front and five #6 x 1 1/4" toward the rear). **Do not put the longer screws in the front positions, it could dent the Computer Case Top.**

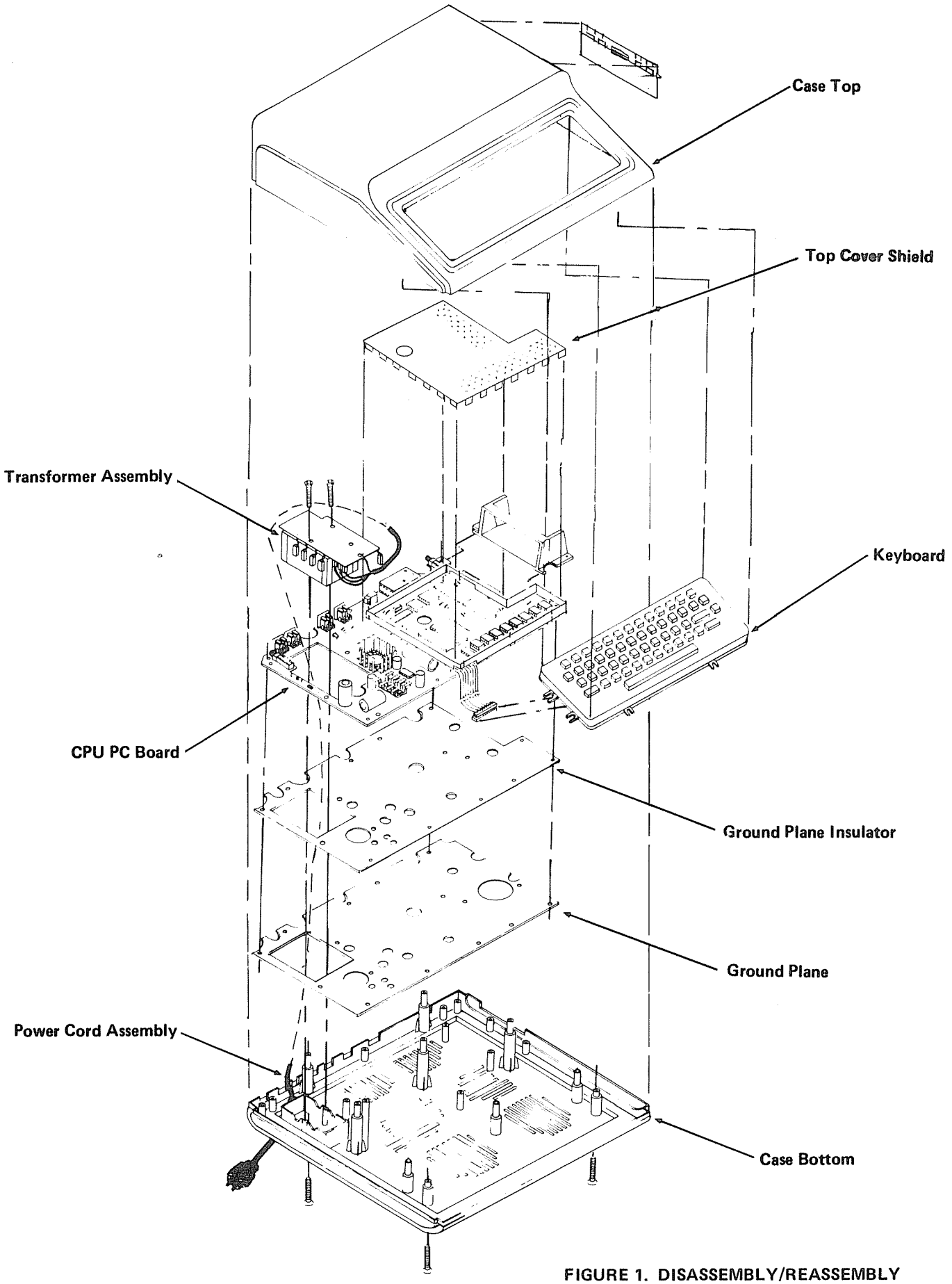


FIGURE 1. DISASSEMBLY/REASSEMBLY

SECTION III

THEORY OF OPERATION

68Ø9E CPU

The 68Ø9E is one of the most powerful 8-bit microprocessors available. The architectural features include two 16-bit index registers, two 16-bit stack pointers, and two 8-bit accumulators. A block diagram of the 68Ø9E CPU is shown in Figure 2.

Figure 3 shows the programming model of the 68Ø9E CPU. A and B are the two 8-bit accumulators. They are used for arithmetic operations and data manipulation. Also A and B may be combined to form the 16-bit register D, with A as the most significant byte. The Program Counter (PC) is used primarily for the CPU to keep track of its location in memory. X and Y are both 16-bit index registers. They are used by software to point to certain data or program segments in memory. The Hardware Stack Pointer (S) is used by the processor during subroutine calls and interrupts. Also available in the 68Ø9E is the User Stack (U) which has all of the flexibility of the Hardware Stack, and is controlled exclusively by the programmer. In addition to all of the pointers and registers the 68Ø9E also has a Direct Page Register (DP) and a Condition Code Register (CC). The Direct Page Register contents are used as the upper 8 bits of address when the direct addressing mode is used. This allows the direct mode to be used any place in memory. The Condition Code contains all of the arithmetic flags plus the mask bits for IRQ* and FIRQ*. These arithmetic flags are used to control all of the conditional branches. The mask bits allow the CPU to ignore all but the non-maskable Interrupt.

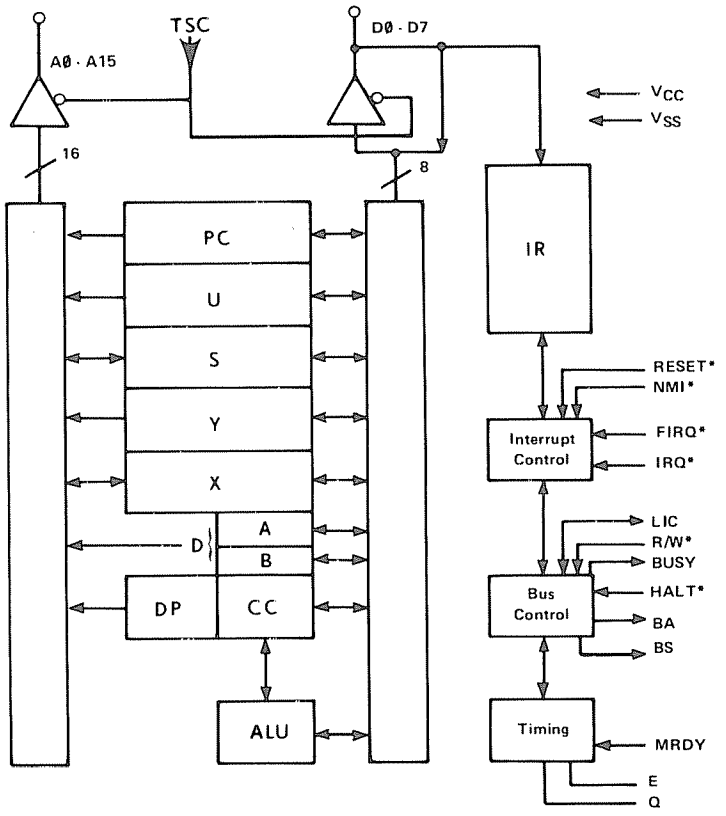


FIGURE 2. 6809E CPU BLOCK DIAGRAM

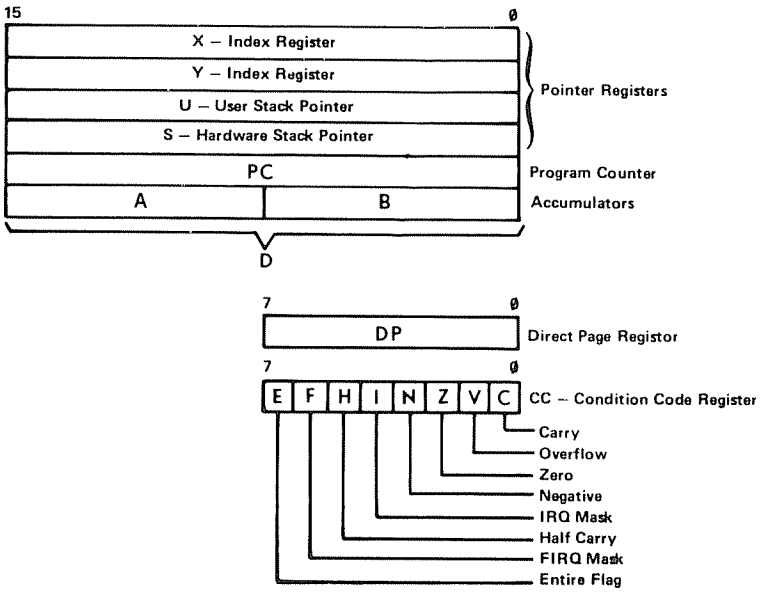


FIGURE 3. PROGRAMMING MODEL OF 6809E CPU

Figure 4 shows the typical timing for both the read and write cycle of the 68Ø9E CPU. This timing is modified by Color Computer hardware during any access of the dynamic RAM. The address from the CPU will be provided to the RAM only while the E clock is high. This presents no problem as long as the RAM is sufficiently fast.

The 68Ø9E CPU (U1) is a 4Ø-pin IC. The Color Computer uses 34 of the 4Ø possible signals. Of the 34 signals, the life blood of the computer is the address and data lines. It is the duty of the address lines to select one address out of 65,536 possible locations. After the address has been selected, the data lines either input data to the CPU or output data to the selected location. The R/W* line (pin 32) is used to determine whether a read or write operation will occur. As long as the line is high the CPU is reading data. When it goes low the CPU is writing data.

In order for the 68Ø9E CPU to function, two clock inputs must be provided, E and Q. These clocks are provided by U1Ø, an MC6883 dynamic RAM Controller chip (SAM) and are 5Ø% duty cycle clocks at a frequency of Ø.89 MHz. As shown in Figure 4, Q is a quadrature clock signal which leads E by 9Ø degrees.

The other signals generated by U1 and used by the Color Computer are the Control/Interrupt pins. The RESET* (pin 37) indicates that a power-up or RESET has occured and the CPU will start over by executing the program addressed by the top two bytes of the BASIC ROM. This program is the Reset Routine that configures all of the programmable hardware in the Color Computer.

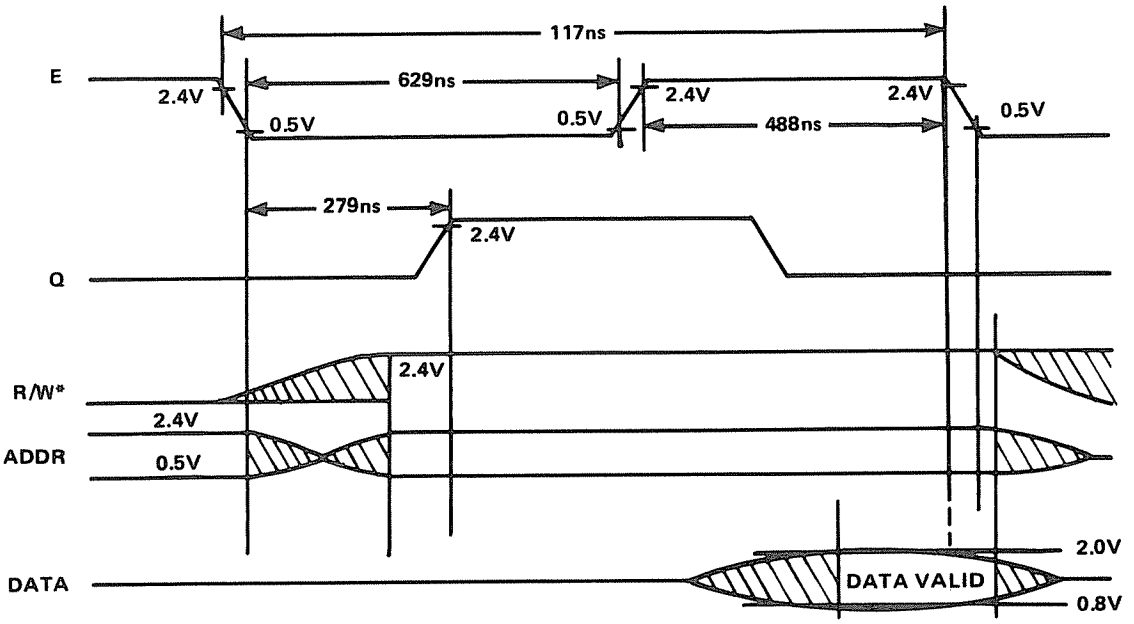
Three interrupt input pins are also used. IRQ* and FIRQ* are maskable interrupts which are connected to the PIA's and are used for multiple interrupt inputs. The non-maskable interrupt (NMI*) is reserved for Cartridge usage. All of these interrupt inputs use 4.7K pull-up resistors (R4, R5, and R6).

The last signal of the 68Ø9E CPU used by the Color Computer is HALT* (pin 4Ø). This signal also requires a pull-up resistor (R3-4.7K). When the HALT* input is pulled low, the address bus, data bus, and R/W* line are all placed in the tri-state condition. This allows an external device to control the computer via the Cartridge connector.

RESET CIRCUIT

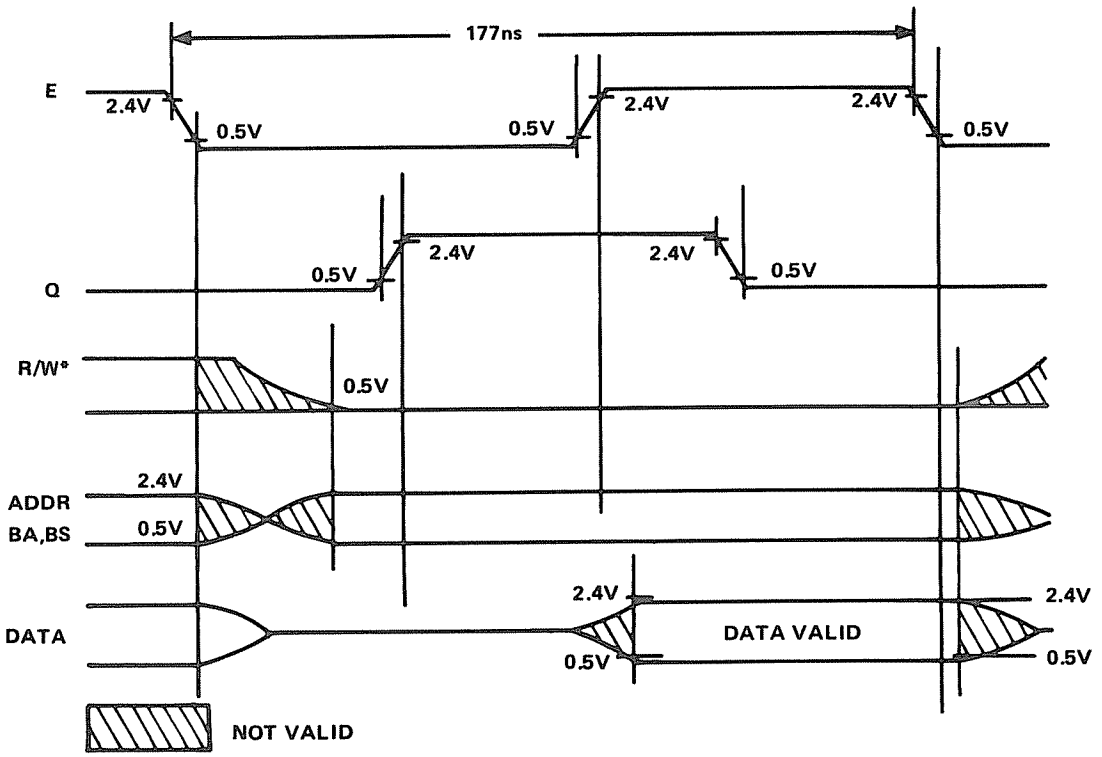
The reset circuitry is composed of R1, R2, C1, C4Ø, CR1, CR2, and CR3. This circuit provides two different time duration pulses for power-up or reset. R1 and C4Ø provide a pulse of approximately 1Ø milliseconds which is used to reset the MC6883 memory controller chip (U1Ø). The reset input to U1Ø is also used as an output, so diode CR2 is used to isolate the output signal on pin 7 from the reset circuitry.

The second reset pulse is the master system reset signal. This is provided to the CPU and both PIA's (U4 and U8). C1 and R2 provide this master reset pulse of approximately Ø.1 sec. CR1 is used to isolate the two RC circuits. CR3 allows a quick discharge of C4Ø and C1 for rapid multiple resets.



READ DATA TIMING

NOT VALID



NOT VALID

WRITE DATA TIMING

FIGURE 4. CPU READ/WRITE TIMING

DYNAMIC MEMORY CONTROL

One of the most important chips in the Color Computer is the MC6883 (U1Ø). This chip is a synchronous address multiplexer, sometimes referred to as SAM. SAM generates all of the system timing for the Color Computer and all of the device selection. In addition, it generates video address lines and multiplexes these with the CPU address lines for the dynamic memory. A funtional block diagram of the MC6883 is shown in Figure 5.

To control this versatile chip, a 16-bit control register is used. These sixteen bits are divided as follows:

VDG ADDRESSING MODE	– 3 bits
VDG ADDRESS OFFSET	– 7 bits
PAGE SWITCH	– 1 bit
MPU RATE	– 2 bits
MEMORY SIZE	– 2 bits
MAP TYPE	– 1 bit

To set one of these bits, an odd address in the range of FFCØ-FFDF is written to. To clear one of the bits, an even address in the same range is written to. The Memory Map (page 10) shows the breakdown of these bits.

The Color Computer timing chain begins with the 14.31818 MHz oscillator composed of R43, X1, C51, C4, and the internal oscillator in the MC6883. This is a series resonant circuit. C51 and C4 are used to exactly fix the frequency of the oscillation. C4 is a variable capacitor which allows minor frequency adjustments to compensate for device variation. C4 should be adjusted to give a video clock frequency of exactly 3.579545 MHz. R43 is used to control the voltage output of the oscillator.

From the master clock frequency of 14.31818 MHz, all of the system timing is derived. Figure 6 shows the breakdown of the master clock frequency to generate the timing signals. The video clock is exactly 14.31818 MHz/4 and must be the most accurate frequency in the Color Computer to provide a color picture. The next two signals, E and Q, are used by the CPU (U1). These signals are equal to the master clock divided by 16; a frequency of 0.89 MHz. The Q signal leads the E signal by ninety degrees.

The E clock is the most important timing signal to the CPU and the multiplexing of RAM addresses roughly follows this signal. RAS* and CAS* are also triggered to occur at Ø.89 MHz. RAS* strobes a row address into the dynamic RAM, and CAS* strobes a column address into RAM.

Figure 6 also shows the division of the RAM between the video address lines and the address lines from the CPU. During any CPU cycle, the RAM is only available to the CPU during the active portion of the E clock. However, this is sufficient if the RAM is capable of completing a Read or Write cycle during this time (the cycle time is a simple matter of specifying the correct access time for the RAM). The RAM is available to the video display during the low portion of the E clock (in actual fact, the display only requires the RAM during every other cycle of the E clock). To make this VIDEO/CPU multiplexing work, the MC6883 chip (U1Ø) must keep the video display address lines in sync with the 68Ø9E CPU (U1) address lines; otherwise, a conflict could develop between the CPU and the video display. The sync process is accomplished immediately following reset by stopping the video clock until the VDG is in sync with the CPU.

The next major function of the MC6883 is address multiplexing for the dynamic RAM. First, the video address lines are reproduced, using FS*, HS*, DAØ, and the VDG mode information (FS* is detected when DAØ is in the tri-state mode). These address lines are then added to the upper address lines from the address offset register to form the complete video address. The video address lines are then connected to the multiplexer bank. Also connected to the multiplexer bank is a 7-bit refresh counter. This 7-bit counter is used during horizontal sync to refresh the RAM. At other times this function is performed by the video address lines.

The multiplexer bank first selects either video/refresh address lines or CPU address lines. Next, the multiplexer selects between row and column address lines. The multiplexer then distinguishes between 4K, 16K, or 32K dynamic RAM's and presents the seven or eight address lines for the RAM's at the MC6883 output pins (pins 28 - 34).

The last major function of the MC6883 is device selection. The sixteen address lines from the CPU are used to select either the internal registers of the MC6883 or up to eight external devices. This memory map is shown in detail on pages 5 through 9. However, before the eight device selects leave the chip, they are multiplexed into three lines. At the output of the MC6883, a 74LS138 is used to de-multiplex the device selects. This 74LS138 (U11) allows the Color Computer to select between RAM, three sources of ROM, or the two PIA's. Also one NOR gate (U29 – 74LS02) is used to produce a clocked select signal for the ROM's and the RAM.

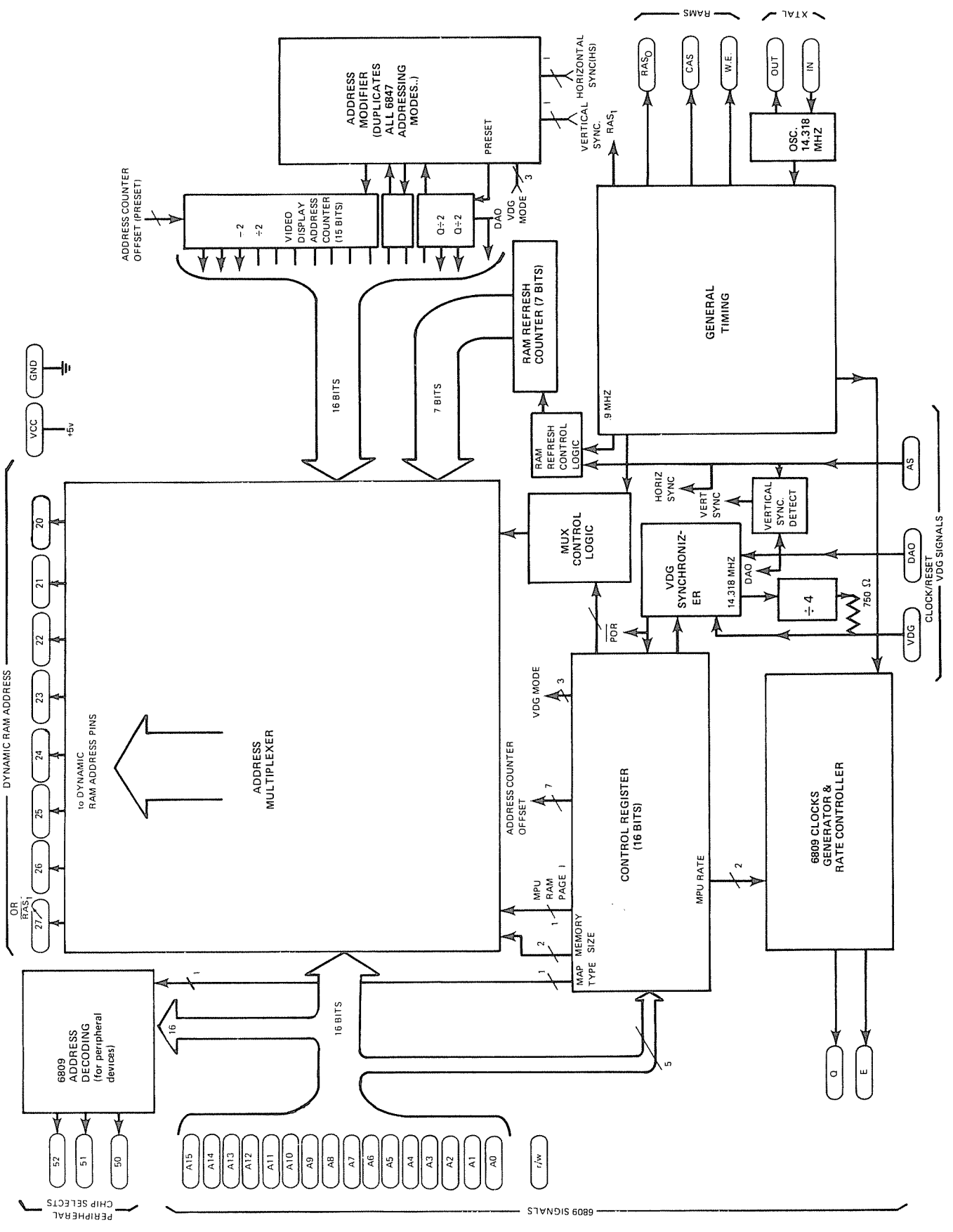


FIGURE 5. MC6883 BLOCK DIAGRAM

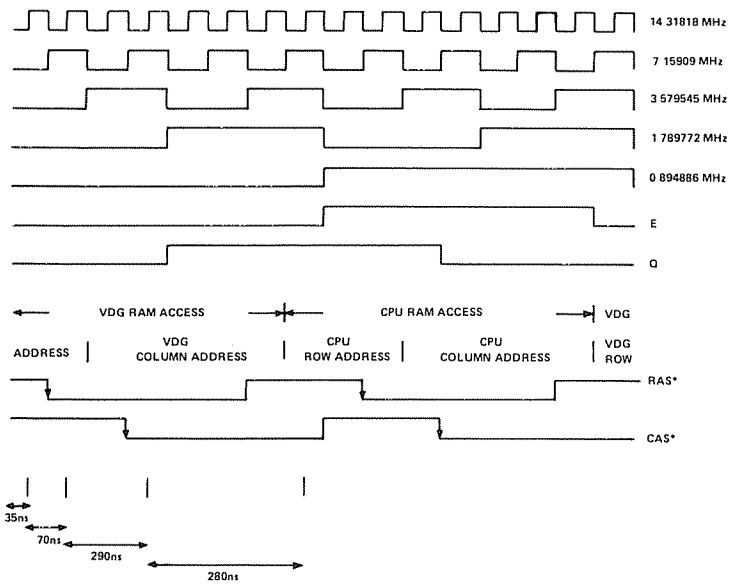


FIGURE 6. COLOR COMPUTER TIMING DIAGRAM

ROM

The Read Only Memories used in the Color Computer are simple digital devices requiring only data lines, address lines, and a chip select line. The chip select line turns on the ROM for operation. Then, one of 8,192 memory locations is accessed by the thirteen address lines. The eight data bits of stored information are then available at the data bus outputs for the CPU.

In the Color Computer, one or two 8K ROM's are used for the BASIC Interpreter. To access these ROM's, the decoding circuitry produces two chip select lines. The main BASIC ROM (U3) is located at the Hexidecimal address AØØØ-BFFF. The Expansion ROM (U28) is located at the address 8ØØØ-9FFF.

VIDEO INTERFACE

The primary portion of the video interface is shown on sheet 2 of the schematic diagram. The clock source for the video interface is the VDG CLK signal from the MC6883 chip (U1Ø). This clock must be exactly 3.579545 MHz to generate a color signal for a TV. To operate properly, the VDG chip (U7) must be set to the correct mode by the control lines coming from PIA (U4). The VDG will then generate a display based on the data present on the input lines.

In the Color Computer, the memory address lines for the video display are supplied by the MC6883 chip (U1Ø). To maintain synchronization with the VDG (U7), the horizontal sync signal and the LSB of the VDG address lines are connected to the MC6883 chip. In addition, the field sync signal is connected to the tri-state control of the VDG causing the address lines to enter a tri-state condition during vertical blanking. In total, thirteen video address lines are supplied to the RAM to support the maximum display size of 6K. The starting address of the display memory is located in the upper left corner of the display screen. As the television sweeps from left to right and top to bottom, the video address lines are incremented to produce the display.

The eight data input lines to the VDG are supplied by an octal latch. This latch is necessary to hold the output data for 16K RAM chips which have an unlatched output. In reality, this data is simply the contents of a portion of dynamic RAM.

The other VDG input lines used by the Color Computer are listed below.

MODE CONTROL A*/G – selects between alpha-semigraphics and full graphic modes.

MODE CONTROL A*/S – selects between alphanumerics and semigraphics. This line is connected to data bit 7.

MODE CONTROL INT*/EXT – used to select the semigraphic – 6 mode. This line is connected to the same PIA bit as GMØ.

MODE CONTROL INV – selects between a black character on a green background or a green character on a black background. This line is connected to data bit 6.

MODE CONTROL GMØ, GM1, & GM2 – these three lines are used to select one of eight full graphic modes.

CLOCK (CLK) – The VDG clock input (CLK) requires a 3.579545 MHz (standard) TV crystal frequency square wave.

THREE-STATE CONTROL – (MS*) is a TTL compatible input which, when low, forces the VDG address lines into a high impedance state.

The following output signals are used by the Color Computer.

LUMINANCE (Y) – this six level analog output contains composite sync, blanking, and four levels of video luminance.

ØA – This three level analog output is used in combination with ØB and Y outputs to specify one of eight colors.

ØB – This four level analog output is used in combination with ØA and Y outputs to specify one of eight colors. Additionally, one analog level is used to specify the time of the color burst reference signal.

CHROMA BIAS (CHB) – This pin is an analog output and provides a DC reference corresponding to the quiescent value of ØA and ØB. CHB is used to guarantee good thermal tracking and minimize the variation between the parts.

FIELD SYNC – (FS*) – The high to low transition of the FS* output coincides with the end of active display area. The low to high transition of FS* coincides with the trailing edge of the vertical synchronization pulse.

HORIZONTAL SYNC – (HS*) – The HS* pulse is synchronous with the horizontal synchronization pulse furnished to the television receiver by the VDG. The high to low transition of the HS* output coincides with the leading edge of the horizontal synchronization pulse.

Together, the VDG (U7) and the MC6883 (U1Ø) are capable of generating a large number of distinct display modes. Of this large quantity, fourteen separate Modes will be described. These include an alphanumeric, five semigraphic, and eight full graphic modes.

ALPHANUMERIC DISPLAY MODES – All alphanumeric modes occupy an 8 x 12 dot character matrix box and there are 32 x 16 character boxes per TV frame. Each horizontal dot (dot-clock) corresponds to one half the period duration of the 3.58 MHz clock and each vertical dot is one scan line. One of two colors for the lighted dots may be selected by the color set select pin (pin 39). An internal ROM will generate 64 ASCII display characters in a standard 5 x 7 box. Six bits of the eight-bit data word are used for the ASCII character generator and the two bits not used are used to implement inverse video and mode switching to semigraphics –4, –8, –12, or –24.

The ALPHA SEMIGraphics –4 mode translates bits Ø through 3 into a 4 x 6 dot element in the standard 8 x 12 dot box. Three data bits may be used to select one of eight colors for the entire character box. The extra bit is used to switch to alphanumeric. A 512 byte display memory is required. A density of 64 x 32 elements is available in the display area. The element area is four dot-clocks wide by six lines high.

The ALPHA SEMIGraphics –6 mode maps six 4 x 4 dot elements into the standard 8 x 12 dot alphanumeric box, a screen density of 64 x 48 elements is available. Six bits are used to generate this map and two data bits may be used to select one of four colors in the display box. A 512 byte display memory is required. The element area is four dot-clocks wide by four lines high.

The ALPHA SEMIGraphics – 8 mode maps eight 4 x 3 dot elements into the standard 8 x 12 dot box. This mode requires four memory locations per box and each memory location may specify one of eight colors or black. A 2048 byte display memory is required. A density of 64 x 64 elements is available in the display area. The element area is four dot-clocks wide by three lines high.

The ALPHA SEMIGraphics –12 mode maps twelve 4 x 2 dot elements into the standard 8 x 12 dot box. This mode requires six memory locations per box and each memory location may specify one of eight colors or black. A 3072 byte display memory is required. A density of 64 x 96 elements is available in the display area. The element area is four dot-clocks wide by two lines high.

The ALPHA SEMIGraphics –24 mode maps twenty-four 4 x 1 dot elements into the standard 8 x 12 dot box. This mode requires twelve memory locations per box and each memory location may specify one of eight colors or black. A 6144 byte display memory is required. A density of 64 x 192 elements is available in the display are. The element area is four dot-clocks wide by one line high.

FULL GRAPHIC MODES – There are eight full graphic modes available from the VDG. These modes require 1K to 6K bytes of memory. The eight full-graphic modes include an outside color border in one of two colors depending upon the color set select pin (CSS). The CSS pin (pin 39) selects one of two sets of four colors in the four color graphic modes.

The 64 x 64 Color Graphics mode generates a display matrix of 64 elements wide by 64 elements high. Each element may be one of four colors. A 1K x 8 display memory is required. Each pixel equals four dot-clocks by three scan lines.

The 128 x 64 Graphics Mode generates a matrix 128 elements wide by 64 elements high. Each element may be either ON or OFF. However, the entire display may be one of two colors, selected by using the color set select pin. A 1K x 8 display memory is required. Each pixel equals two dot-clocks by three scan lines.

The 128 x 64 Color Graphics mode generates a display matrix 128 elements wide by 64 elements high. Each element may be one of four colors. A 2K x 8 display memory is required. Each pixel equals two dot-clocks by three scan lines.

The 128 x 96 Graphics mode generates a display matrix 128 elements wide by 96 elements high. Each element may be either ON or OFF. However, the entire display may be one of two colors selected by using the color select pin. A 2K x 8 display memory is required. Each pixel equals two dot-clocks by two scan lines.

The 128 x 96 Color Graphics mode generates a display 128 elements wide by 96 elements high. Each element may be one of four colors. A 3K x 8 display memory is required. Each pixel equals two dot-clocks by two scan lines.

The 128 x 192 Graphics mode generates a display matrix 128 elements wide by 192 elements high. Each element may be either ON or OFF, but the ON elements may be one of two colors selected with color set select pin. A 3K x 8 display memory is required. Each pixel equals two dot-clocks by one scan line.

The 128 x 192 Color Graphics mode generates a display 128 elements wide by 192 elements high. Each element may be one of four colors. A 6K x 8 display memory is required. A detailed description of the VDG modes is given in Table 2. Each pixel equals two dot-clocks by one scan line.

The 256 x 192 Graphics mode generates a display 256 elements wide by 192 elements high. Each element may be either ON or OFF, but the ON element may be one of two colors selected with the color set select pin. A 6K x 8 display memory is required. Each pixel equals one dot-clock by one scan line.

The following tables present mode programming information, a detailed description of the display modes, and the display character set.

TABLE 1. MODE SELECTION

MC6883 DISPLAY MODE REGISTERS			PIA REGISTER BITS HEX ADDRESS (FF22)								DATA BITS		ALPHA/GRAPHIC MODE SELECTED
V_2	V_1	$V_\emptyset$	7	6	5	4	3	2	1	Ø	7	6	
Ø	Ø	Ø	Ø	X	X	Ø	CSS	N	N	N	Ø	Ø	Alphanumerics
Ø	Ø	Ø	Ø	X	X	Ø	CSS	N	N	N	Ø	1	Alphanumerics Inverted
Ø	Ø	Ø	Ø	X	X	Ø	X	N	N	N	1	X	Semigraphics - 4
Ø	Ø	Ø	Ø	X	X	1	CSS	N	N	N	1	X	Semigraphics - 6
Ø	1	Ø	Ø	X	X	Ø	X	N	N	N	1	X	Semigraphics - 8
1	Ø	Ø	Ø	X	X	Ø	X	N	N	N	1	X	Semigraphics - 12
1	1	Ø	Ø	X	X	Ø	X	N	N	N	1	X	Semigraphics - 24
Ø	Ø	1	1	Ø	Ø	Ø	CSS	N	N	N	X	X	64 x 64 Color Graphics
Ø	Ø	1	1	Ø	Ø	1	CSS	N	N	N	X	X	128 x 64 Graphics
Ø	1	Ø	1	Ø	1	Ø	CSS	N	N	N	X	X	128 x 64 Color Graphics
Ø	1	1	1	Ø	1	1	CSS	N	N	N	X	X	128 x 96 Graphics
1	Ø	Ø	1	1	Ø	Ø	CSS	N	N	N	X	X	128 x 96 Color Graphics
1	Ø	1	1	1	Ø	1	CSS	N	N	N	X	X	128 x 192 Graphics
1	1	Ø	1	1	1	Ø	CSS	N	N	N	X	X	128 x 192 Color Graphics
1	1	Ø	1	1	1	1	CSS	N	N	N	X	X	256 x 192 Graphics

X = DON'T CARE
N = DO NOT CHANGE

TABLE 2. DETAILED DESCRIPTION OF DISPLAY MODES

VDG PINS		COLOR			TV SCREEN		VDG DATA BUS	COMMENTS
CSS	INV	Character Color	Background	Border	Display Mode	Detail		
0	0	Green	Black	Black	32 Characters in columns	8 dots × 12 dots (7 × 5)	0 INV ASCII code	The ALPHANUMERIC INTERNAL mode uses an internal character generator which contains the following five dot by seven dot characters: @ A B C D E F G H I J K L M N O P Q R S T U V W X Y Z [/] ↑ ← SP ! " # $ % & * + , = / 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
	1	Black	Green					
1	0	Orange	Black	Black	16 Characters in rows			
	1	Black	Orange					
X	X	Lx C2 C1 C0 Color 0 X X X Black 1 0 0 0 Green 1 0 0 1 Yellow 1 0 1 0 Blue 1 0 1 1 Red 1 1 0 0 Buff 1 1 0 1 Cyan 1 1 1 0 Magenta 1 1 1 1 Orange		Black	64 Display elements in columns 32 Display elements in rows	L_3 L_2 / L_1 L_0 one element	1 C_2 C_1 C_0 L_3 L_2 L_1 L_0	The SEMIGRAPHICS FOUR mode uses an internal "coarse graphics" generator in which a rectangle (eight dots by twelve dots) is divided into four equal parts. The luminance of each part is determined by a corresponding bit on the VDG data bus. The color of illuminated parts is determined by three bits. It requires 512 bytes of display memory.
0	X	Lx C1 C0 Color 0 X X Black 1 0 0 Green 1 0 1 Green 1 1 0 Blue 1 1 1 Red		Black	64 Display elements in columns	L_5 L_4 / L_3 L_2 / L_1 L_0	C_1 C_0 L_5 L_4 L_3 L_2 L_1 L_0	The SEMIGRAPHIC SIX mode is similar to the SEMIGRAPHIC FOUR mode with the following difference: The eight dot by twelve dot rectangle is divided into six equal parts. Color is determined by the two remaining bits. It requires 512 bytes of display memory.
1		0 X X Black 1 0 0 Buff 1 0 1 Buff 1 1 0 Magenta 1 1 1 Orange			48 Display elements in rows			
X	X	Lx C2 C1 C0 Color 0 X X X Black 1 0 0 0 Green 1 0 0 1 Yellow 1 0 1 0 Blue 1 0 1 1 Red 1 1 0 0 Buff 1 1 0 1 Cyan 1 1 1 0 Magenta 1 1 1 1 Orange		Black	64 Display elements in columns 64 Display elements in rows	L_1 L_0 / L_3 L_2 / L_5 L_4 / L_7 L_6	1 C_2 C_1 C_0 L_1 L_0 X X 1 C_1 C_1 C_0 L_3 L_2 X X 1 C_2 C_1 C_0 X X L_5 L_4 1 C_2 C_1 C_0 X X L_7 L_6	The SEMIGRAPHIC EIGHT mode requires four column consecutive addresses*, and produces a 2 x 4 block. It requires 2048 bytes of display memory.
X	X	Lx C2 C1 C0 Color 0 X X X Black 1 0 0 0 Green 1 0 0 1 Yellow 1 0 1 0 Blue 1 0 1 1 Red 1 1 0 0 Buff 1 1 0 1 Cyan 1 1 1 0 Magenta 1 1 1 1 Orange		Black	64 Display elements in columns 96 Display elements in rows	L_1 L_0 / L_3 L_2 / L_5 L_4 / L_7 L_6 / L_9 L_8 / L_{11} L_{10}	1 C_2 C_1 C_2 L_1 L_0 X X 1 C_2 C_1 C_0 L_3 L_2 X X 1 C_2 C_1 C_0 L_5 L_4 X X 1 C_2 C_1 C_0 X X L_7 L_6 1 C_2 C_1 C_0 X X L_9 L_8 1 C_2 C_1 C_0 X X L_{11} L_{10}	The SEMIGRAPHIC TWELVE mode requires six column consecutive addresses*, and produces a 2 x 6 block. It requires 3072 bytes of display memory.

*Four column consecutive addresses starting at HEX 0400 are 0400, 0420, 0440, 0460.

TABLE 2. DETAILED DESCRIPTION OF DISPLAY MODES CONT.

VDG PINS		COLOR			TV SCREEN		VDG DATA BUS	COMMENTS
CSS	INV	Character Color	Background	Border	Display Mode	Detail		
X	X	Lx C2 C1 C0 Color Ø X X X Black 1 Ø Ø Ø Green 1 Ø Ø 1 Yellow 1 Ø 1 Ø Blue 1 Ø 1 1 Red 1 1 Ø Ø Buff 1 1 Ø 1 Cyan 1 1 1 Ø Magenta 1 1 1 1 Orange		Black	64 Display elements in columns 192 Display elements in rows	L_1 L_0 L_3 L_2 L_5 L_4 L_7 L_6 L_9 L_8 L_{11} L_{10} L_{13} L_{12} L_{15} L_{14} L_{17} L_{16} L_{19} L_{18} L_{21} L_{20} L_{23} L_{22}	1 C_2 C_1 C_0 L_1 L_0 X X 1 C_2 C_1 C_0 L_3 L_2 X X 1 C_2 C_1 C_0 L_5 L_4 X X 1 C_2 C_1 C_0 L_7 L_6 X X 1 C_2 C_1 C_0 L_9 L_8 X X 1 C_2 C_1 C_0 L_{11} L_{10} X X 1 C_2 C_1 C_0 X X L_{13} L_{12} 1 C_2 C_1 C_0 X X L_{15} L_{14} 1 C_2 C_1 C_0 X X L_{17} L_{16} 1 C_2 C_1 C_0 X X L_{19} L_{18} 1 C_2 C_1 C_0 X X L_{21} L_{20} 1 C_2 C_1 C_0 X X L_{23} L_{22}	The SEMIGRAPHIC TWENTY FOUR mode requires twelve column consecutive addresses*, and produces a 2 x 12 block. It requires 6144 bytes of display memory.
Ø	X	C1 C0 Color Ø Ø Green Ø 1 Yellow 1 Ø Blue 1 1 Red		Green	64 Display elements in columns	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS ONE C mode uses a maximum of 1024 bytes of display RAM in which one pair of bits specifies one picture element.
1		Ø Ø Buff Ø 1 Cyan 1 Ø Magenta 1 1 Orange		Buff	64 Display elements in rows			
Ø	X	Lx Color Ø Black 1 Green		Green	128 Display elements in columns	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS ONE R mode uses a maximum of 1024 bytes of display RAM in which one bit specifies one picture element.
1		Ø Black 1 Buff		Buff	64 Display elements in rows			
Ø	X	Same colors as Graphics one C		Green	128 Display elements in columns	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS TWO C mode uses a maximum of 2048 bytes of display RAM in which one pair of bits specifies one picture element.
1				Buff	64 Display elements in rows			
Ø	X	Same colors as Graphics one R		Green	128 Display elements in columns	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS TWO R mode uses a maximum of 1536 bytes of display RAM in which one bit specifies one picture element.
1				Buff	96 Display elements in rows			
Ø	X	Same colors as Graphics one C		Green	128 Display elements in columns	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS THREE C mode uses a maximum of 3072 bytes of display RAM in which one pair of bits specifies one picture element.
1				Buff	96 Display elements in rows			
Ø	X	Same colors as Graphics one R		Green	128 Display elements in columns	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS THREE R mode uses a maximum of 3072 bytes of display RAM in which one bit specifies one picture element.
1				Buff	192 Display elements in rows			
Ø	X	Same colors as Graphics one C		Green	128 Display elements in columns	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS SIX C mode uses a maximum of 6144 bytes of display RAM in which one pair of bits specifies one picture element.
1				Buff	192 Display elements in rows			
Ø	X	Same colors as Graphics one R		Green	256 Display elements in columns	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS SIX R mode uses a maximum of 6144 bytes of display RAM in which one bit specifies one picture element.
1				Buff	192 Display elements in rows			

*Four column consecutive addresses starting at HEX Ø4ØØ are Ø4ØØ, Ø42Ø, Ø44Ø, Ø46Ø.

TABLE 3. DISPLAY CHARACTER SET

HEX VALUE		CHARACTER	HEX VALUE		CHARACTER
Non-Inverted	Inverted		Non-Inverted	Inverted	
00	40	@	18	58	X
01	41	A	19	59	Y
02	42	B	1A	5A	Z
03	43	C	1B	5B	[
04	44	D	1C	5C	\
05	45	E	1D	5D	]
06	46	F	1E	5E	↑
07	47	G	1F	5F	←
08	48	H	20	60	
09	49	I	21	61	!
0A	4A	J	22	62	"
0B	4B	K	23	63	#
0C	4C	L	24	64	$
0D	4D	M	25	65	%
0E	4E	N	26	66	&
0F	4F	O	27	67	'
10	50	P	28	68	(
11	51	Q	29	69	)
12	52	R	2A	6A	*
13	53	S	2B	6B	+
14	54	T	2C	6C	,
15	55	U	2D	6D	-
16	56	V	2E	6E	.
17	57	W	2F	6F	/

HEX VALUE		CHARACTER
Non-Inverted	Inverted	
30	70	0
31	71	1
32	72	2
33	73	3
34	74	4
35	75	5
36	76	6
37	77	7
38	78	8
39	79	9
3A	7A	:
3B	7B	;
3C	7C	<
3D	7D	>
3E	7E	=
3F	7F	?

At pin 28 of the VDG, the Y signal contains composite video and sync information. An example of this type of video signal is shown in Figure 7. This signal together with three color signals, CHB (pin 9), ØA (pin 11), and ØB (pin 1Ø) is connected to the MC1372 color mixer chip (U12).

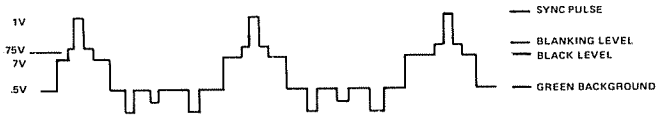


FIGURE 7. VDG VIDEO OUTPUT

The MC1372 is a complete Color TV video modulator chip. However, for the Color Computer it is used only as a color mixer chip. Figure 8 shows a block diagram of the MC1372 chip. Pins 1 and 2 of the MC1372 form an oscillator circuit, but this is not needed in the Color Computer. The reference clock frequency of exactly 3.579545 MHz is produced by the MC6883 chip (U1Ø). This signal is then rounded off by R17 and C53 before being connected to pin 2 of the MC1372 (U12). Pin 1 is left unconnected. Also, the duty cycle adjust input (pin 3) is left unconnected since a 5Ø% duty cycle signal is produced by the MC6883.

The RF oscillator portion of the MC1372 is not required, so diode CR8 and resistor R2Ø are used to kill the oscillation. Also the orientation of CR8 controls the generation of normal or inverted video.

Using the color signals from the VDG, U12 produces the chroma output at pin 8. This signal consists of the reference color burst and the video color information. The MC1372 requires this signal to be AC coupled to pin 1Ø. This is accomplished by capacitor C42. Resistor R18 determines the Luminance to Chrominance ratio.

The complete color video signal is available at pin 12 of the MC1372. However, at this point the signal has no drive capability and must be amplified before it can drive the modulator. This amplification is accomplished by Q1 and the associated circuitry. The video amplifier is powered by 8 volts DC. This power supply is produced off of the +12V supply by zener diode CR16, (a 3.9 volt zener diode). R69 is used to stabilize the zener voltage while C12 and C25 filter the voltage. This 8V supply is then connected to the collector of the transistor (Q1), and through a 3.9K pullup to the video output pin of the MC1372 (pin 12).

The video amplifier is a common collector amplifier designed to provide current gain. R19 and R8 form a voltage divider for the video input signal. R9 and R21 are used to modify the voltage divider to compensate for variations in the output voltage of the MC1372. R46 is a bootstrap resistor used to provide as much current gain from the amplifier as possible. R47 is a biasing resistor for the amplifier.

The video output from the emitter of Q1 is connected directly to pin 1 of the UM1285-8 modulator (U5). This signal should be adjusted with R21 so that the blanking level is exactly 2.35V. A sample of this video signal is shown in Figure 9.

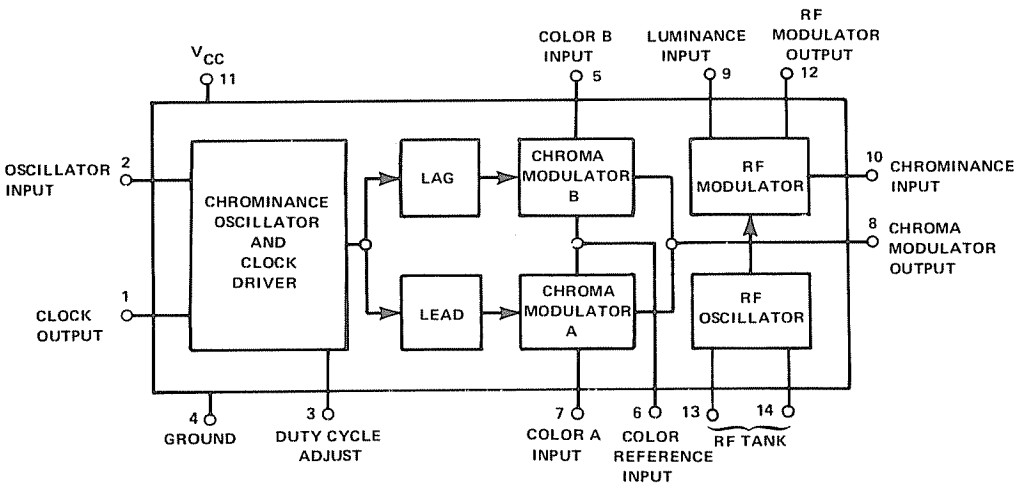


FIGURE 8. MC1372 BLOCK DIAGRAM

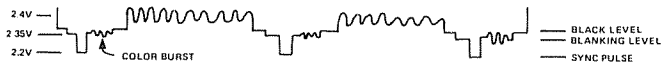


FIGURE 9. VIDEO INPUT TO THE MODULATOR

The UM1285-8 modulator is a high performance intercarrier vestigial sideband unit. The modulator is powered off the 12-volt supply with an inline current limiting resistor, R45. The modulator also has sound capability which is used by the Color Computer. The last input to the modulator is the channel select switch (S3). Channel 4 is selected by allowing the input to float high. Channel 3 is selected by ground.

Internal to the modulator, the DC sound input signal is converted to a 4.5 MHz frequency modulated signal. This signal is then mixed with the video and used to modulate the RF signal for the selected channel (61.25 MHz for Channel 3 or 67.25 MHz for channel 4). This final output is available at the phone jack connector of the modulator.

PIA's

The Color Computer uses two peripheral interface adapters (PIA's). These devices provide a universal interface to the 68Ø9E CPU chip, and they support all of the I/O functions in the Color Computer.

The functional configuration of the PIA is programmed by the CPU during the reset routine. Each of the peripheral data lines may be programmed to act as an input or output, and each of four control/interrupt lines may be programmed for one of several control modes. Figure 1Ø shows a block diagram of a PIA.

As shown in the block diagram, a PIA consists of two 8-bit data registers and 4 control/interrupt lines. The two 8-bit data registers are controlled by two data direction registers. These direction control registers are set up by the reset routine and normally will not be changed.

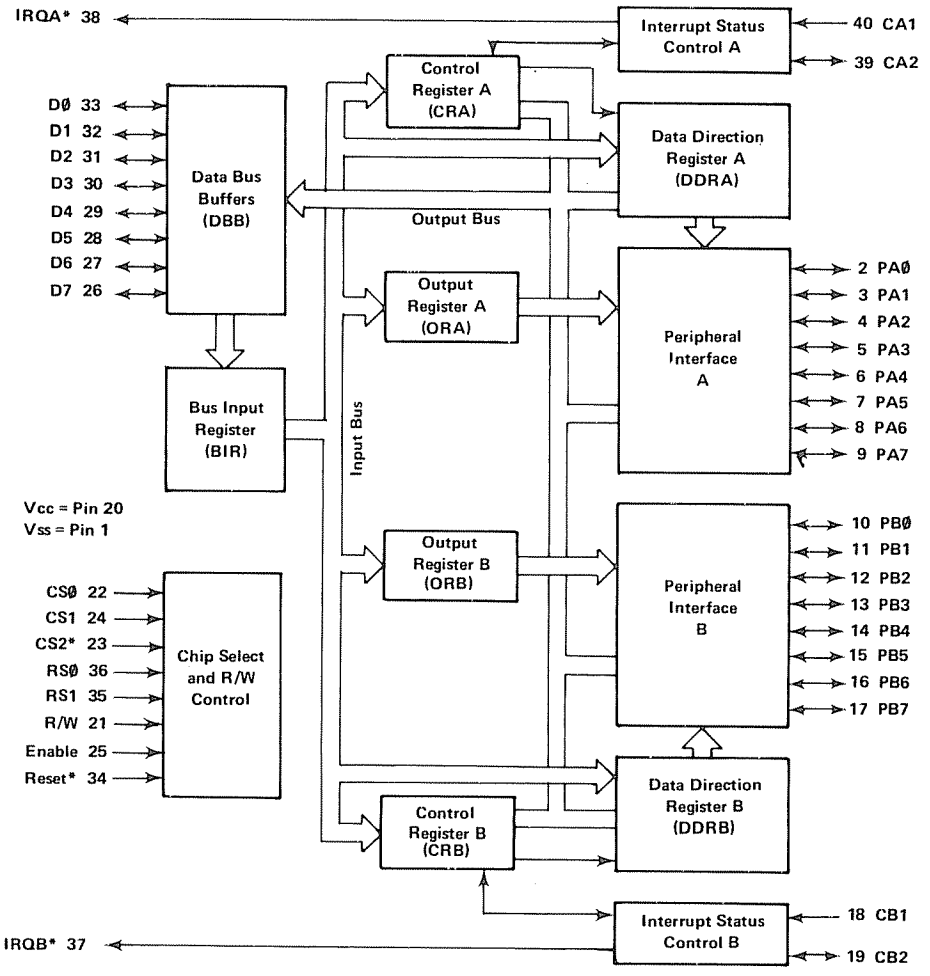


FIGURE 10. PIA BLOCK DIAGRAM

The four control/interrupt lines are controlled by the two control registers. The control registers also handle device selection within the PIA. Two of the four lines function only as interrupt inputs, and the other two lines may be used as interrupt inputs or outputs.

PIA U8 is used mainly for the keyboard. Data register B (pins 10-17) is programmed as an output, and is used to strobe the keyboard columns. The first seven lines of data register A (pins 2-8) are programmed as inputs and are used to read the keyboard rows. Pins 2 and 3 are also used as fire button inputs for the joysticks.

The other pins of PIA U8 serve various functions. Data register A (pin 9) is programmed as an input for the joystick interface. CA2 and CB2 (pins 19 and 39) are used as outputs. These two lines select one of four joystick or sound inputs. The last two pins of PIA U8, CA1 (pin 40) and CB1 (pin 18), are used as interrupt inputs. They are both tied to video clock outputs from the VDG (U7). If enabled, CA1 provides an interrupt after each video line. CB1, if enabled, provides an interrupt after each screen of data (60 Hz).

PIA U4 is used for several different functions. Pins 4-9 of data register A are used for the 6-bit digital to analog converter. Pin 3 of register A is the signal RS232OUT. This signal is used to drive the printer and other devices. Pin 2 of register A is the input for data from the cassette. Pins 13-17 of data register B are used to control the selection of the various alphanumeric and graphic modes of the VDG. Pin 12 of register B is an input for the memory size jumper. Pin 11 of register B is the single bit sound output. Pin 10 is the RS232IN signal input pin.

The control and interrupt pins of PIA U4 also serve various functions. CA1 (pin 40) is the input for the signal CD (a status interrupt input for the RS232C interface). CA2 is an output used to control the cassette motor. CB1 is the cartridge interrupt input. Whenever a cartridge is inserted in the computer, this input will interrupt BASIC and jump to the program in the cartridge. Finally, CB2 is used as an output to enable sound from the analog multiplexer (U9).

Digital to Analog (D/A)

A commonly used input/output (I/O) device in the Color Computer is the 6-bit digital to analog converter (D/A). This device is addressed as the six MSB's of Hexidecimal address FF20. It allows the 6-bit digital word to be converted to an analog voltage level between 0.25 volts and 4.75 volts.

The converter is composed of a CMOS buffer (U2) and six discrete resistors. The converter operates by acting as a simple voltage divider. That is, the high outputs represent +5 volts and the low outputs, ground. The voltage is then determined by obtaining the parallel equivalent of the resistors tied high, the parallel equivalent of all the resistors (approximately 5K), and multiplying this ratio by 5 volts.

This simple picture is modified by three extra resistors (R72, R41, and R42). R72 is a 100K resistor connected to +5 volts, and the series equivalent of R41 and R42 forms a 100K resistor connected to ground. The effect of these resistors is to limit the minimum voltage to +0.25 volts and the maximum voltage to +4.75 volts. Also, C52 is included to filter the output voltage. For simplicity, the approximate output voltage may be calculated by the following formula:

$$\text{VOLTAGE} = (N \times 0.0715) + 0.25$$

N = the 6-bit value (0-63)

JOYSTICK INTERFACE

One important usage of the D/A converter is with the joystick interface circuitry. This interface uses an analog multiplexer to select one of the four input joystick values. These values range between 0 and 5 volts. From the output of the multiplexer, the signal is directed to a comparator, which is also connected to the D/A converter. Then by a method of software successive approximation the joystick value may be determined to the 6-bit accuracy of the D/A converter.

Also provided in the joystick are two fire switches (momentary contact switches). One side of each switch is connected to ground, and the other side is connected to a PIA input. These two PIA inputs are also shared by rows 1 and 2 of the keyboard, so a conflict may exist if both are used at once. The PIA inputs are normally high so it is a simple software function to read the fire switches.

SOUND OUTPUT

Another important usage of the D/A converter is the sound output. This D/A converter is the primary source of sound effects for the computer, however three other sound sources are provided. These extra sound sources are a single bit sound source, sound from the cassette tape recorder, and sound from the cartridge.

The D/A output is connected directly to the MC14529B analog multiplexer (U9). This chip is used to select one of three sound sources, and maybe disabled to allow use of the fourth single bit sound source. Table 4 shows the selection of the various sound sources. Figure 11 shows all of the circuitry for sound generation.

The cassette sound output must be modified before being connected to the analog multiplexer. For this purpose, a 10μf non-polarized capacitor (C2) is used to level shift the signal. Also, two 4.7K resistors (R31 and R32) assign a DC level of 2.5 volts and limit the signal to Ø to 5 volts. This signal is then connected to the multiplexer (U9).

The output of the analog multiplexer is connected to pin 3 of the modulator (U5), and to the single bit sound source (pin 11, U4), which is isolated by a 1ØK resistor. At any time, only one of the two sources should be used, to avoid mixing the two sources.

TABLE 4. SOUND SELECTION

SNDEN U9-15	SEL 1 U9-6	SEL 2 U9-7	SOUND SOURCE SELECTED
1	Ø	Ø	6 BIT DIA
1	1	Ø	CASSETTE
1	Ø	1	CARTRIDGE
1	1	1	NOT USED
Ø*	X	X	SINGLE BIT SOUND

*NOTE: For single bit sound, PIA U4 pin 11 must be programmed as an output. It is normally programmed as an input.

X = DON'T CARE
Ø = LOGIC LOW
1 = LOGIC HIGH

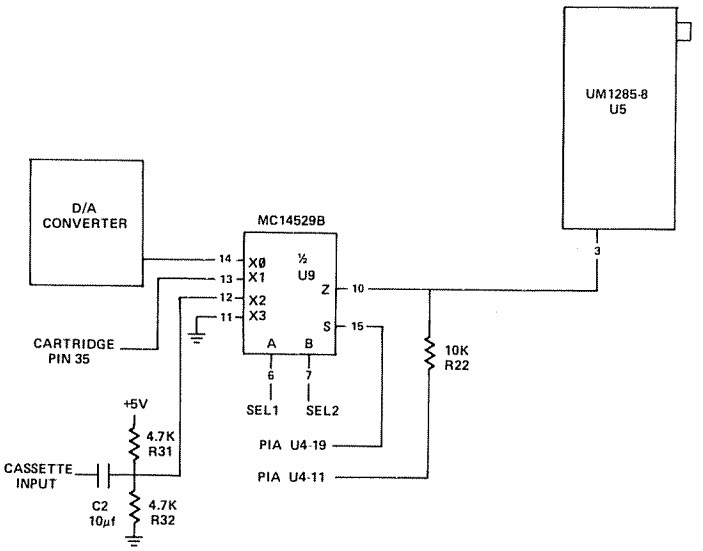


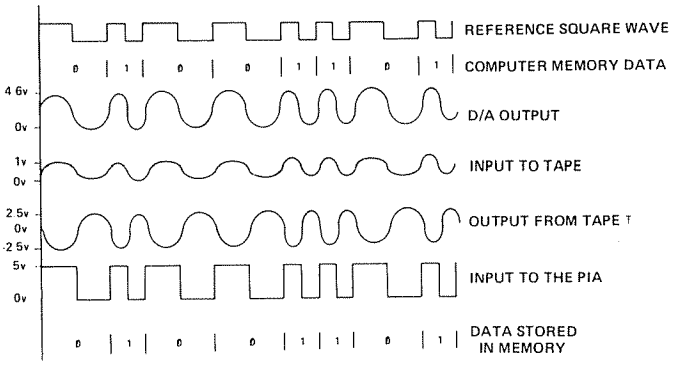
FIGURE 11. SOUND CIRCUITRY

CASSETTE INTERFACE

The cassette interface is composed of an output attenuator connected to the 6-bit D/A, a motor control circuit, and an input zero crossing detector. However, most of the important cassette parameters are controlled by software.

The cassette format chosen uses a sinewave of 2400 or 1200 Hertz to yield a Baud rate of approximately 1500 Baud. In this format, a Ø (or logic low) is represented by one cycle of 1200 Hertz, and a 1 (or logic high) is represented by one cycle of 2400 Hertz. A sample of data is shown in Figure 12. A typical program tape would consist of a leader of alternating 1's and Ø's, followed by one or more blocks of data. A block of data is composed of Ø to 255 bytes of data with a checksum, sync byte, and the block length.

The output circuit utilizes the 6-bit D/A to generate a sinewave of 1200 or 2400 Baud. This signal is then attenuated to approximately 1 volt and connected to the auxiliary input of the cassette recorder.



† This is shown inverted to indicate possible phase inversion by the tape recorder

FIGURE 12. SAMPLE DATA OF CASSETTE FORMAT

The motor control circuit is controlled by an output PIA pin. This signal is used to switch transistor Q4. Q4 provides sufficient current capability to drive the relay coil. Diode CR7 is used to shunt voltage surges whenever Q4 is switched. Diodes CR9 and CR1Ø perform a similar function for the relay switch contacts. Whenever the relay contacts are opened or closed, a high voltage spike could occur. However, diodes CR9 and CR1Ø will shunt away any high voltage. C8Ø is provided to prevent RF noise associated with contact switching.

The input circuit is a zero crossing detector. R33 is a termination resistor for the cassette output. Resistors R37 and R38 are used to bias one input of the comparator at 1 volt. The other input is also biased at 1 volt by R36 and the series combination of R35 and R34. If the AC input from the recorder goes negative, diode CR4 turns on and sets the input to the comparator equal to 1/2 volt. Since the other input is biased at 1 volt, the comparator output is switched to the high state. If the AC input from the recorder is positive, diode CR4 is turned off and the input to the comparator will be at some point greater than 1 volt, in which case, the comparator output will be low.

The comparator output is open-collector, so pull-up resistor R40 is provided to generate a TTL signal. R39 is used to prevent oscillation of the comparator. The final portion of the cassette circuit is capacitor C81, which is used to isolate RF noise from the cassette cable.

DETAILED TAPE FORMAT INFORMATION

The standard TRS-80 Color Computer tape is composed of the following items:

1. A leader consisting of 128 bytes of Hex 55
2. A Namefile block
3. A blank section of tape approximately equal to 0.5 seconds in length; this allows BASIC time to evaluate the Namefile.
4. A second leader of 128 bytes of Hex 55
5. One or more Data blocks
6. An End of File block

The block format for Data blocks, Namefile blocks, or an End of File block is as follows:

1. One leader byte — 55H
2. One sync byte — 3CH
3. One block type byte — 01H = Data FFH = End of File ØØH = Namefile
4. One block length byte — ØØH to FFH
5. Data — Ø to 255 bytes
6. One checksum byte — the sum of all the data plus block type and block length
7. One leader byte — 55H

The End of File block is a standard block with a length of Ø and the block type equal to FFH.

The Namefile block is a standard block with a length of 15 bytes (ØFH) and the block type equals ØØH. The 15 bytes of data provide information to BASIC and are employed as described below:

1. Eight bytes for the program name
2. One file type byte — ØØH = BASIC Ø1H = Data Ø2H = Machine Language
3. One ASCII flag byte — ØØH = Binary FFH = ASCII
4. One Gap flag byte — Ø1H = Continuous FFH = Gaps
5. Two bytes for the start address of a machine language program
6. Two bytes for the load address of a machine language program

RS232C INTERFACE

The RS232C Interface utilizes a 4-pin DIN connector (P2). This interface allows the computer to have serial communication with printers, modems, or other computers. The four signals used by the interface are:

1. CD – a status input line
2. RS232IN – serial data input
3. GROUND – zero voltage reference
4. RS232OUT – serial data out

The pinout for the DIN connector is shown in Figure 13.

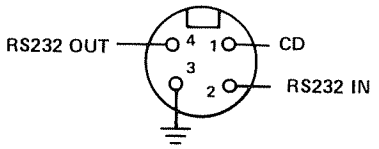


FIGURE 13. RS-232C CONNECTOR PIN-OUT

In general, an RS232C signal is defined as a high (or logic 1) if the voltage is greater than +3 volts. It is defined as a low (or logic Ø) if the voltage is less than –3 volts. The range of –3 volts to +3 volts is undefined.

The RS232C interface circuitry is shown on sheet 2 of the schematic, upper right corner. For the signal RS232OUT, an output pin of PIA U4 (pin 3) is tied to a 741C Op-amp (U15). The Op-amp is referenced at 1.4 volts by resistors R23 and R24. This reference causes the Op-amp to swing between the two power supply voltages (+/–12 volts) as the TTL input switches states. A 1ØØ ohm resistor (R27) is included to provide a current limit on the output.

The two input signals (RS232IN and CD) utilize identical circuits. RS232IN (pin 2, U14) is tied to input pin 1Ø of PIA U4, and CD (pin 1, U14) is tied to pin interrupt input 4Ø of PIA U4. The inputs from the external device are connected to the positive side of a diode. This diode blocks the application of a negative voltage to the comparator (U14). When a positive voltage is applied, the diode conducts, and the voltage is applied to the input. The comparator is referenced at 2 volts, thus if the input voltage is greater than 2.6 volts, the comparator is turned on.

The comparator output is open-collector so a pullup resistor is required for the output. Also a feedback resistor of 1ØM is used to prevent oscillation or ringing.

KEYBOARD INTERFACE

The components which make up the Keyboard Interface are shown on sheet 3 of the schematic, upper left corner. The PIA chip (U8) is the only digital circuit used. The PIA chip is a programmable interface device which functions as both an input and an output register. The eight keyboard columns are attached to the B side of the PIA. These eight lines are programmed to be outputs. The seven keyboard rows are attached to the A side of the PIA. These seven PIA lines are programmed to be inputs.

To read the keyboard, only one column is enabled by writing a zero in the bit that corresponds to that column and by writing ones in all the other bits. If a key has been pressed in that column, one of the input lines will be a zero and the key location will correspond to the bit that is low. By scanning each column in the keyboard, all of the keys may be checked.

SYSTEM POWER SUPPLY

The Color Computer requires four supply voltages: +12 volts, –12 volts, –5 volts, and +5 volts. The largest current requirement is on the +5 volt supply, therefore it is designed to provide up to 1.35 amp. The next largest requirement is 4ØØ milliamps on the +12 volt supply. The requirements for –12 and –5 volts are very minimal, so the –5 volt supply is rated at 1ØØ microamps and the –12 volt supply at 1ØØ milliamps.

The power supply is shown on sheet 3 of the schematic diagram. On the primary side of the transformer, the power supply incorporates a Ø.7 amp fuse and three high voltage capacitors. These capacitors (C2Ø, C21, and C22) provide noise immunity and isolate computer noise. The two active lines of the power cord are connected across the primary side of the power transformer. The third line (ground) is connected to the computer ground.

The transformer has two center-tapped secondary windings. One secondary is rated at 16.3 volts AC at 1 amp, and is used solely for the 5 volt supply. The other secondary is rated at 33.5 volts AC at Ø.35 amps. Both center taps are connected to ground. Each side of the 16.3 volt AC secondary is connected to a rectifier diode (CR12 and CR13). This produces a full-wave rectified signal when the two negative sides of the diodes are tied together.

All of the above circuitry is located on a secondary board inside of the Computer case. This isolates the high voltage AC signals away from the main circuit board. This transformer board is indicated on the schematic by a dashed line.

At the output of the transformer assembly, four signals are connected to the main board; ground, the input to the +5 volt regulator circuit, and the two sides of the 33.5 volt secondary. The two lines from the 33.5 volt secondary are connected to the bridge rectifier CR11.

At the output of bridge CR11, are three nearly identical regulator circuits. Each one uses a three terminal regulator chip to generate the DC supply voltages. C7 is the filter capacitor for the +12 volt supply. This is connected to U17 (a 78M12 regulator), and the + side of the bridge. CR14 provides protection for the regulator chip. C14 is the output capacitor for the +12 volt regulator. The negative side of the bridge is connected to filter capacitor C9. From C9, the −12 volt is identical to the +12 volt regulator circuit with the exception of C17. This capacitor is needed because two regulator circuits are sharing the same filter capacitor. The −5 volts regulator circuit is current limited by resistor R67. Also, due to the very low current, the protection diode and the large output capacitor have been eliminated.

Compared to the other regulator circuits, the +5 volt supply is a complex assortment of resistors, capacitors, and transistors. However, this circuit will provide a reliable 1.35 amp maximum current. The circuit begins with filter capacitor C1Ø. Connected to C1Ø is the pass transistor Q2, and its bias resistor (R59). Q2 controls the flow of current into the +5 volt line, but the actual job of regulation is performed by U13 (a 723C adjustable voltage regulator). The regulator output (pin 1Ø) is buffered by Q3. Then Q3 is used to drive the base of pass transistor Q2.

Figure 14 shows a Block diagram of the 723C regulator chip. The regulator is powered from the +12 volt supply. In operation, a 7.15 volt zener reference is available at pin 6. Resistors R6Ø, R61, and R62 then divide this reference voltage down to 5 volts, which is connected to pin 5 of the regulator. Pin 5 is the non-inverting input to internal Op-amp Zb (as shown in Figure 14). The inverting input is connected through a feed-back resistor (R63) to the +5 volt output. Op-amp Zb is then turned on or off in response to changes on the 5 volt line. C11 is the frequency compensation capacitor for Zb.

The output from Op-amp Zb controls transistor Qa, which drives the regulator output. Qa is also powered from the +12 volt supply through resistor R58. There is also a second control source on Qa, which is transistor Qb. This transistor allows a current limit to be set by resistors R65 and R64. If the current limit is exceeded, Qb will turn on and turn off Qa.

Returning briefly to pass transistor Q2, the next component is R66, which limits the output current. Overvoltage protection is provided by CR17, a 6.2V zener diode. C16 is the output filter capacitor for the +5 volt supply.

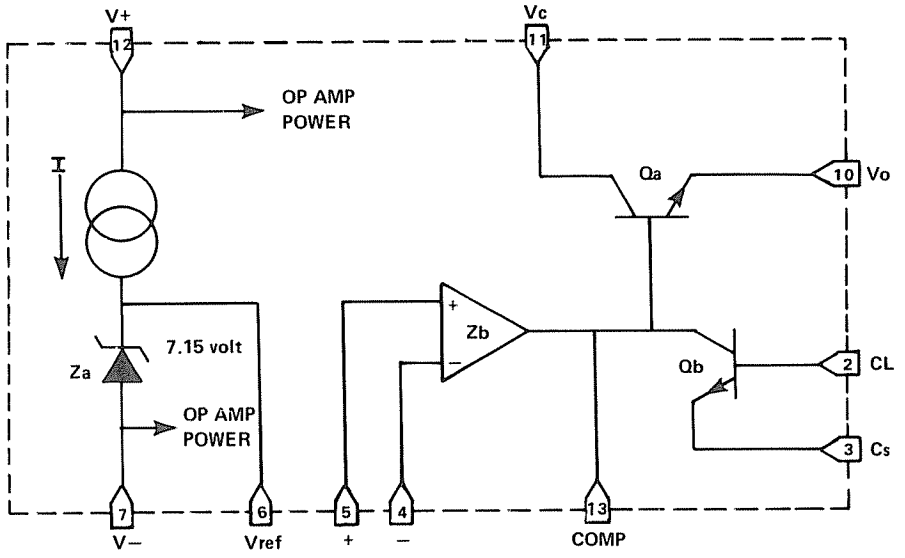


FIGURE 14. 723 REGULATOR BLOCK DIAGRAM

CARTRIDGE ROM AND OTHER DEVICES

The 40-pin cartridge connector provides the possibility of expanding the TRS-80 Color Computer in almost any manner. All of the important CPU bus signals are tied to this connector. A complete list and brief description of these signals is provided in Table 5.

The most common usage of the cartridge connector is with the ROM Cartridge. A schematic of the ROM Cartridge board is shown in Figure 15. In operation, U1 would be a 16K, 32K, or 64K ROM, and U2 might be a 16K or 32K ROM (the total of U1 and U2 must not be greater than 64K). For cartridge detection, the clock signal (Q) is shorted to the cartridge interrupt pin. This generates an interrupt anytime the cartridge is plugged in and forces the computer to jump to the program in ROM.

In addition to the expected data, address, and R/W lines, several control and special purpose signals are available on the Cartridge connector. They are described in detail as follows:

HALT* – This signal allows the data and address buses to be placed in the tri-state mode so an external processor may access RAM and ROM.

NMI* – This is the non-maskable interrupt input to the CPU.

RESET* – This is master system reset and power-up clear signal.

E & Q – These are the two clock signals for the 6809E CPU.

CART* – This is an interrupt input to one of the PIA'S. It is used to detect the presence of a Cartridge.

CTS* – This is the select signal to the Cartridge. The address space C000 (Hex) through FFEF (Hex) is selected.

SND – This signal is connected directly to the sound multiplexor, to allow a sound source in the cartridge.

SCS* – This is a spare divide select signal from U11. It selects the address space FF40 (Hex) through FF5F (Hex).

SLENB* – This signal disables the internal device selection. This allows decoded but unused sections of memory to be used by the Cartridge hardware.

TABLE 5. CARTRIDGE CONNECTOR SIGNALS

PIN #	SIGNAL NAME	DESCRIPTION
1	-12 V	-12 Volts (100 MA)
2	+12 V	+ 12 Volts (300 MA)
3	HALT*	Halt Input to the CPU
4	NMI*	Non-Maskable Interrupt to the CPU*
5	RESET*	Main Reset And Power-Up Clear Signal To The System
6	E	Main CPU Clock (Ø.89 MHz)
7	Q	Quadrative Clock Signal Which Leads E
8	CART*	Interrupt Input For Cartridge Detection
9	+5V	+5 Volts (300 MA)
10	DØ	CPU Data Bit Ø
11	D1	CPU Data Bit 1
12	D2	CPU Data Bit 2
13	D3	CPU Data Bit 3
14	D4	CPU Data Bit 4
15	D5	CPU Data Bit 5
16	D6	CPU Data Bit 6
17	D7	CPU Data Bit 7
18	R/W*	CPU Read – Write Signal
19	AØ	CPU Address Bit Ø
20	A1	CPU Address Bit 1
21	A2	CPU Address Bit 2
22	A3	CPU Address Bit 3
23	A4	CPU Address Bit 4
24	A5	CPU Address Bit 5
25	A6	CPU Address Bit 6
26	A7	CPU Address Bit 7
27	A8	CPU Address Bit 8
28	A9	CPU Address Bit 9
29	A1Ø	CPU Address Bit 1Ø
3Ø	A11	CPU Address Bit 11
31	A12	CPU Address Bit 12
32	CTS*	Cartridge Select Signal
33	GND	Signal Ground
34	GND	Signal Ground
35	SND	Sound Input
36	SCS*	Spare Select Signal
37	A13	CPU Address Bit 13
38	A14	CPU Address Bit 14
39	A15	CPU Address Bit 15
4Ø	SLENB*	Input To Disable Device Selection

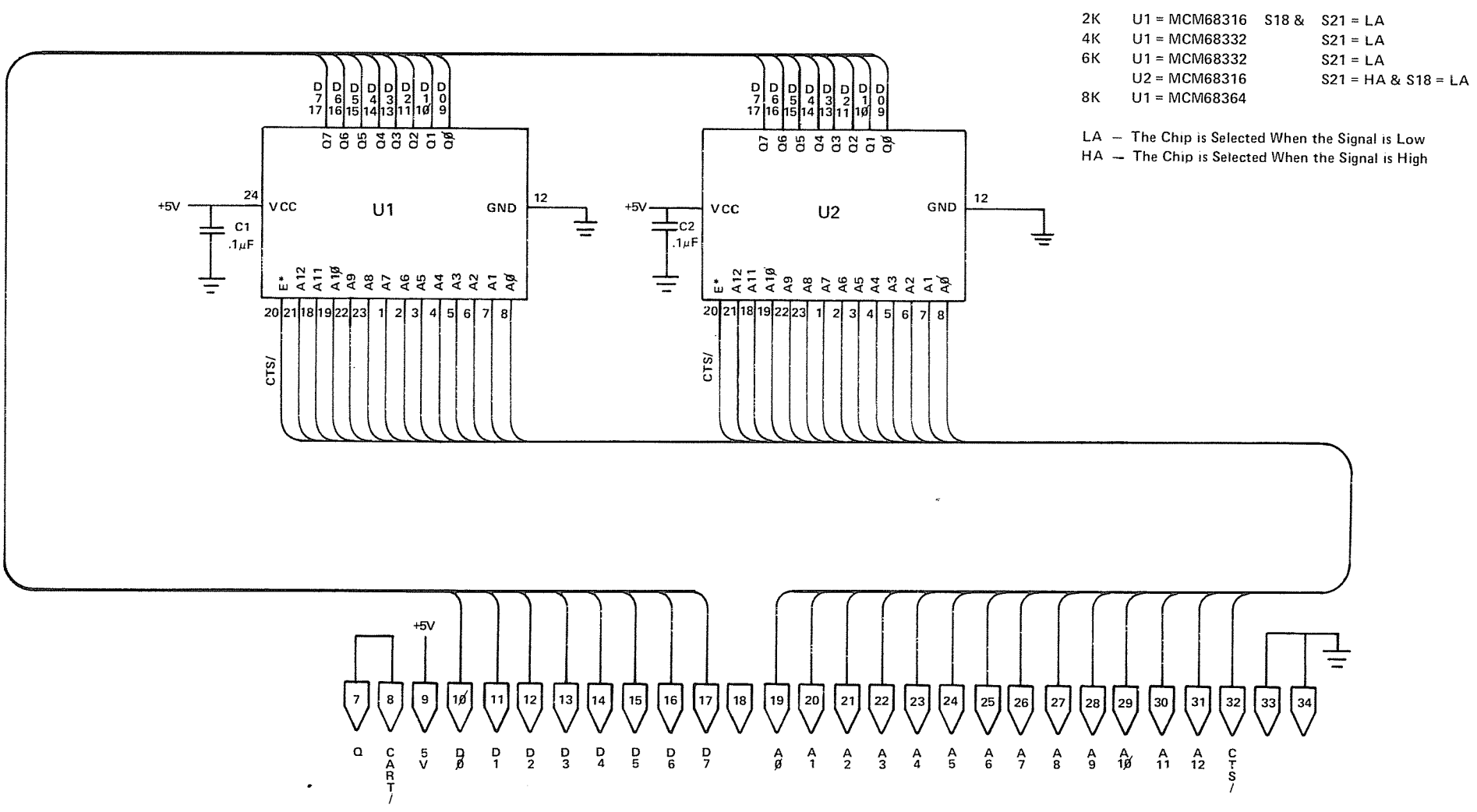


FIGURE 15. ROM CARTRIDGE BOARD SCHEMATIC

RS232C DEVICES

The RS232C Interface hardware in the Color Computer is capable of communication with any device which will operate with the minimum three signal interface. It is also possible that devices which use a larger set of RS232C signals may be used with the Color Computer. This would be accomplished by connecting unused device inputs to the correct high or low level.

In software, the only RS-232C device supported by the 8K BASIC ROM is a serial printer. For use with the printer, the pin assignment of P2 differs from that listed in the RS232C Interface section.

Pin 1 is not used.
Pin 2 is connected to the busy output (or status line) of the printer.
Pin 3 is ground.
Pin 4 is the computer output to the printer.

If your printer does not provide a status line, then pin 2 must be connected to a positive voltage of +3 volts or greater (up to the maximum +12 volts). This tells the computer that the printer is ready all of the time.

In order to operate, the software must make several assumptions about the printer. These assumptions are:

1. 600 Baud
2. The Printer width is 132 columns.
3. The printer generates a busy output when it is not ready.
4. The printer will automatically carriage return at the end of a line.
5. The data format is one start bit (logical zero), seven data bits (LSB first), two stop bits (logical one), and no parity. (1)

Some printers will require that these assumptions be modified. This may be accomplished by changing RAM variables or by a special driver routine.

A list of all of the printer variables is given in Table 6. Also, Table 7 lists some alternate values for these variables. The last comma field variable (2) should be set equal to the width value minus the comma field width. The comma field width will normally stay at 16.

NOTES:

(1) In Revision 1.1 ROM's this format has been changed from seven to eight data bits.

(2) Comma field is the number of spaces allowed to print a variable value.

TABLE 6. LINE PRINTER VARIABLES

VARIABLE	HEXIDECIMAL ADDRESS	DECIMAL ADDRESS	INITIAL VALUE HEXI-DECIMAL	INITIAL VALUE DECIMAL
BAUD RATE MSB	0095	149	00	0
BAUD RATE LSB	0096	150	57	87
LINE DELAY MSB	0097	151	00	0
LINE DELAY LSB	0098	152	01	1
COMMA FIELD WIDTH	0099	153	10	16
LAST COMMA FIELD	009A	154	70	112
LINE PRINTER WIDTH	009B	155	84	132

TABLE 7. ALTERNATE LINE PRINTER VARIABLE VALUES

BAUD RATE:	DECIMAL VALUE MSB	DECIMAL VALUE LSB	HEXIDECIMAL VALUE MSB	HEXIDECIMAL VALUE LSB
120 BAUD	1	202	Ø1	CA
300 BAUD	Ø	180	ØØ	BE
600 BAUD	Ø	87	ØØ	57
1200 BAUD	Ø	41	ØØ	29
2400 BAUD	Ø	18	ØØ	12

LINE DELAY:	DECIMAL VALUE MSB	DECIMAL VALUE LSB	HEXIDECIMAL VALUE MSB	HEXIDECIMAL VALUE LSB
.288 SECONDS	64	Ø	4Ø	ØØ
.576 SECONDS	128	Ø	8Ø	ØØ
1.15 SECONDS	255	255	FF	FF

WIDTH:	DECIMAL VALUE	HEXIDECIMAL VALUE
16 CHARACTERS/LINE	16	1Ø
32 CHARACTERS/LINE	32	2Ø
64 CHARACTERS/LINE	64	4Ø
255 CHARACTERS/LINE	255	FF

JOYSTICKS

The joysticks are two identical assemblies which will plug into either P3 or P4. Figure 16 shows a schematic of the joystick assembly. It consists simply of a push button switch for the fire switch and the dual potentiometers connected by a mechanical assembly.

The mechanical assembly causes both potentiometers to be changed at the same time. This gives the effect of a two-dimensional control. The potentiometers are connected so that 5 volts is applied to one side of the variable resistor, and ground is connected to the other. This allows the center wiper to vary from Ø to 5 volts as the handle is moved. The push button switch merely provides a momentary ground contact for an input signal.

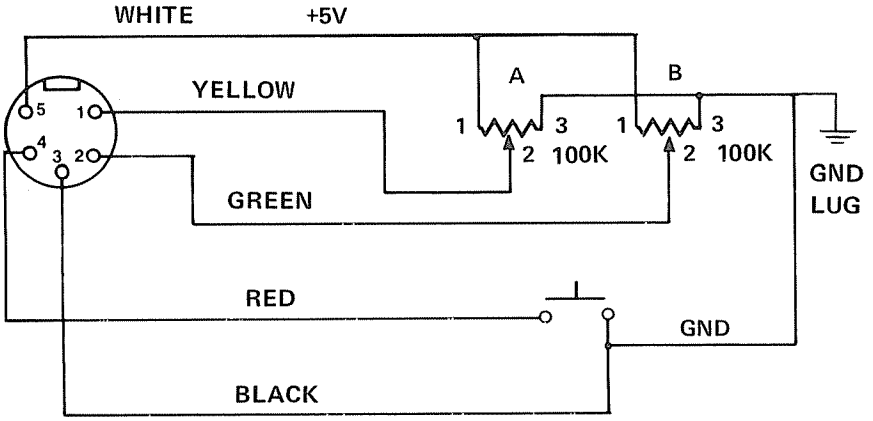


FIGURE 16. JOYSTICK SCHEMATIC

TV SWITCH BOX

The antenna switch box consists of a switch and a balun, with connectors provided for attachment to the computer, the TV antenna, and the home TV. The switch box is connected to the customer's TV, through the 300 ohm twin lead output. The TV antenna is attached directly to the switch box. The computer output is connected through a 75 ohm coax cable to the phone plug input on the switch box. Figure 17 shows a schematic of the antenna switch box.

From the computer, the signal is connected to a balun in the switch box, which matches the modulator's 75 ohm output impedance to a TV's 300 ohm antenna input impedance. This signal is then connected to the switch. The switch is specially designed to provide the 60dB of isolation required between the computer and the TV antenna.

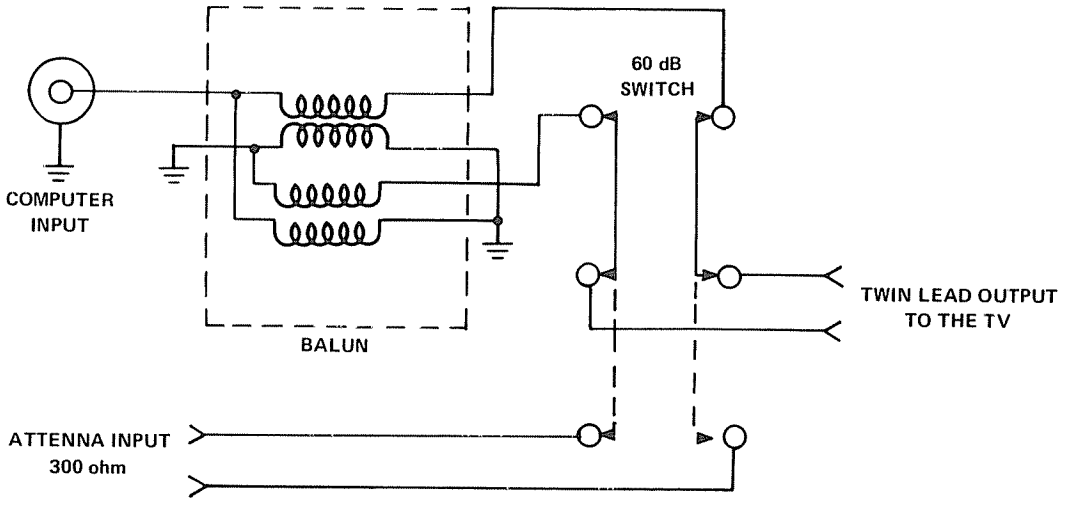


FIGURE 17. ANTENNA SWITCH BOX SCHEMATIC

SECTION IV

TROUBLESHOOTING

FAULT ISOLATION

Problems with the TRS-80 Color Computer may be divided into two major categories, I/O problems and "dead" computer problems. If the computer will display the sign-on message, then the Color Computer Diagnostic ROM may be used to isolate the section of the computer that is bad. If, however, the computer displays garbage on the TV screen, then one of the major logic functions has failed.

A "dead" computer (garbage on the display or no display) indicates a major malfunction of the machine. In this case, the first thing to check is the power supply voltage levels. These may be checked at the following points.

+5 volts — Test Point 12
-5 volts — Test Point 11
+12 volts — Test Point 9
-12 volts — Test Point 10
Ground — Test Point 3

Or if you are having problems finding these test points, check the voltages on one of the RAM chips (U20 - U27).

Pin 1 = -5 volts (minus five)
Pin 8 = +12 volts
Pin 9 = +5 volts

If one of the power supply voltages is off by more than 5%, determine if the fault is due to a failure within the power supply or to another section affecting the power supply. Refer to the Power Supply section for possible causes of the problem and tips on how correct it.

If all of the voltages are correct but there is no display whatsoever on the TV screen, a video problem is evident. Refer to the Video Interface section for hints on fixing this problem.

If all of the voltages are at the proper level but you still have a screen full of garbage, then you should try chip substitution. Try replacing the following chips.

U20 - U27	Dynamic RAM chips
U10	MC6883 Dynamic RAM controller
U1	MC6809E CPU chip
U4 and U8	MC6821 PIA
U3	MCM68A364 ROM

Make sure you replace the RAM chips with the same size (4K, 16K, or 32K) as the original chips.

If the computer still displays garbage after the chip substitution, the most likely problem is a short on the address or data bus. Remove the ground plane and carefully look at the insulator and the PC Board. It is possible that one of the IC leads has punctured the insulator and is shorting out. If the computer operates without the ground plane, then trim the excess leads on the bottom of the board. Make sure you don't leave any loose material on the bottom of the board when you replace the ground plane.

If the computer still fails to operate after removing the ground shield, you will need to start a methodical checking process. First, make certain that the CPU (U1) is running by using an oscilloscope to look at some of the address lines (pins 8 - 23) and the data lines (pins 24 - 31). They should normally be changing states fairly fast. If they are not changing at all, then one of the control or clock signals to the CPU is wrong. Pins 34 and 35 of U1 should have a 0.89 MHz clock input to the CPU (U1). Pins 2, 3, 4, 40, and 37 should all be high. Pin 39 should be low.

If the CPU is running then there is some short or open on the address or data bus. Check to make certain that all of the sockets are properly soldered into the board. It is possible that one of the pins on a socket has been bent under. Also check for any defect on the board such as a solder short or a broken etch.

DIAGNOSTIC NOTES

It is possible that the Diagnostic test may designate a part of the circuit that is not the faulty part. If the designated part does not seem to be causing the problem, the following notes may help.

A video problem is usually caused by U7 (MC6847), however, a video failure may also be caused by U10 (MC6883). The chip U10 could also be the cause of a RAM problem. A RAM connected failure of U10 would be indicated if repeated trys of the RAM test showed random chip failures, or if replacing the indicated RAM chip does not fix the problem.

VIDEO INTERFACE

The video interface is composed of four primary parts U6, U7, U12, and U5. Also U10 is used to provide the video address lines to the RAM. The most likely source of a problem is U7 (MC6847). However, it is always a good idea to isolate the source of a problem before trying to desolder chips.

If the problem is no picture or a distorted picture, then a new switch box and cable should be tried. If you still do not have a picture, then use your oscilloscope to look at U7, pin 28. You should have a video signal at this point. (Refer to the Video Interface section of the Theory of Operation for an example of what this signal should look like.) If you do not

have a video signal, check U7, pin 33. There should be a 3.579 MHz clock signal at this point. If you have a clock signal but no video at pin 33, then U7 is bad. (You might also check pin 17 just to make sure the chip has +5 volts.)

If you have a video signal at pin 28 of U7 but still have no TV picture, the next point to check is U12, pin 12. Again there should be a video signal at this point. If you do not have a video signal on pin 12 then check the inputs to the chip. (Pin 2 = 3.579 MHz clock; pin 11 = +5 volts; pin 9 = input video; etc.) Also check for +8 volts on the top side of R16. If all the inputs are present then U12 is probably bad.

The last place to check the video signal is on the modulator input (pin 1 of U5). If you have the video signal at the point and at the proper DC level, then U5 is probably bad. If the video signal is not present, then Q1 or one of the associated biasing resistors is probably the faulty part. (Make sure you check for +8 volts on the collector of Q1.) If the video signal is at the wrong DC level, try adjusting R21. If the signal will not adjust to the proper level then most likely one of the biasing resistors for Q1 is bad. U12 may also cause this problem if the output from pin 12 is out of spec.)

If the video problem is associated with only one mode of operation (graphics, semigraphics, or alphanumerics) then one of three chips is causing the problem; U6, U7, or U10. If some of the dots are missing from alphanumeric characters then U7 is faulty. If some characters are being displayed as the wrong character, then the correct data is not being supplied to the data inputs to U7. U6 latches this data so it may be causing the problem or there may be a short on the data lines.

If some of the graphics modes do not work, then check pins 27, 29, 30, and 35 of U7. These pins should change from high to low as you change from one mode to the next. These signals are supplied from U4, which could be causing the problem if signals are changing properly. If these pins all seem to change, then the problem is caused by U10 or U7. (Since U10 is in a socket, try replacing it first.)

JOYSTICK INTERFACE

Before you tear into the computer to fix a joystick related problem, try a second set of joystick controllers to make sure the problem is in the computer. The only possible fire switch problem, that will not also show up as a keyboard problem, is if L2 or L3 is broken or the etch is cut or shorted.

To troubleshoot the joystick interface you should have the Diagnostic joystick test running. If the problem is missing blocks, then one of the bits going to the D/A converter is not changing properly. Set both joysticks to the bottom right corner. Use an oscilloscope to check the D/A pins from U4 (pins 4 through 9). If all of the pins are changing then U4 is good. Also check the output pins of U2, they should all be changing. Finally, look at the output of the D/A converter (U14, pin 8). At this point you should see an even stairstep function. If one or more of the steps is twice as large as the other steps then one of the resistors is bad.

If the problem is that the joysticks do not work in one or more directions, connect an oscilloscope to U9, pin 9. With the Diagnostic joystick test running you should see four DC voltage segments. One dimension on each joystick should affect one of the segments. Try moving the joysticks around to check this. You can look at the DC voltages directly from the pots at the input pins of U9. If the inputs of U9 are changing (including select pins 6 and 7) but the output is not, then U9 is probably faulty.

If U9 seems to be working properly then check U14. Set both joysticks to the center. Checking pin 8 of U14 you should see an even stairstep function going up to approximately 2.5 volts. The output, pin 14, should be switching each time the stairstep on pin 8 peaks. If the output is not switching, then U14 is not working.

CASSETTE INTERFACE

If you are having cassette problems, run the joystick test first to confirm that the D/A is working. If the computer passes the joystick test then there are only three other components in the output circuit that could be failing; R41, R42, or C82.

The cassette input circuit is a simple sinewave-to-squarewave converter. To test it you will need a long tape of consistent data. By running this tape, your should be able to compare the input sinewave to the output squarewave and see if the converter is working. If this circuit is working, the only other part involved in the cassette interface is U4.

If the problem is motor control, relay K1 is most likely bad. To test this, check to see that the collector of Q4 is switching as you use the MOTOR ON and MOTOR OFF command. If it is not switching, Q4 or the PIA output pin is faulty.

KEYBOARD INTERFACE

The keyboard interface is a very simple electronic circuit. The only digital part ised is U8. Usually a keyboard failure will be caused by a mechanical failure of the keyboard itself, or a short or open in the calbe. Mechanical failures will usually be only one isolated key failing. Cable failures will cause an entire keyboard row or column not to work.

RS-232 INTERFACE

The RS-232 Interface utilizes three level converter circuits. Isolating the problem in these three circuits will be a simple matter of comparing the input to the output.

Connect a DIN-type plug to the I/O Serial jack to short together pins 1, 2, and 4. Now type in the following test program:

```
 5 POKE 65312,2
10 FOR X = 0 TO 10: NEXT X
15 POKE 65312,0
20 FOR X = 0 TO 10: NEXT X
25 GOTO 5
```

Run the program and check pin 2 of U15; a switching TTL waveform should be present. Pin 6 of U15 should have the same waveform except that it will be switching from +11 volts to - 11 volts. Also check pins 4 and 6 of U14. These pins should have the same waveform switching from 0 to +10 volts. The outputs of U14, pins 1 and 2 should show the original TTL signal when the test program is running.

POWER SUPPLY

If you have a power supply problem, usually only one of the four supply voltages will be bad. However the +5 volt supply is powered by the +12 volts supply, so a bad +12 volt supply will also cause the +5 volt supply to fail. Anytime you have a supply that is at zero volts, you should measure the resistance between ground and that supply (with power off). This will quite often show that you have a short to ground. Please note that the +5 volt supply has an overvoltage diode, CR17, which will automatically short to ground in the case of an overvoltage condition on the +5 volt power supply.

If the problem is not an external short to ground, refer to Figure 1 and check the voltages along the affected power supply. If the voltage is bad at one output of CR11, the regulator or the filter capacitor is bad. If both voltages are bad then CR11 is faulty. Check that CR11 has the correct input voltage from the transformer. If the voltage is correct at the input to the regulator and the output is not shorted, then the regulator is bad.

The +5 volt supply is more complex than the other supplies. However, you may use the same troubleshooting method as with the other supplies. Check the voltage from the input to the output of the supply until you find the point where the voltages are wrong. This will usually point to the bad device. A faulty +5 volt supply may be caused by U13, Q2, or Q3.

If the +5 volt supply was shorted to ground by CR17 then there is also a problem with the regulator circuit. To correct this, remove CR17 and break the +5 volt line while troubleshooting the supply. Removing R66 will break the +5 volt output line.

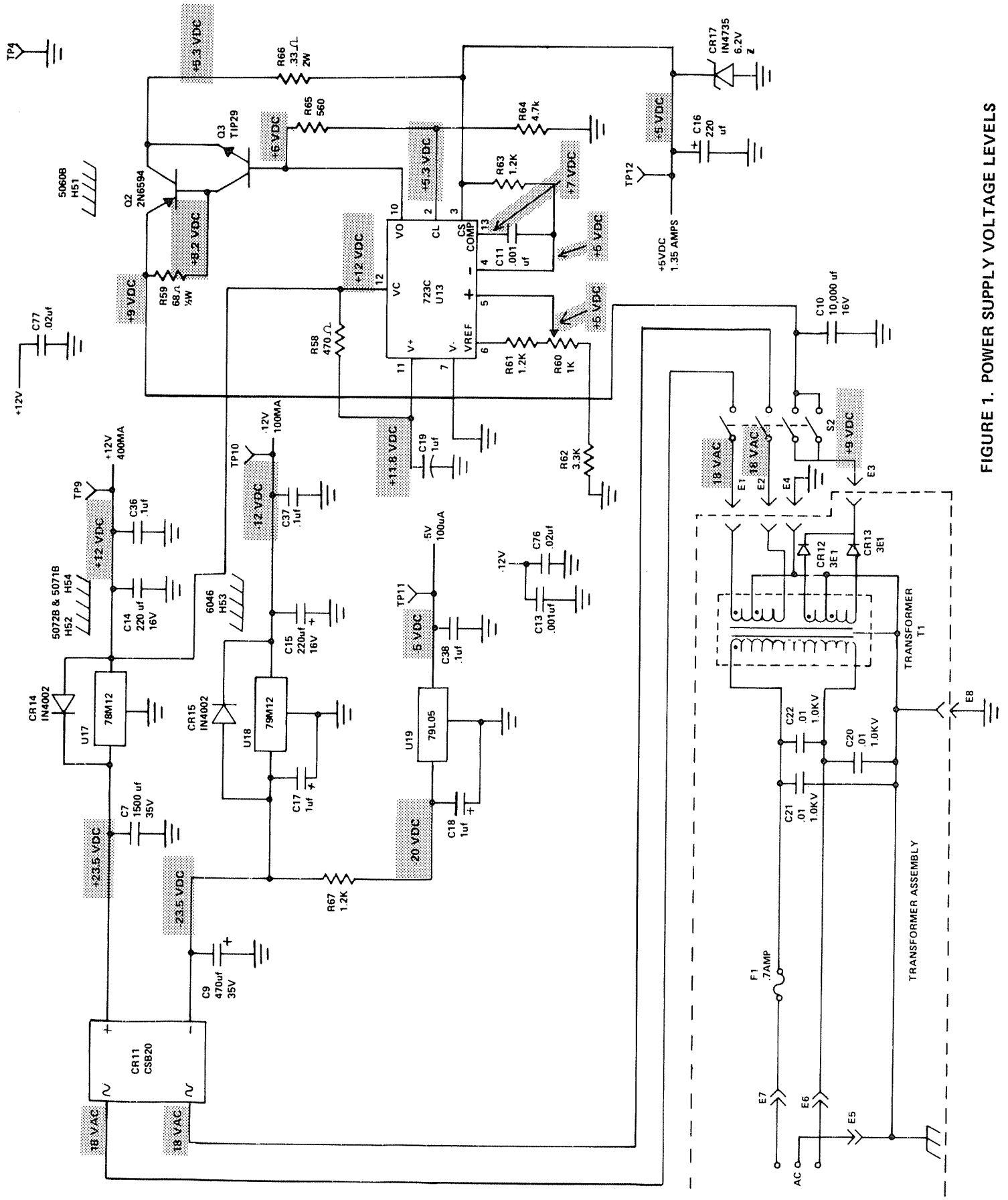


FIGURE 1. POWER SUPPLY VOLTAGE LEVELS

SECTION V

PARTS LISTS

PRINTED CIRCUIT BOARD PARTS LIST

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	CAPACITORS		
C1	1μF, 50V, electrolytic, radial	8325104	ACC105QJAP
C2	10μF, 25V, non-polarized, radial	8396101	ACC106QFBP
C3	100μF, 16V, electrolytic, radial	8326251	ACC107QDAP
C4	9 - 35pF, variable	8360356	AC-4926
C5	100μF, 16V, electrolytic, radial	8327101	ACC107QDAP
C6	25μF, electrolytic, radial	8326251	ACC256MDAP
C7	1500μF, 35V, electrolytic, axial	8318153	ACC158QGAA
C8	100μF, 16V, electrolytic, radial	8327101	ACC107QDAP
C9	470μF, 35V, electrolytic, radial	8327473	ACC477QGAP
C10	10,000μF, 16V, electrolytic, axial	8319101	ACC109QDAA
C11	0.001μF, 50V, PO	8352104	ACC102KJGP
C12	100μF, 16V, electrolytic, radial	8327101	ACC107QDAP
C13	0.001μF, 50V, ceramic disc	8302104	ACC102QJCP
C14	220μF, 16V, electrolytic, radial	8327221	ACC227QDAP
C15	220μF, 16V, electrolytic, radial	8327221	ACC227QDAP
C16	220μF, 16V, electrolytic, radial	8327221	ACC227QDAP
C17	1μF, 50V, tantalum	8335104	ACC105QJTP
C18	1μF, 50V, tantalum	8335104	ACC105QJTP
C19	1μF, 50V, tantalum	8335104	ACC105QJTP
C20	0.01μF, 1kv, ceramic disc	8303108	ACC103QXCP
C21	0.01μF, 1kv, ceramic disc	8303108	ACC103QXCP
C22	0.01μF, 1kv, ceramic disc	8303108	ACC103QXCP
C23	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA
C24	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA
C25	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA
C26	0.022μF, 50V	8303224	ACC223QJCP
C27	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA
C28	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA
C29	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA
C30	0.022μF, 50V	8303224	ACC223QJCP
C31	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA
C32	↓	↓	↓
C33			
C34			
C35			
C36			
C37			
C38			
C39			
C40			
C41			
C42			
C43			
C44			
C45			
C46			
C47			
C48			
C49			
C50	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA

PRINTED CIRCUIT BOARD PARTS LIST (cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	CAPACITORS (cont'd)		
C51	39pF, ceramic disc	8300394	ACC390QJCP
C52	20pF, 50V, ceramic disc	8300204	ACC200QJCP
C53	56pF, 50V, ceramic disc	8300564	ACC560QJCP
C54	0.022μF, 50V	8303224	ACC223QJCP
C55	0.022μF, 50V	8303224	ACC223QJCP
C56	0.022μF, 50V	8303224	ACC223QJCP
C57	0.01μF, 50V, ceramic disc	8303104	ACC103QJCP
C58	0.01μF, 50V, ceramic disc	8303104	ACC103QJCP
C59	0.022μF, 50V	8303224	ACC223QJCP
C60	0.022μF, 50V	8303224	ACC223QJCP
C61	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA
C62	↓	↓	↓
C63			
C64			
C65			
C66			
C67			
C68			
C69			
C70			
C71			
C72	0.1μF, 50V, monolithic, axial	8374104	ACC104QJCA
C73	56pF, 50V, ceramic disc	8300564	ACC560QJCP
C74	0.022μF, 50V	8303224	ACC223QJCP
C75	56pF, 50V, ceramic disc	8300564	ACC560QJCP
C76	0.022μF, 50V	8303224	ACC223QJCP
C77	↓	↓	↓
C78			
C79			
C80			
C81	0.022μF, 50V	8303224	ACC223QJCP
C82	0.0022μF, 50V	8302224	ACC222MJCP
C83	0.001μF, 50V, ceramic disc	8302104	ACC102QJCP
C84	0.022μF, 50V	8303224	ACC223QJCP
C85	220pF, 50V, ceramic disc	8301224	ACC221QJCP
	CONNECTORS		
P1	40 pin, AMP	8519093	AJ6902
P2	4 pin DIN	8519094	AJ6904
P3	6 pin DIN	8519095	AJ6905
P4	6 pin DIN	8519095	AJ6905
P5	5 pin DIN	8519085	AJ6903
*P6	Keyboard shield connector	8519104	AJ6907
P7	16 pin Header	8519106	AJ6906

*will not appear on later revision Boards.

PRINTED CIRCUIT BOARD PARTS LIST (cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	CRYSTAL		
X1	14.31818MHz	8409008	AMX2797
	DIODES		
CR1	1N4148	8150148	ADX1152
CR2	↓	↓	↓
CR3			
CR4			
CR5			
CR6			
CR7	1N4148	8150148	ADX1152
CR8	1N4002	8150002	ADX1148
CR9	1N982, zener	8150982	ADX1103
CR10	1N982, zener	8150982	ADX1103
CR11	VM-28, bridge rectifier	8160028	AMX4582
CR12	1N5401, 100V, 3A	8160401	ADX1474
CR13	1N5401, 100V, 3A	8160401	ADX1474
CR14	1N4002	8150002	ADX1148
CR15	1N4002	8150002	ADX1148
CR16	1N5228, 3.9V, zener	8150228	ADX1473
CR17	1N4735, 6.2V, zener	8150735	ADX0214
	FUSE		
F1	700mA (0.7A)	8479003	AHF1185
	INDUCTORS		
L1			
L2	3.3μh	8419005	ACA8059
L3	3.3μh	8419005	ACA8059
	INTEGRATED CIRCUITS		
U1	MC6809E, CPU	8040809	AXX3051
U2	MC14050B, Latch	8030050	AMX4584
U3	MCM68A364, BASIC ROM	8040364	AXX3052
U4	MC6821, PIA	8040821	AMX4578
U5	UM1285-8, Modulator	8050285	AMX4576
U6	74LS273, Octal Flip-Flop	8020273	AMX4227
U7	MC6847, VDG	8040847	AMX4575
U8	6821, PIA	8040821	AMX4578
U9	MC14529B, Data Separator	8030529	AMX4585
U10	MC6883L, SAM	8040278	AMX4579
U11	74LS138, Decoder	8020138	AMX4583
U12	MC1372, Video Mixer	8050372	AMX4574
U13	723C, +5V Regulator	8050723	AMX3548
U14	LM339, Quad Comparator	8050339	AMX4200
U15	741C, Op Amp	8050741	AMX4258
U16	74LS244, Buffer	8020244	AMX3864
U17	78M12, +12V, Regulator	8050812	AMX4577

PRINTED CIRCUIT BOARD PARTS LIST (cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	INTEGRATED CIRCUITS (cont'd)		
U18	79M12, -12V Regulator	8050912	AMX4188
U19	79L05, -5V Regulator	8051905	AMX4260
*U20	MCM4027AC3, 4K RAM	8040027	AXX3044
*U21	↓	↓	↓
*U22			
*U23			
*U24			
*U25			
*U26			
*U27	MCM4027AC3, 4K RAM	8040027	AXX3044
†U28	MCM68A364, BASIC ROM Extended	8042364	AXX3054
U29	74LS02, Quad NOR gate	8020002	AMX3551
*For 16K RAM model:			
U20 - U27	SCM90072C, 16K RAM	8040016	AXX3055
†For 16K RAM version only.			
	RELAY		
K1	R7336-1	8429102	AR8130
	RESISTORS		
R1	100K, 1/4W, 5%	8207410	AN0371EEC
R2	100K, 1/4W, 5%	8207410	AN0371EEC
R3	4.7K, 1/4W, 5%	8207247	AN0247EEC
R4	4.7K, 1/4W, 5%	8207247	AN0247EEC
R5	4.7K, 1/4W, 5%	8207247	AN0247EEC
R6	4.7K, 1/4W, 5%	8207247	AN0247EEC
R7	4.7K, 1/4W, 5%	8207247	AN0247EEC
R8	18K, 1/4W, 5%	8207318	AN0303EEC
R9	150 ohm, 1/4W, 5%	8207115	AN0142EEC
R10	10K, 1/4W, 1%	8201310	AN0281BEE
R11	20K, 1/4W, 1%	8201320	AN0306BEE
R12	40.2K, 1/4W, 1%	8201340	AN0597BEE
R13	80.6K, 1/4W, 1%	8201381	AN0359BEE
R14	162K, 1/4W, 1%	8201416	AN0385BEE
R15	324K, 1/4W, 1%	8201432	AN0408BEE
R16	3.9K, 1/4W, 5%	8207239	AN0237EEC
R17	470 ohm, 1/4W, 5%	8207147	AN0169EEC
R18	750 ohm, 1/4W, 5%	8207175	AN0185EEC
R19	12K, 1/4W, 5%	8207312	AN0288EEC
R20	360 ohm, 1/4W, 5%	8207136	AN0159EEC
R21	500 ohm, Trim Pot	8279150	AP7156
R22	10K, 1/4W, 5%	8207310	AN0281EEC
R23	3.9K, 1/4W, 5%	8207239	AN0237EEC
R24	1.5K, 1/4W, 5%	8207215	AN0206EEC
R25	1K, 1/4W, 5%	8207210	AN0196EEC
R26	1K, 1/4W, 5%	8207210	AN0196EEC

PRINTED CIRCUIT BOARD PARTS LIST (cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	RESISTORS (cont'd)		
R27	100 ohm, 1/2W, 5%	8217110	AN0132EFB
R28	10K, 1/4W, 5%	8207310	AN0281EEC
R29	10K, 1/4W, 5%	8207310	AN0281EEC
R30	1K, 1/4W, 5%	8207210	AN0196EEC
R31	4.7K, 1/4W, 5%	8207247	AN0247EEC
R32	4.7K, 1/4W, 5%	8207247	AN0247EEC
R33	220 ohm, 1/4W, 5%	8207122	AN0149EEC
R34	8.2K, 1/4W, 5%	8207282	AN0271EEC
R35	6.8K, 1/4W, 5%	8207268	AN0262EEC
R36	56K, 1/4W, 5%	8207356	AN0345EEC
R37	56K, 1/4W, 5%	8207356	AN0345EEC
R38	15K, 1/4W, 5%	8207315	AN0297EEC
R39	1.5M, 1/4W, 5%	8207515	AN0450EEC
R40	1K, 1/4W, 5%	8207210	AN0196EEC
R41	24K, 1/4W, 5%	8207324	AN0526EEC
R42	75K, 1/4W, 5%	8207375	AN0527EEC
R43	1.5K, 1/4W, 5%	8207215	AN0206EEC
R44	4.7K, 1/4W, 5%	8207247	AN0247EEC
R45	180 ohm, 1/4W, 5%	8207118	AN0144EEC
R46	470 ohm, 1/4W, 5%	8207147	AN0169EEC
R47	1.5K, 1/4W, 5%	8207215	AN0206EEC
R48	10K, 1/4W, 5%	8207310	AN0281EEC
R49	10M, 1/4W, 5%	8207610	AN0482EEC
R50	100 ohm, 1/2W, 5%	8217110	AN0132EFB
R51	10K, 1/4W, 5%	8207310	AN0281EEC
R52	10K, 1/4W, 5%	8207310	AN0281EEC
R53	15K, 1/4W, 5%	8207315	AN0297EEC
R54	15K, 1/4W, 5%	8207315	AN0297EEC
R55	10M, 1/4W, 5%	8207610	AN0482EEC
R56	10M, 1/4W, 5%	8207610	AN0482EEC
R57	1K, 1/4W, 5%	8207210	AN0196EEC
R58	470 ohm, 1/4W, 5%	8207147	AN0169EEC
R59	68 ohm, 1/4W, 5%	8207068	AN0111EEC
R60	1K, Trim Pot	8279210	AP0835
R61	1.2K, 1/4W, 5%	8207212	AN0199EEC
R62	3.3K, 1/4W, 5%	8207233	AN0230EEC
R63	1.2K, 1/4W, 5%	8207212	AN0199EEC
R64	4.7K, 1/4W, 5%	8207247	AN0247EEC
R65	560 ohm, 1/4W, 5%	8207156	AN0176EEC
R66	0.33 ohm, 2W	8247833	AN0522EHB
R67	1.2K, 1/4W, 5%	8207212	AN0199EEC
R68	10K, 1/4W, 5%	8207310	AN0281EEC
R69	820 ohm, 1/4W, 5%	8207182	AN0187EEC
R70	not used		
R71	220 ohm, 1/4W, 5%	8207122	AN0149EEC
R72	100K, 1/4W, 5%	8207410	AN0371EEC
*R73	470 ohm, 1/4W, 5%	8207147	AN0169EEC
*R74	470 ohm, 1/4W, 5%	8207147	AN0169EEC

*May appear as follows:

Ferrite Bead, #2643021801	8419012	————

PRINTED CIRCUIT BOARD PARTS LIST (cont'd)

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	RESISTORS (cont'd)		
†R75	33 ohm, resistor pak	8290014	ARX0220
†R76	33 ohm, 1/4W, 5%	8207033	AN0087EEC
†R77	33 ohm, 1/4W, 5%	8207033	AN0087EEC
R78	33 ohm, 1/4W, 5%	8207033	AN0087EEC
R79	33 ohm, 1/4W, 5%	8207033	AN0087EEC
R80	470 ohm, 1/4W, 5%	8207147	AN0169EEC
R81	300K, 1/4W, 5%	8207430	----------
R82	82K, 1/4W, 5%	8207382	AN0360EEC
R83	33 ohm, 1/4W, 5%	8207033	AN0087EEC
†May appear as follows:			
	Ferrite Bead #264000301	8419014	----------
	SWITCHES		
S1	Reset	8489003	S0852
S2	Power, 4PDT	8489002	S0851
S3	Channel Select, SPST	8489029	S9142
	TRANSFORMER		
T1	33.5V and 16.3V, 50-60Hz	8790020	ATA0856
	TRANSISTORS		
Q1	MPS3904	8110904	AMX3583
Q2	2N6594, PNP	8100594	AMX3799
Q3	TIP29, NPN	8110029	AMX3582
Q4	2N2222	8110222	AMX4263

DESCRIPTION	QUANTITY	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	MISCELLANOUS		
Cartridge Slide Guide	1	8719110	ART3326
Clip, Cord (Keyboard)	1	8559009	AHB9420
Clip, Fuse	2	8479004	AF1176
Ground Plane Bottom	1	8729043	AHD3325
Ground Plane Fastener	16	8559023	AHD9012
Ground Plane Insulator	1	8539008	ART3324
Insulator, mica	1	8539009	AHC0332
Insulator, mica (U18)	1	8539003	AHB9181
Jumper Cable, transformer	1	8709158	AW2586
Jumper Plug	2	8519021	AJ6769
Nut, #4	2	8579003	AHD7143
Screw, #4-40 x 3/8"	2	8569082	AHD9011
Socket, 16 pin	8	8509003	AJ6581
Socket, 24 pin	2	8509001	AJ6579
Socket, 40 pin	4	8509002	AJ6580
Tubing, air shrink, 3/4"	3	8539011	AHC0323

ILLUSTRATED PARTS BREAKDOWN

ITEM NUMBER	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
1	Case Top	8719107	AZ5844
2	Cartridge Door	8729035	ADA0337
3	Cartridge Slide Guide	8719110	ART3326
4	Keyboard	9790501	AXX0206
	Keyboard Cable Assembly	8709141	AW2589
5	Insulator, ground plane	8539008	ART3324
6	Ground Plane	8729043	ART3325
7	Case Bottom	8719108	AZ5845
8	Screw, #6 x 7/8"	8569092	AHD9016
9	Screw, #6 x 1 1/4"	8569085	AHD9015
10	Power Cord Assembly	8709150	AW2587
11	Transformer	8790020	ATA0856
12	Screw, #6 x 1/2"	8569086	AHD9013
13	Top Cover Support	8729045	ART3323
14	Top Cover	8729044	AZ5846
15	Logo, Color Computer	8719120	AHC0324
16	RAM ID, 4K	8789260	AHC0320

MISCELLANEOUS

not shown	Fastener, ground plane (16)	8559023	AHD9012
not shown	Feet, Rubber (4)	8719123	AF0315
not shown	Screw, #6 x 1/2"	8569087	AHD9014

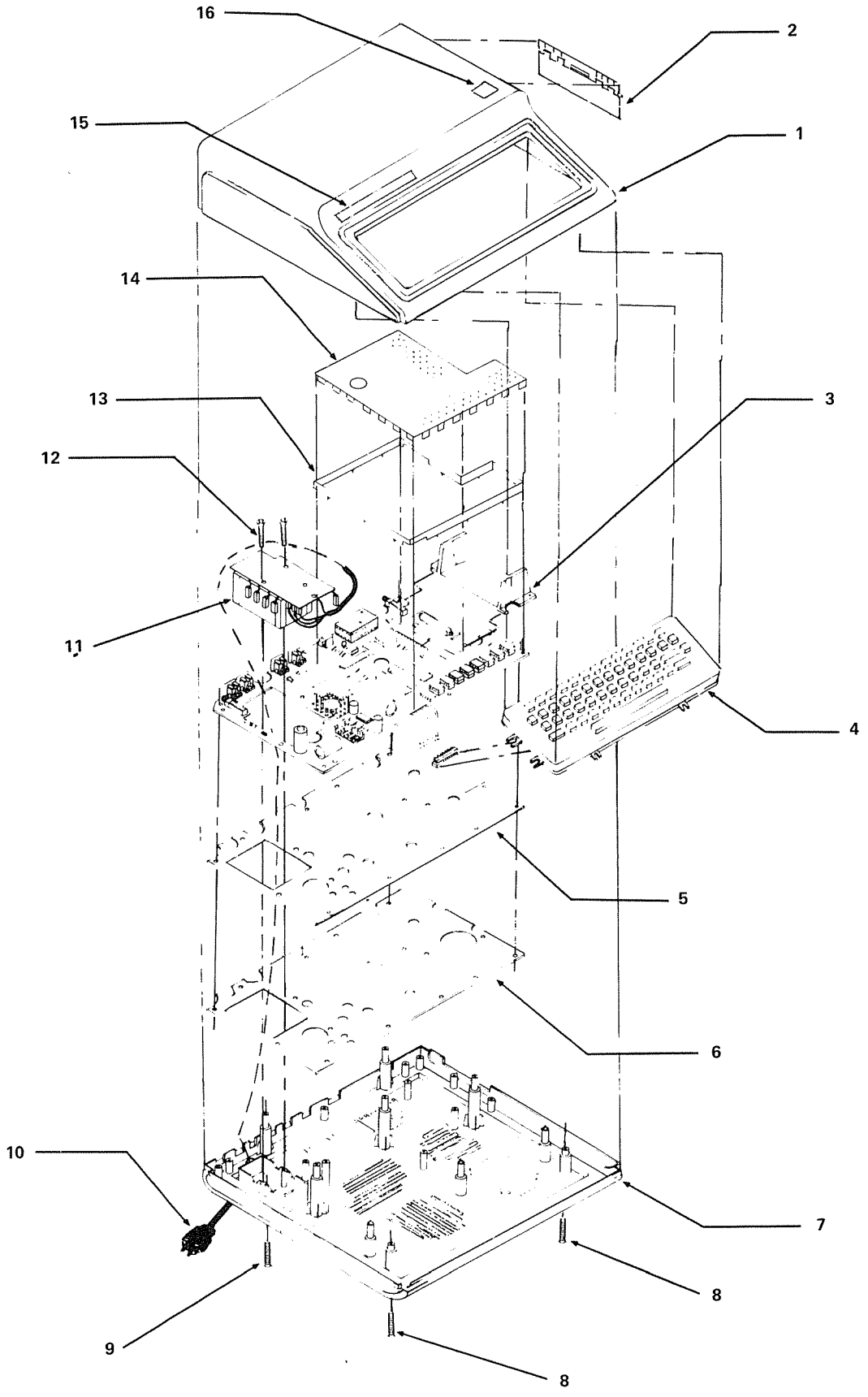


FIGURE 1. ILLUSTRATED PARTS BREAKDOWN

SECTION VI

PRINTED CIRCUIT BOARD

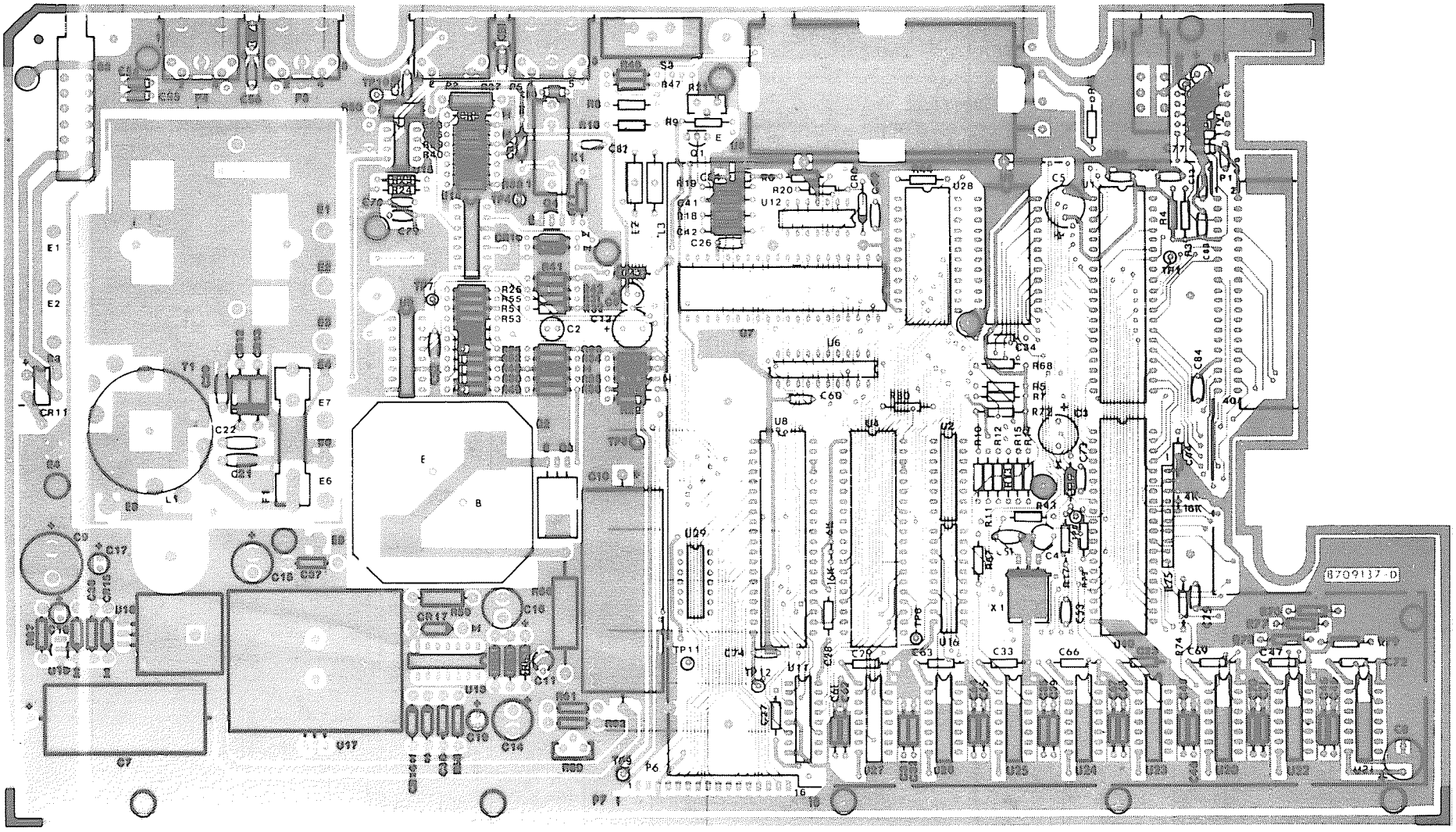


FIGURE 1. PRINTED CIRCUIT BOARD – COMPONENT SIDE

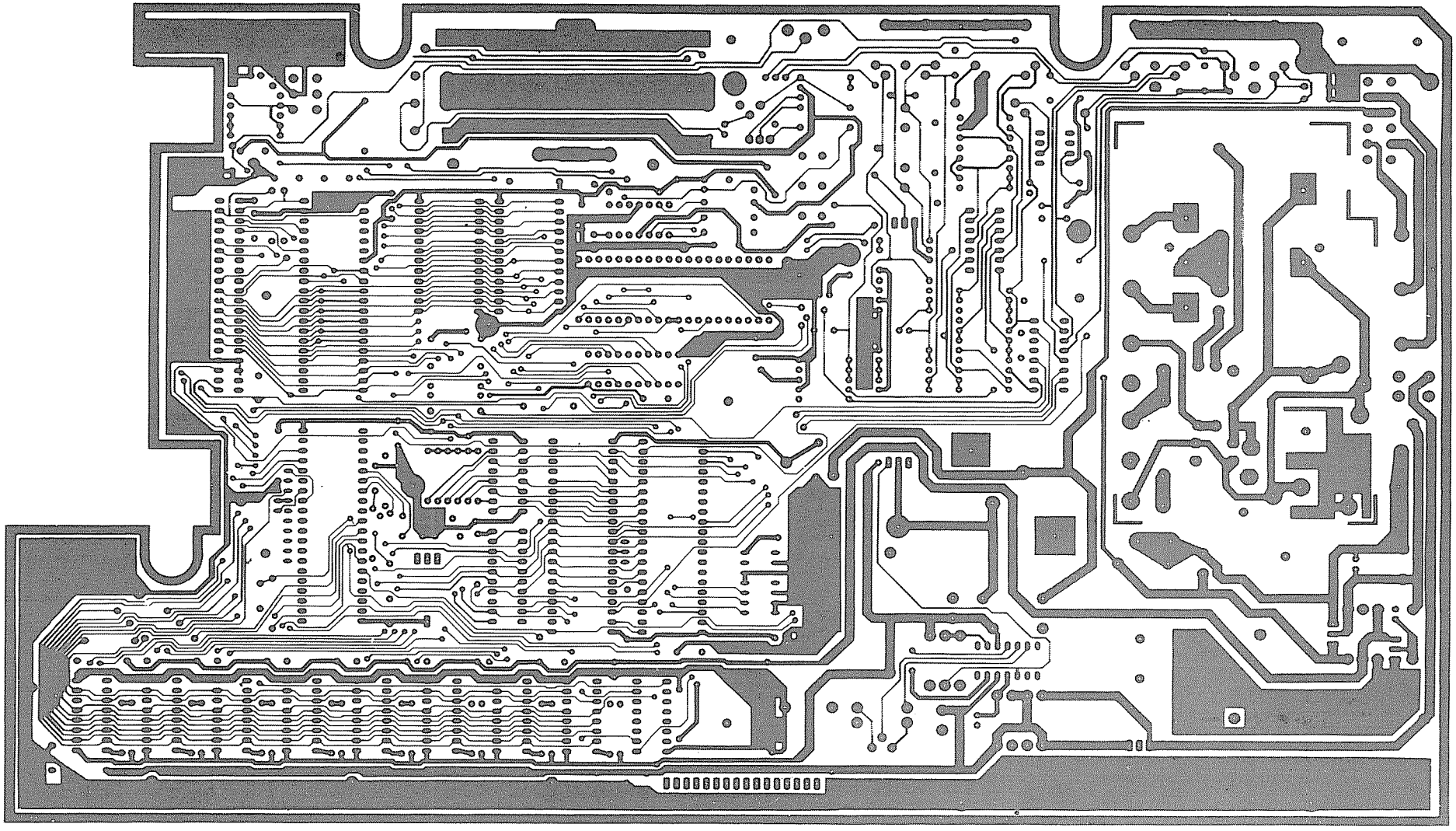
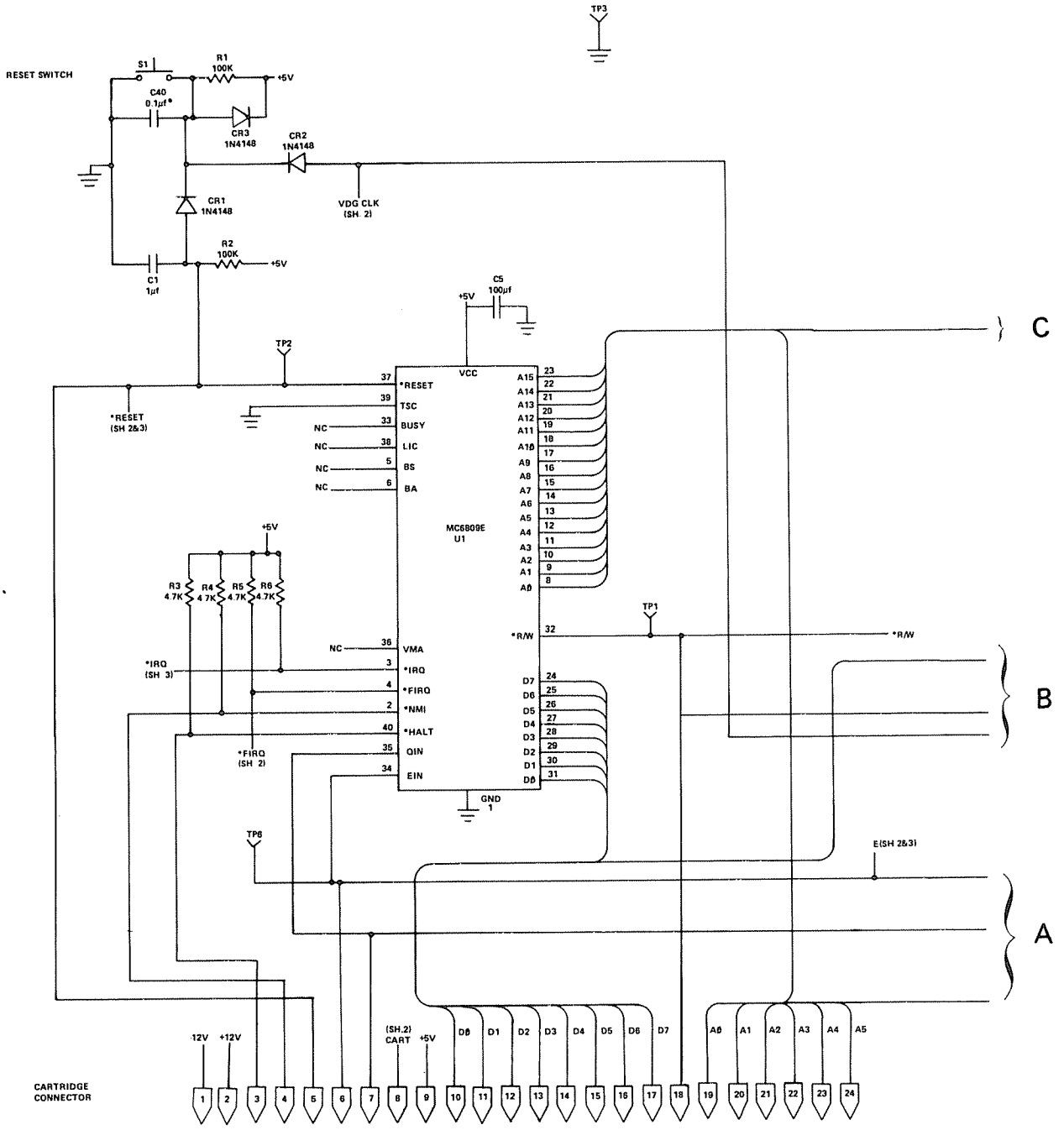


FIGURE 2. PRINTED CIRCUIT BOARD – CIRCUIT SIDE

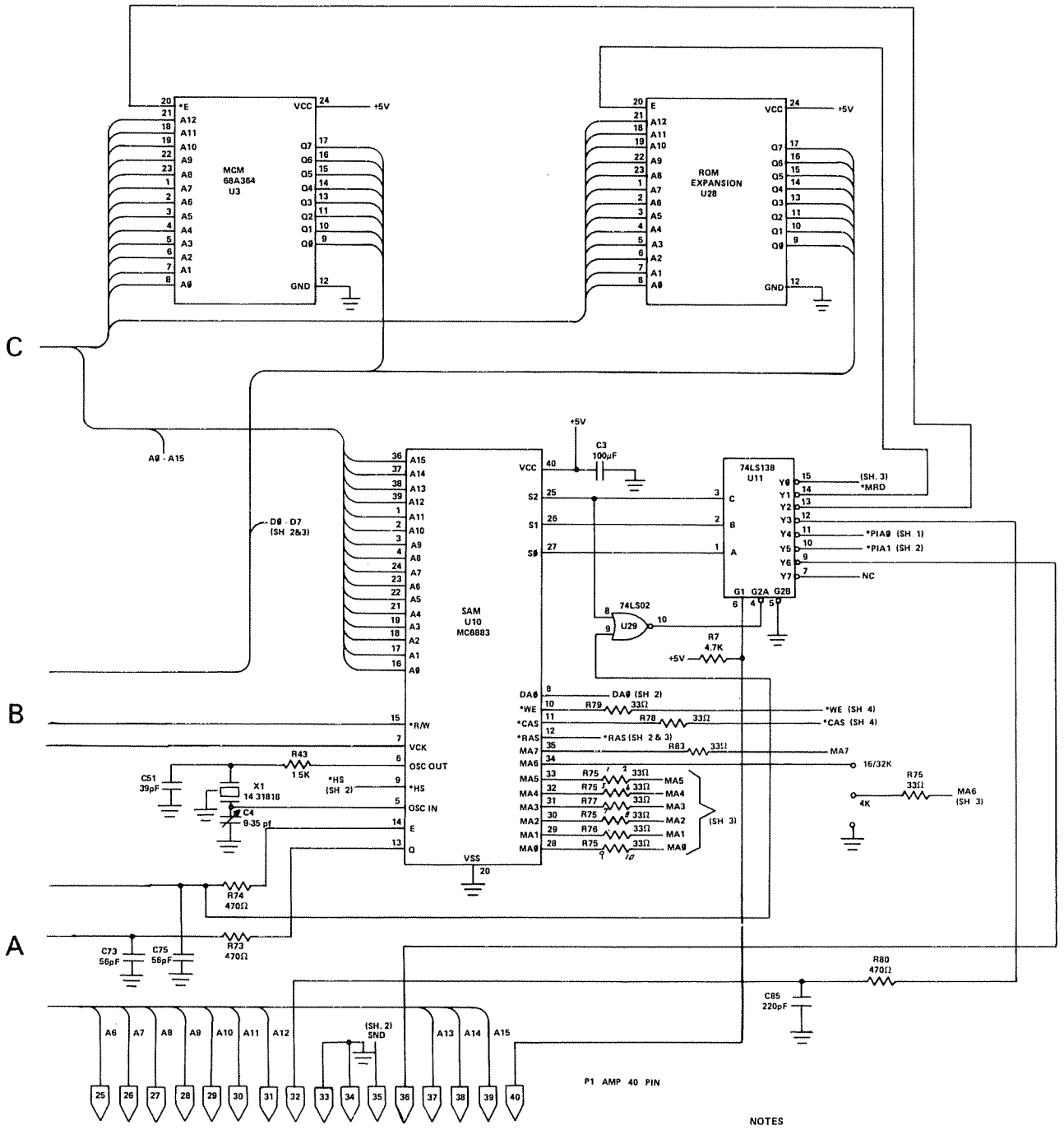
SECTION VII

SCHEMATIC



	+5V	GND
U11	16	8
U29	14	7

COLOR COMPUTER SCHEMATIC – SHEET 1



NOTES

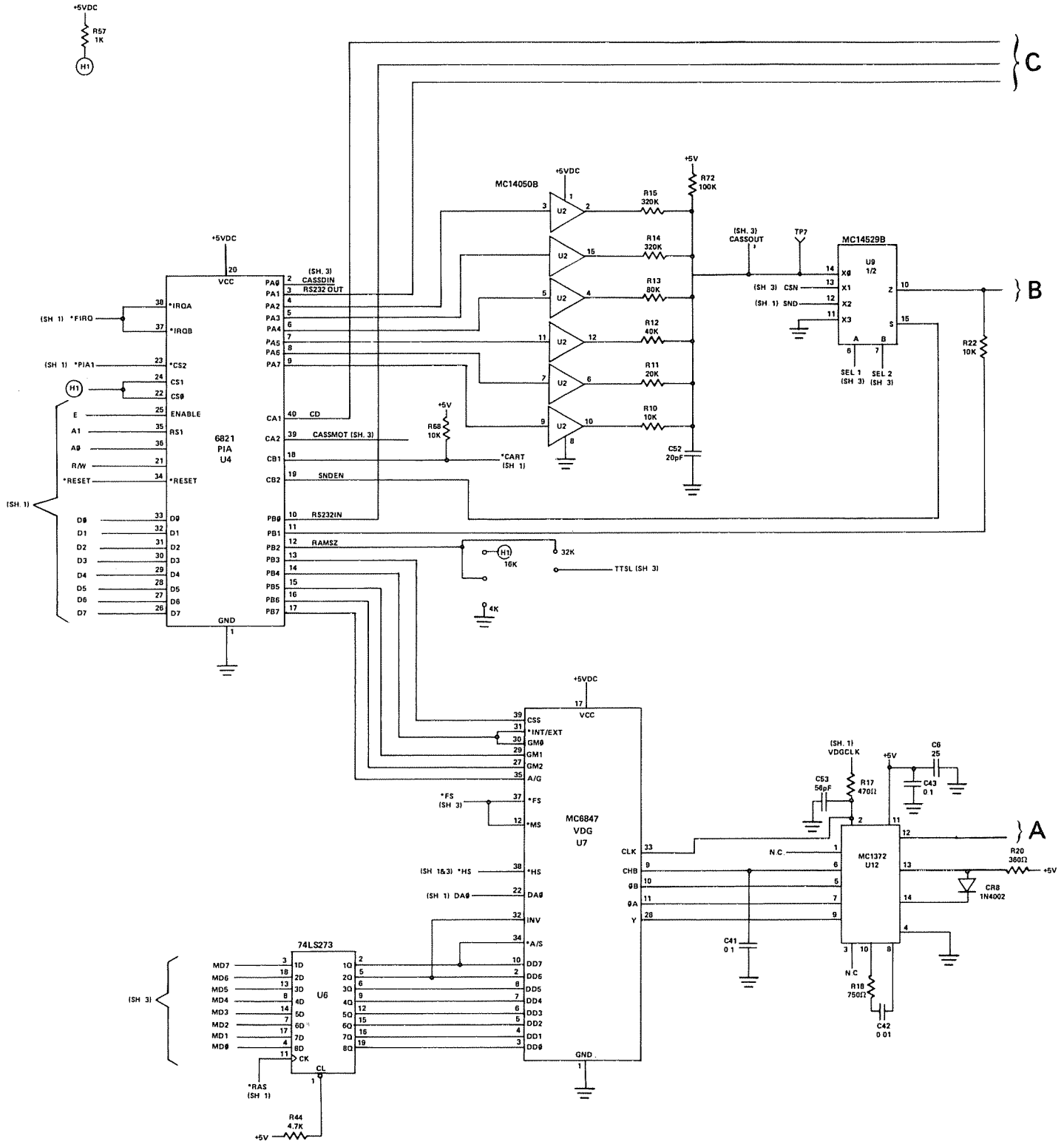
1 ON SOME BOARDS, THE FOLLOWING RESISTORS HAVE BEEN REPLACED WITH FERRITE BEADS:
R73, R74 R75 (5 beads) R76, R77, R78 R79 and R83

2 R83 IS USED ONLY ON 32K BOARDS

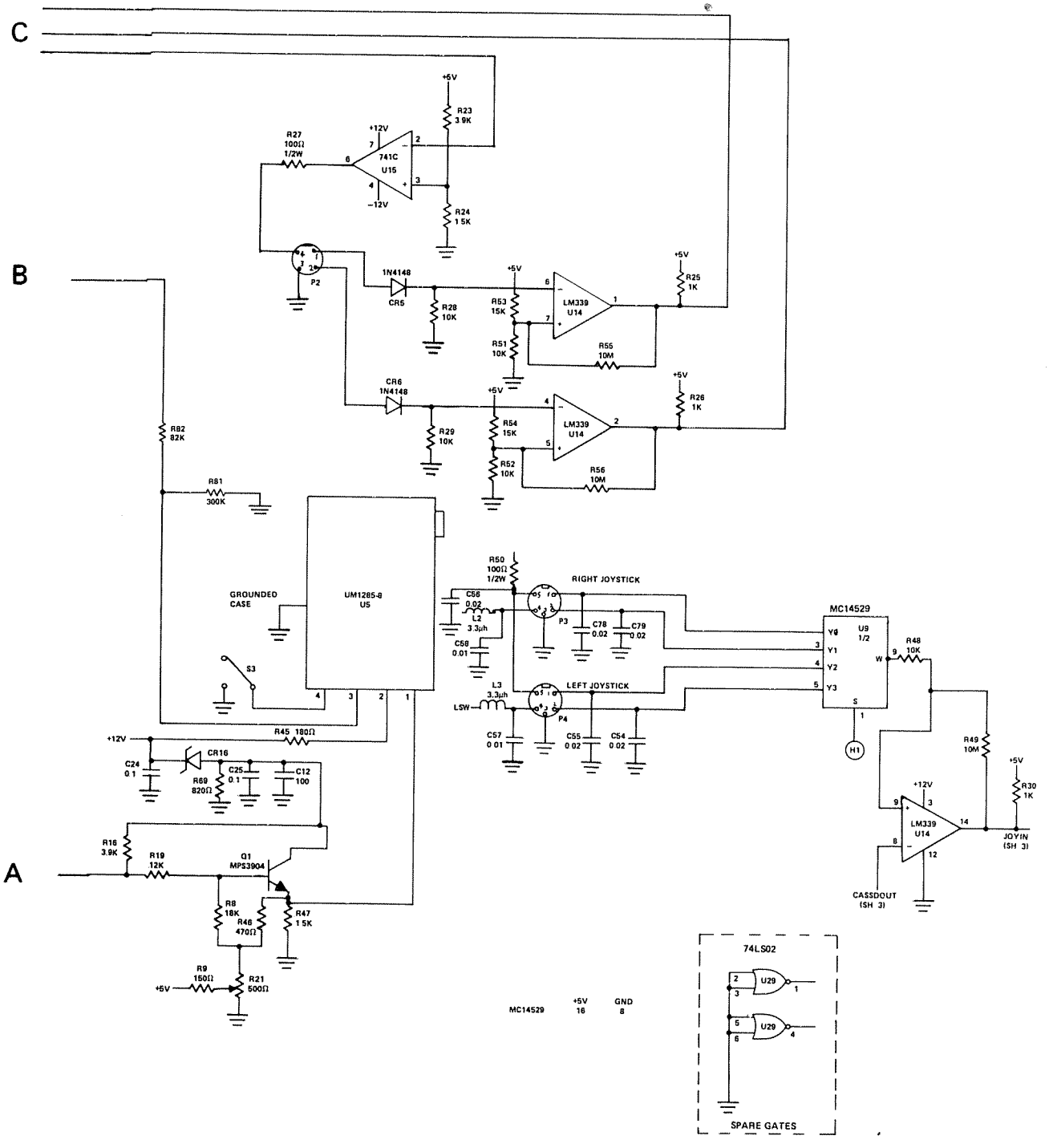
3 THE FOLLOWING CAPACITORS ARE DELETED FOR 32K:
C31 C35, C45, C48 C61 C64, C67, and C70

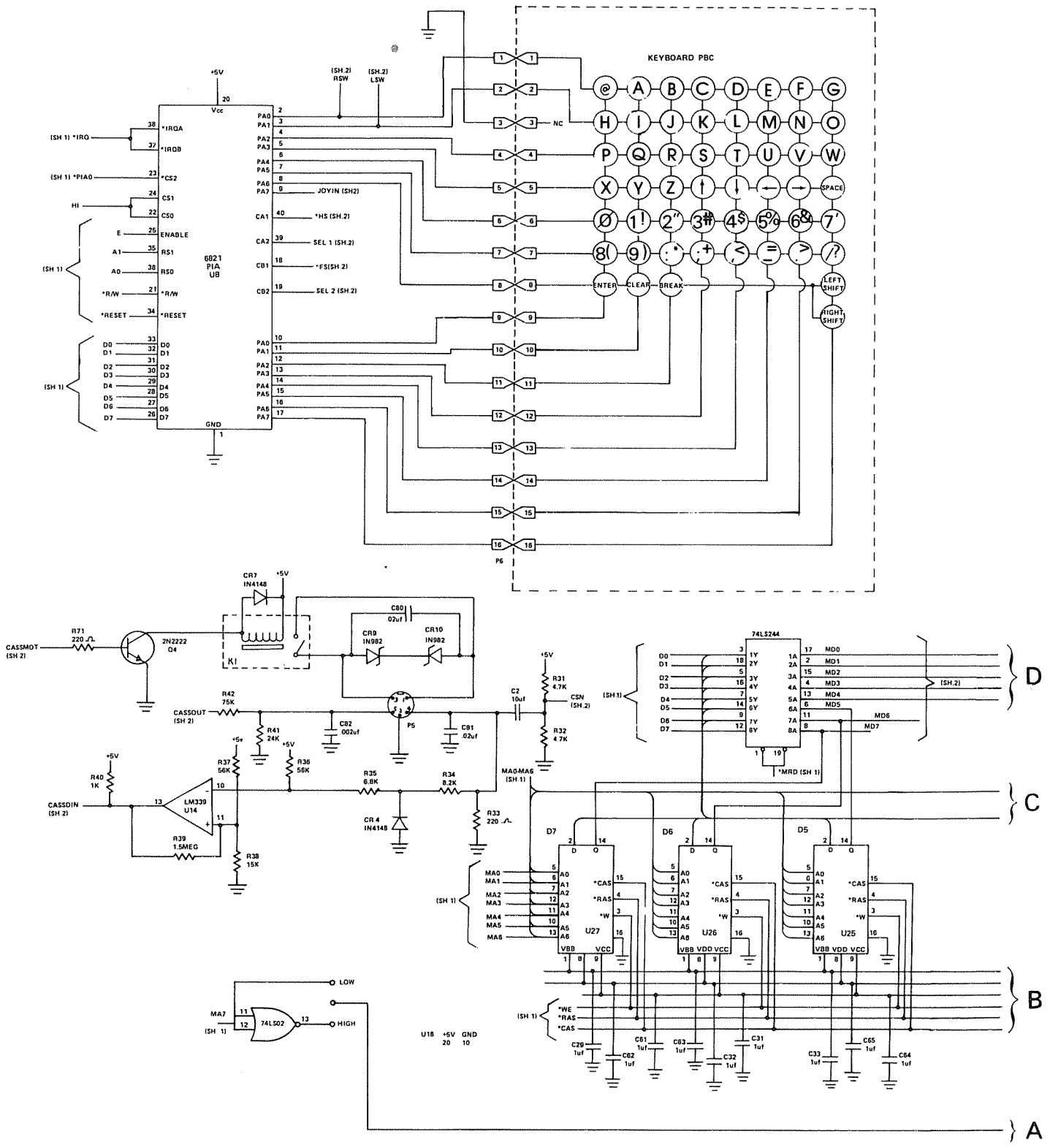
4 ON A 4K RAM, PIN 13 IS CS*

5 ON A 32K RAM, PIN 8 IS Vcc, PIN 1 IS N/C, AND PIN 9 IS A7

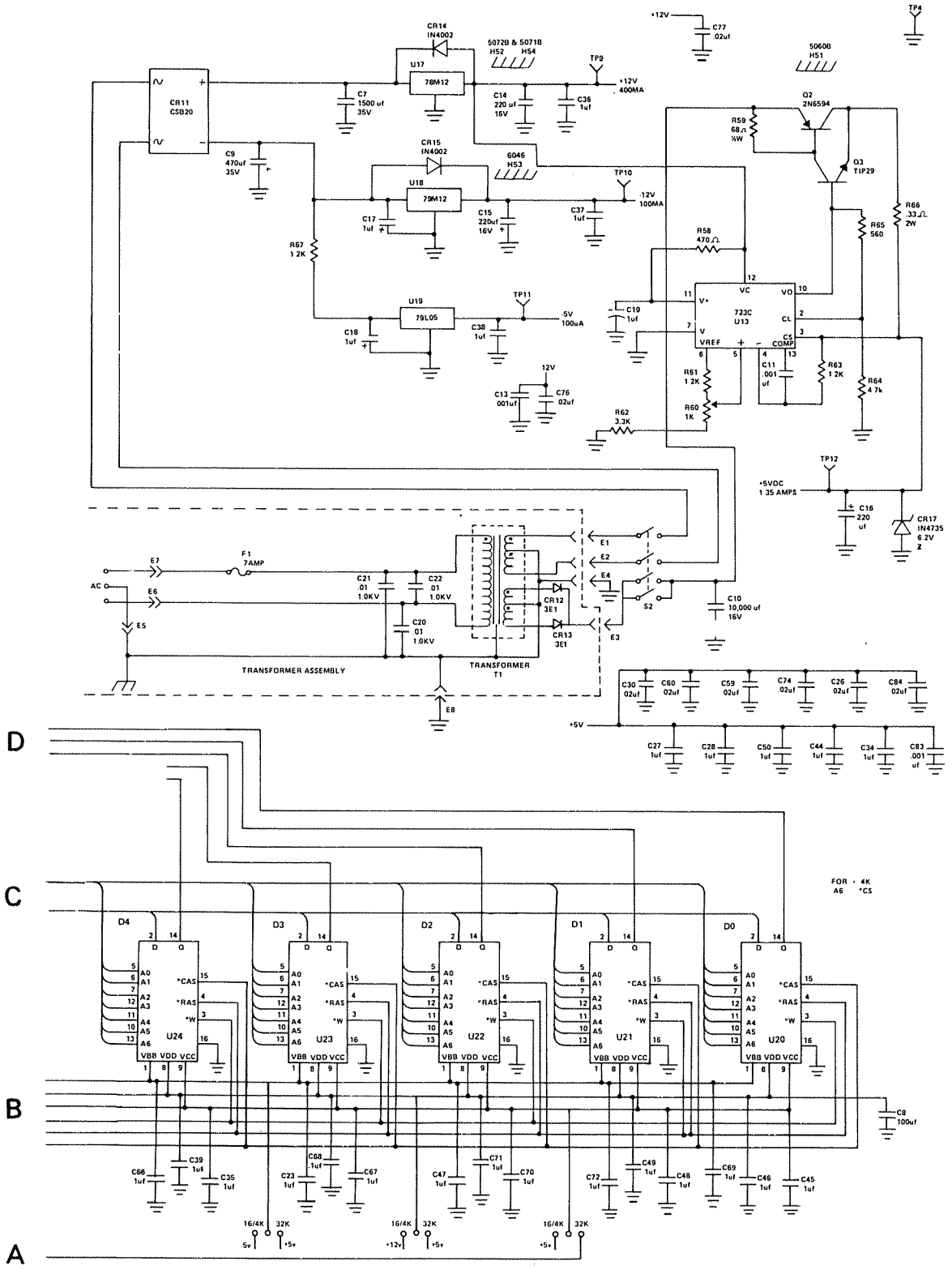


COLOR COMPUTER SCHEMATIC – SHEET 2


C
B
A
+5V
R23 3.9K
+12V
R27 100Ω 1/2W
741C U15
-12V
R24 1.5K
P2
1N4148
CR5
R28 10K
R53 15K
R51 10K
LM339 U14
R55 10M
R25 1K
CR6 1N4148
R29 10K
R54 15K
R52 10K
R56 10M
R26 1K
R82 82K
R81 300K
GROUNDED CASE
UM1285-8 U5
S3
R50 100Ω 1/2W
RIGHT JOYSTICK
C56 0.02
L2 3.3μh
C58 0.01
P3
C78 0.02
C79 0.02
L3 3.3μh
LSW
LEFT JOYSTICK
P4
C57 0.01
C55 0.02
C54 0.02
MC14529
U9 1/2
Y0
Y1
Y2
Y3
S
W
R48 10K
H1
R49 10M
R30 1K
JOYIN (SH 3)
CASSDOUT (SH 3)
R45 180Ω
C24 0.1
CR16
R69 820Ω
C25 0.1
C12 100
R16 3.9K
R19 12K
Q1 MPS3904
R8 18K
R46 470Ω
R47 1.5K
R9 150Ω
R21 500Ω
MC14529 +5V 16 GND 8
74LS02
U29
SPARE GATES



COLOR COMPUTER SCHEMATIC – SHEET 3


CR11 CSD20
CR14 IN4002
CR15 IN4002
U17 78M12
U18 79M12
U19 79L05
5072B & 5071B H52 H54
6046 H53
50608 H51
TP8 +12V 400MA
TP10 12V 100MA
TP11 5V 100uA
TP12 +5VDC 1.35 AMPS
TP4
Q2 2N6594
Q3 TIP29
723C U13
VC VO V+ CL V VREF CS COMP
C7 1500 uf 35V
C9 470uf 35V
C14 220 uf 16V
C15 220uf 16V
C17 1uf
C18 1uf
C36 1uf
C37 1uf
C38 1uf
C77 .02uf
C19 1uf
C11 .001 uf
C13 001uf
C76 02uf
C16 220 uf
CR17 IN4735 6.2V
R58 470Ω
R59 68Ω ½W
R60 1K
R61 1.2K
R62 3.3K
R63 1.2K
R64 4.7k
R65 560
R66 33Ω 2W
R67 1.2K
F1 7AMP
E1 E2 E3 E4 E5 E6 E7 E8
S2
C10 10,000 uf 16V
C20 .01 1.0KV
C21 .01 1.0KV
C22 .01 1.0KV
CR12 3E1
CR13 3E1
TRANSFORMER ASSEMBLY
TRANSFORMER T1
C30 02uf
C60 02uf
C59 02uf
C74 .02uf
C26 02uf
C84 02uf
C27 1uf
C28 1uf
C50 1uf
C44 1uf
C34 1uf
C83 .001 uf
+5V
D
C
B
A
D4 D3 D2 D1 D0
U24 U23 U22 U21 U20
D Q
A0 A1 A2 A3 A4 A5 A6
*CAS *RAS *W
VBB VDD VCC
C66 1uf
C39 1uf
C35 1uf
C68 .1uf
C23 1uf
C67 1uf
C47 1uf
C71 1uf
C70 1uf
C72 1uf
C49 1uf
C48 1uf
C69 1uf
C46 1uf
C45 1uf
C8 100uf
16/4K 32K
5v +5v
+12v +5v
FOR 4K A6 *CS

RADIO SHACK A DIVISION OF TANDY CORPORATION

U.S.A.
FORT WORTH, TEXAS 76102

CANADA
BARRIE, ONTARIO, L4M4W5

TANDY CORPORATION

AUSTRALIA
280-316 VICTORIA ROAD
RYDAMERE, N.S.W. 2116

BELGIUM
PARC INDUSTRIEL NANINNE
5140 NANINNE

UNITED KINGDOM
BILSTON ROAD, WEDNESBURY
WEST MIDLANDS WS10 7JN