MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

# MC6821

## NMOS
(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

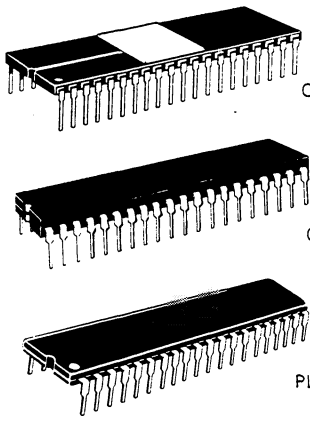
## PERIPHERAL INTERFACE ADAPTER

### PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the M6800 family of microprocessors. This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL-Compatible
- Static Operation

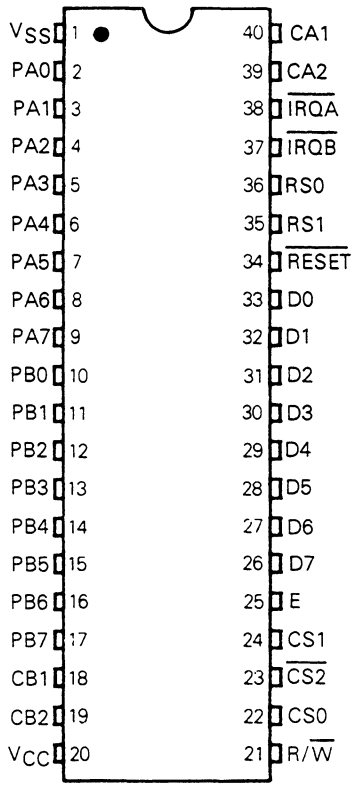


**L SUFFIX**
CERAMIC PACKAGE
CASE 715

**S SUFFIX**
CERDIP PACKAGE
CASE 734

**P SUFFIX**
PLASTIC PACKAGE
CASE 711

**PIN ASSIGNMENT**




### ORDERING INFORMATION

| Package Type | Frequency (MHz) | Temperature | Order Number |
|---|---|---|---|
| Ceramic L Suffix | 1.0 | 0°C to 70°C | MC6821L |
| | 1.0 | −40°C to 85°C | MC6821CL |
| | 1.5 | 0°C to 70°C | MC68A21L |
| | 1.5 | −40°C to 85°C | MC68A21CL |
| | 2.0 | 0°C to 70°C | MC68B21L |
| Cerdip S Suffix | 1.0 | 0°C to 70°C | MC6821S |
| | 1.0 | −40°C to 85°C | MC6821CS |
| | 1.5 | 0°C to 70°C | MC68A21S |
| | 1.5 | −40°C to 85°C | MC68A21CS |
| | 2.0 | 0°C to 70°C | MC68B21S |
| Plastic P Suffix | 1.0 | 0°C to 70°C | MC6821P |
| | 1.0 | −40°C to 85°C | MC6821CP |
| | 1.5 | 0°C to 70°C | MC68A21P |
| | 1.5 | −40°C to 85°C | MC68A21CP |
| | 2.0 | 0°C to 70°C | MC68B21P |

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## MAXIMUM RATINGS

| Characteristics | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | −0.3 to +7.0 | V |
| Input Voltage | $V_{in}$ | −0.3 to +7.0 | V |
| Operating Temperature Range<br>MC6821, MC68A21, MC68B21<br>MC6821C, MC68A21C | $T_A$ | $T_L$ to $T_H$<br>0 to 70<br>−40 to +85 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that $V_{in}$ and $V_{out}$ be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{CC}$).

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance<br>Ceramic<br>Plastic<br>Cerdip | $\theta_{JA}$ | <br>50<br>100<br>60 | °C/W |

## POWER CONSIDERATIONS

The average chip-junction temperature, $T_J$, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. $P_{PORT}$ may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between $P_D$ and $T_J$ (if $P_{PORT}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring $P_D$ (at equilibrium) for a known $T_A$. Using this value of K the values of $P_D$ and $T_J$ can be obtained by solving equations (1) and (2) iteratively for any value of $T_A$.

## DC ELECTRICAL CHARACTERISTICS ($V_{CC}$ = 5.0 Vdc ±5%, $V_{SS}$ = 0, $T_A = T_L$ to $T_H$ unless otherwise noted).

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **BUS CONTROL INPUTS (R/$\overline{W}$, Enable, $\overline{RESET}$, RS0, RS1, CS0, CS1, CS2)** | | | | | |
| Input High Voltage | $V_{IH}$ | $V_{SS}$+2.0 | – | $V_{CC}$ | V |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$−0.3 | – | $V_{SS}$+0.8 | V |
| Input Leakage Current ($V_{in}$ = 0 to 5.25 V) | $I_{in}$ | – | 1.0 | 2.5 | μA |
| Capacitance ($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | $C_{in}$ | – | – | 7.5 | pF |
| **INTERRUPT OUTPUTS ($\overline{IRQA}$, $\overline{IRQB}$)** | | | | | |
| Output Low Voltage ($I_{Load}$ = 3.2 mA) | $V_{OL}$ | – | – | $V_{SS}$+0.4 | V |
| Hi-Z Output Leakage Current | $I_{OZ}$ | – | 1.0 | 10 | μA |
| Capacitance ($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | $C_{out}$ | – | – | 5.0 | pF |
| **DATA BUS (D0-D7)** | | | | | |
| Input High Voltage | $V_{IH}$ | $V_{SS}$+2.0 | – | $V_{CC}$ | V |
| Input Low Voltage | $V_{IL}$ | $V_{SS}$−0.3 | – | $V_{SS}$+0.8 | V |
| Hi-Z Input Leakage Current ($V_{in}$ = 0.4 to 2.4 V) | $I_{IZ}$ | – | 2.0 | 10 | μA |
| Output High Voltage ($I_{Load}$ = −205 μA) | $V_{OH}$ | $V_{SS}$+2.4 | – | – | V |
| Output Low Voltage ($I_{Load}$ = 1.6 mA) | $V_{OL}$ | – | – | $V_{SS}$+0.4 | V |
| Capacitance ($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | $C_{in}$ | – | – | 12.5 | pF |

## DC ELECTRICAL CHARACTERISTICS (Continued)

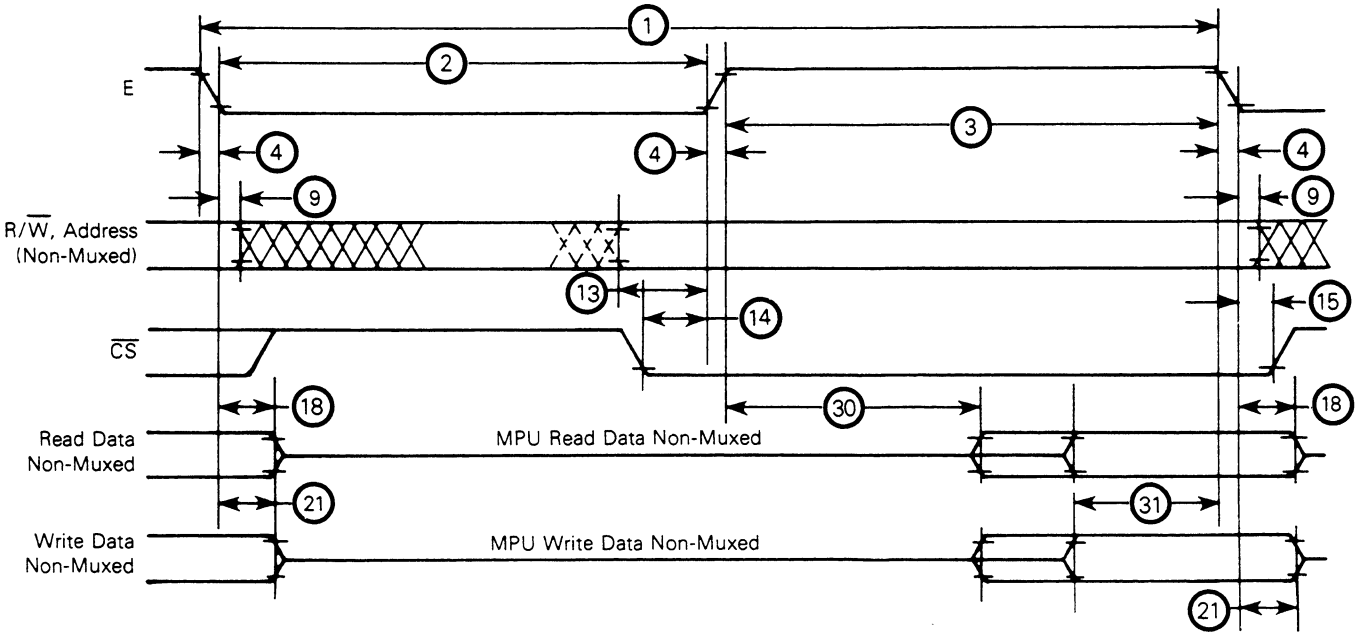
| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **PERIPHERAL BUS (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)** | | | | | | |
| Input Leakage Current ($V_{in}$ = 0 to 5.25 V) | R/$\overline{W}$, $\overline{RESET}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable | $I_{in}$ | – | 1.0 | 2.5 | μA |
| Hi-Z Input Leakage Current ($V_{in}$ = 0.4 to 2.4 V) | PB0-PB7, CB2 | $I_{IZ}$ | – | 2.0 | 10 | μA |
| Input High Current ($V_{IH}$ = 2.4 V) | PA0-PA7, CA2 | $I_{IH}$ | –200 | –400 | – | μA |
| Darlington Drive Current ($V_O$ = 1.5 V) | PB0-PB7, CB2 | $I_{OH}$ | –1.0 | – | –10 | mA |
| Input Low Current ($V_{IL}$ = 0.4 V) | PA0-PA7, CA2 | $I_{IL}$ | – | –1.3 | –2.4 | mA |
| Output High Voltage ($I_{Load}$ = –200 μA)<br>($I_{Load}$ = –10 μA) | PA0-PA7, PB0-PB7, CA2, CB2<br>PA0-PA7, CA2 | $V_{OH}$ | $V_{SS}$ + 2.4<br>$V_{CC}$ – 1.0 | –<br>– | –<br>– | V |
| Output Low Voltage ($I_{Load}$ = 3.2 mA) | | $V_{OL}$ | – | – | $V_{SS}$ + 0.4 | V |
| Capacitance ($V_{in}$ = 0, $T_A$ = 25°C, f = 1.0 MHz) | | $C_{in}$ | – | – | 10 | pF |
| **POWER REQUIREMENTS** | | | | | | |
| Internal Power Dissipation (Measured at $T_L$ = 0°C) | | $P_{INT}$ | – | – | 550 | mW |

## BUS TIMING CHARACTERISTICS (See Notes 1 and 2)

| Ident. Number | Characteristic | Symbol | MC6821 | | MC68A21 | | MC68B21 | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | Min | Max | |
| 1 | Cycle Time | $t_{cyc}$ | 1.0 | 10 | 0.67 | 10 | 0.5 | 10 | μs |
| 2 | Pulse Width, E Low | $PW_{EL}$ | 430 | – | 280 | – | 210 | – | ns |
| 3 | Pulse Width, E High | $PW_{EH}$ | 450 | – | 280 | – | 220 | – | ns |
| 4 | Clock Rise and Fall Time | $t_r$, $t_f$ | – | 25 | – | 25 | – | 20 | ns |
| 9 | Address Hold Time | $t_{AH}$ | 10 | – | 10 | – | 10 | – | ns |
| 13 | Address Setup Time Before E | $t_{AS}$ | 80 | – | 60 | – | 40 | – | ns |
| 14 | Chip Select Setup Time Before E | $t_{CS}$ | 80 | – | 60 | – | 40 | – | ns |
| 15 | Chip Select Hold Time | $t_{CH}$ | 10 | – | 10 | – | 10 | – | ns |
| 18 | Read Data Hold Time | $t_{DHR}$ | 20 | 50* | 20 | 50* | 20 | 50* | ns |
| 21 | Write Data Hold Time | $t_{DHW}$ | 10 | – | 10 | – | 10 | – | ns |
| 30 | Output Data Delay Time | $t_{DDR}$ | – | 290 | – | 180 | – | 150 | ns |
| 31 | Input Data Setup Time | $t_{DSW}$ | 165 | – | 80 | – | 60 | – | ns |

*The data bus output buffers are no longer sourcing or sinking current by $t_{DHR}$max (High Impedance).

**FIGURE 1 — BUS TIMING**




Notes:
1. Voltage levels shown are $V_L \leq 0.4$ V, $V_H \geq 2.4$ V, unless otherwise specified.
2. Measurement points shown are 0.8 V and 2.0 V, unless otherwise specified.

## PERIPHERAL TIMING CHARACTERISTICS ($V_{CC}$ = 5.0 V ±5%, $V_{SS}$ = 0 V, $T_A = T_L$ to $T_H$ unless otherwise specified)

| Characteristic | Symbol | MC6821 | | MC68A21 | | MC68B21 | | Unit | Reference Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| Data Setup Time | $t_{PDS}$ | 200 | – | 135 | – | 100 | – | ns | 6 |
| Data Hold Time | $t_{PDH}$ | 0 | – | 0 | – | 0 | – | ns | 6 |
| Delay Time, Enable Negative Transition to CA2 Negative Transition | $t_{CA2}$ | – | 1.0 | – | 0.670 | – | 0.500 | μs | 3, 7, 8 |
| Delay Time, Enable Negative Transition to CA2 Positive Transition | $T_{RS1}$ | – | 1.0 | – | 0.670 | – | 0.500 | μs | 3, 7 |
| Rise and Fall Times for CA1 and CA2 Input Signals | $t_r$, $t_f$ | – | 1.0 | – | 1.0 | – | 1.0 | μs | 8 |
| Delay Time from CA1 Active Transition to CA2 Positive Transition | $t_{RS2}$ | – | 2.0 | – | 1.35 | – | 1.0 | μs | 3, 8 |
| Delay Time, Enable Negative Transition to Data Valid | $t_{PDW}$ | – | 1.0 | – | 0.670 | – | 0.5 | μs | 3, 9, 10 |
| Delay Time, Enable Negative Transition to CMOS Data Valid PA0-PA7, CA2 | $t_{CMOS}$ | – | 2.0 | – | 1.35 | – | 1.0 | μs | 4, 9 |
| Delay Time, Enable Positive Transition to CB2 Negative Transition | $t_{CB2}$ | – | 1.0 | – | 0.670 | – | 0.5 | μs | 3, 11, 12 |
| Delay Time, Data Valid to CB2 Negative Transition | $t_{DC}$ | 20 | – | 20 | – | 20 | – | ns | 3, 10 |
| Delay Time, Enable Positive Transition to CB2 Positive Transition | $t_{RS1}$ | – | 1.0 | – | 0.670 | – | 0.5 | μs | 3, 11 |
| Control Output Pulse Width, CA2/CB2 | $PW_{CT}$ | 500 | – | 375 | – | 250 | – | ns | 3, 11 |
| Rise and Fall Time for CB1 and CB2 Input Signals | $t_r$, $t_f$ | – | 1.0 | – | 1.0 | – | 1.0 | μ | 12 |
| Delay Time, CB1 Active Transition to CB2 Positive Transition | $t_{RS2}$ | – | 2.0 | – | 1.35 | – | 1.0 | μs | 3, 12 |
| Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$ | $t_{IR}$ | – | 1.60 | – | 1.10 | – | 0.85 | μs | 5, 14 |
| Interrupt Response Time | $t_{RS3}$ | – | 1.0 | – | 1.0 | – | 1.0 | μs | 5, 13 |
| Interrupt Input Pulse Time | $PW_I$ | 500 | – | 500 | – | 500 | – | ns | 13 |
| $\overline{RESET}$ Low Time* | $t_{RL}$ | 1.0 | – | 0.66 | – | 0.5 | – | μs | 15 |

*The $\overline{RESET}$ line must be high a minimum of 1.0 μs before addressing the PIA.

FIGURE 2 — BUS TIMING TEST LOADS

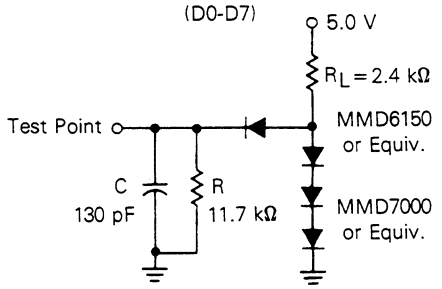



FIGURE 3 — TTL EQUIVALENT TEST LOAD

(PA0–PA7, PB0–PB7, CA2, CB2)

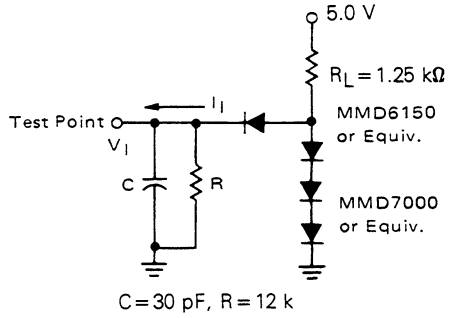



FIGURE 4 — CMOS EQUIVALENT TEST LOAD

(PA0-PA7, CA2)

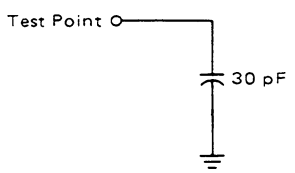



FIGURE 5 — NMOS EQUIVALENT TEST LOAD

($\overline{IRQ}$ Only)

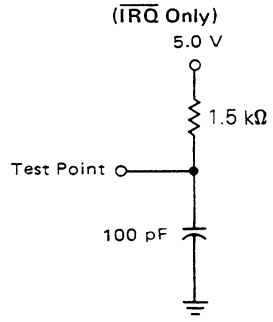


FIGURE 6 — PERIPHERAL DATA SETUP AND HOLD TIMES
(Read Mode)

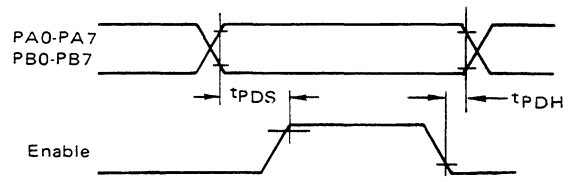
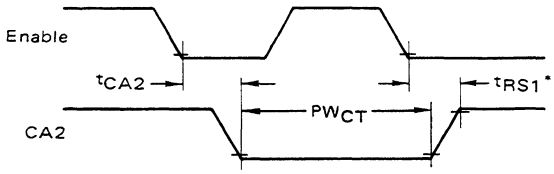



FIGURE 7 — CA2 DELAY TIME
(Read Mode; CRA-5=CRA3=1, CRA-4=0)




*Assumes part was deselected during the previous E pulse.

FIGURE 8 — CA2 DELAY TIME
(Read Mode; CRA-5=1, CRA-3=CRA-4=0)

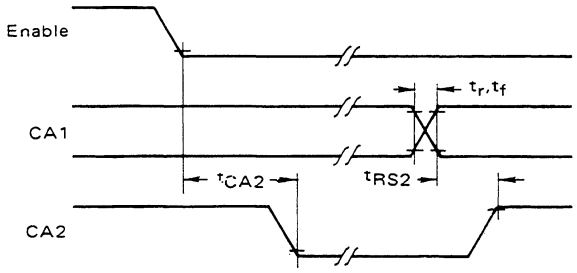



FIGURE 9 — PERIPHERAL CMOS DATA DELAY TIMES
(Write Mode; CRA-5=CRA-3=1, CRA-4=0)

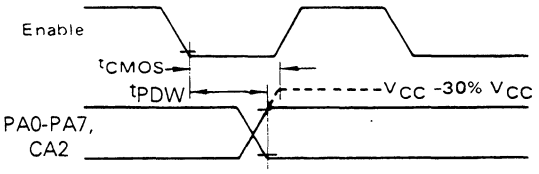
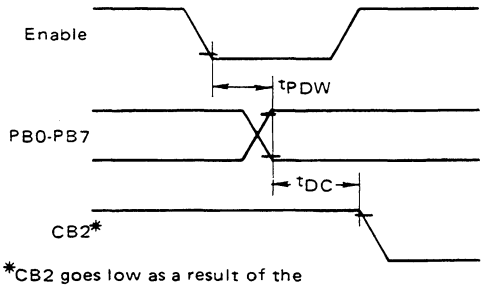
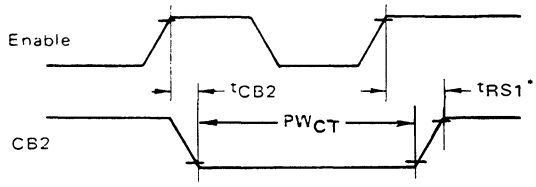



FIGURE 10 — PERIPHERAL DATA AND CB2 DELAY TIMES
(Write Mode; CRB-5=CRB-3=1, CRB-4=0)



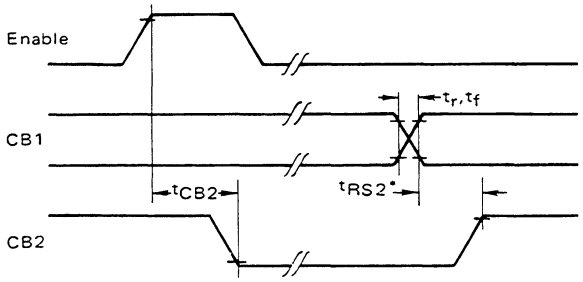

*CB2 goes low as a result of the positive transition of Enable.

FIGURE 11 — CB2 DELAY TIME
(Write Mode; CRB-5=CRB-3=1, CRB-4=0)



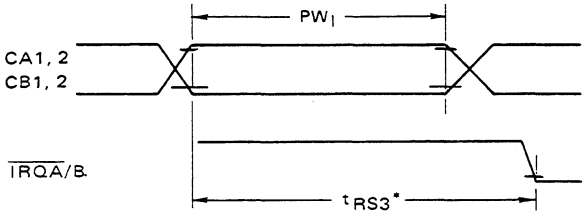

*Assumes part was deselected during the previous E pulse.

FIGURE 12 — CB2 DELAY TIME
(Write Mode; CRB-5=1, CRB-3=CRB-4=0)




*Assumes part was deselected during any previous E pulse.

FIGURE 13 — INTERRUPT PULSE WIDTH AND $\overline{IRQ}$ RESPONSE




*Assumes Interrupt Enable Bits are set.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 14 — $\overline{IRQ}$ RELEASE TIME

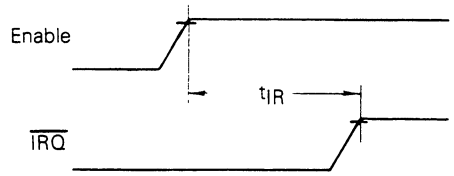
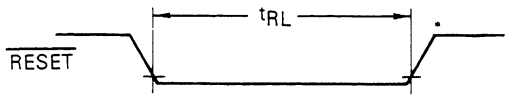


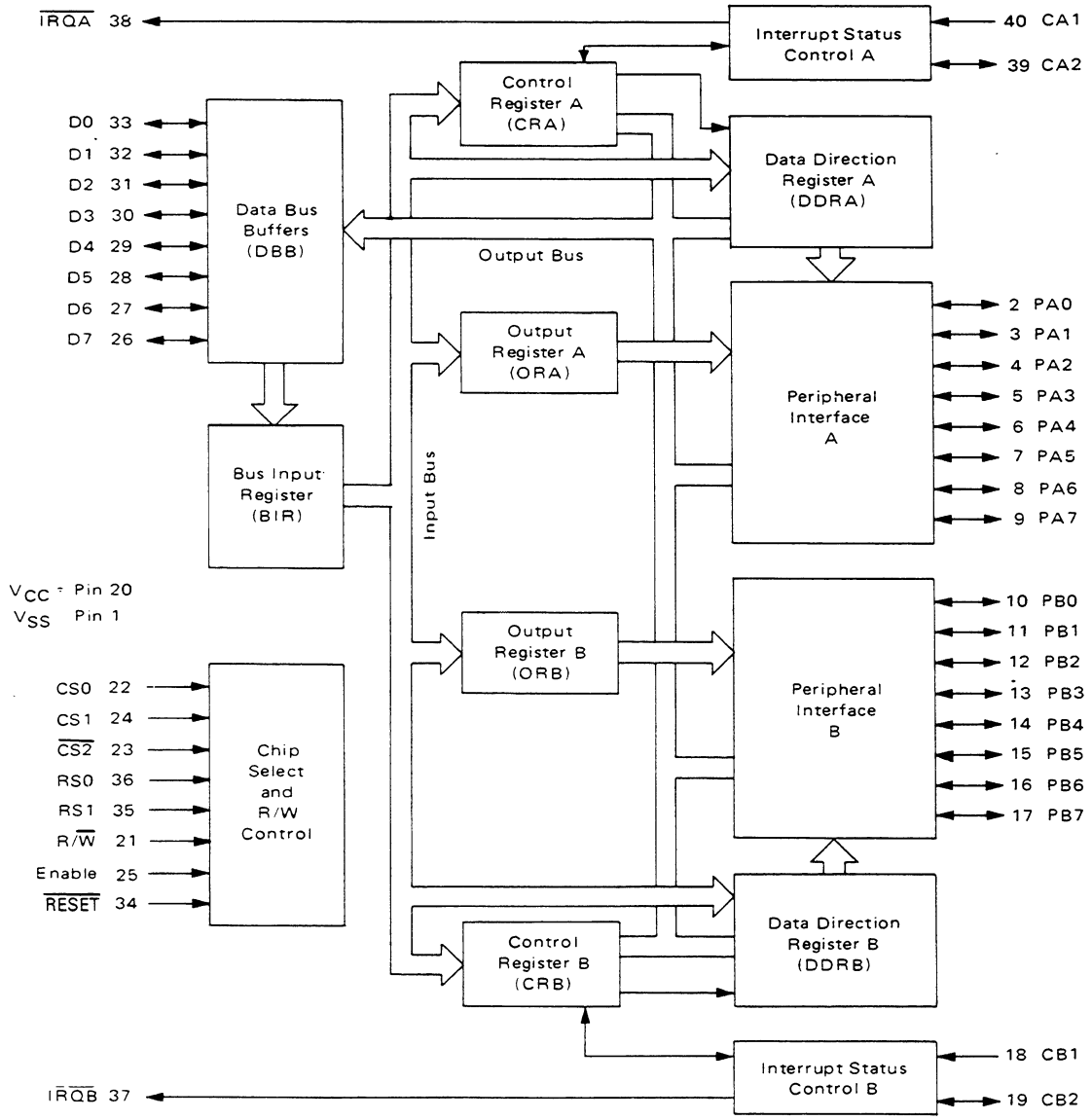

FIGURE 15 — $\overline{RESET}$ LOW TIME




*The $\overline{RESET}$ line must be a $V_{IH}$ for a minimum of 1.0 $\mu$s before addressing the PIA.

Note: Timing measurements are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, unless otherwise noted.

FIGURE 16 — EXPANDED BLOCK DIAGRAM



## PIA INTERFACE SIGNALS FOR MPU

The PIA interfaces to the M6800 bus with an 8-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, a read/write line, an enable line and a reset line. To ensure proper operation with the MC6800, MC6802, or MC6808 microprocessors, VMA should be used as an active part of the address decoding.

**Bidirectional Data (D0-D7)** — The bidirectional data lines (D0-D7) allow the transfer of data between the MPU and the PIA. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the MPU performs a PIA read operation. The read/write line is in the read (high) state when the PIA is selected for a read operation.

**Enable (E)** — The enable pulse, E, is the only timing signal that is supplied to the PIA. Timing of all other signals is referenced to the leading and trailing edges of the E pulse.

**Read/Write (R/$\overline{W}$)** — This signal is generated by the MPU to control the direction of data transfers on the data bus. A low state on the PIA read/write line enables the input buffers and data is transferred from the MPU to the PIA on the E signal if the device has been selected. A high on the read/write line sets up the PIA for a transfer of data to the bus. The PIA output buffers are enabled when the proper address and the enable pulse E are present.

**$\overline{RESET}$** — The active low $\overline{RESET}$ line is used to reset all register bits in the PIA to a logical zero (low). This line can be used as a power-on reset and as a master reset during system operation.

**Chip Selects (CS0, CS1, and $\overline{CS2}$)** — These three input signals are used to select the PIA. CS0 and CS1 must be high and $\overline{CS2}$ must be low for selection of the device. Data transfers are then performed under the control of the enable and read/write signals. The chip select lines must be stable for the duration of the E pulse. The device is deselected when any of the chip selects are in the inactive state.

**Register Selects (RS0 and RS1)** — The two register select lines are used to select the various registers inside the PIA. These two lines are used in conjunction with internal Control Registers to select a particular register that is to be written or read.

The register and chip select lines should be stable for the duration of the E pulse while in the read or write cycle.

**Interrupt Request ($\overline{IRQA}$ and $\overline{IRQB}$)** — The active low Interrupt Request lines ($\overline{IRQA}$ and $\overline{IRQB}$) act to interrupt the MPU either directly or through interrupt priority circuitry. These lines are "open drain" (no load device on the chip). This permits all interrupt request lines to be tied together in a wire-OR configuration.

Each Interrupt Request line has two internal interrupt flag bits that can cause the Interrupt Request line to go low. Each flag bit is associated with a particular peripheral interrupt line. Also, four interrupt enable bits are provided in the PIA which may be used to inhibit a particular interrupt from a peripheral device.

Servicing an interrupt by the MPU may be accomplished by a software routine that, on a prioritized basis, sequentially reads and tests the two control registers in each PIA for interrupt flag bits that are set.

The interrupt flags are cleared (zeroed) as a result of an MPU Read Peripheral Data Operation of the corresponding data register. After being cleared, the interrupt flag bit cannot be enabled to be set until the PIA is deselected during an E pulse. The E pulse is used to condition the interrupt control lines (CA1, CA2, CB1, CB2). When these lines are used as interrupt inputs, at least one E pulse must occur from the inactive edge to the active edge of the interrupt input signal to condition the edge sense network. If the interrupt flag has been enabled and the edge sense circuit has been properly conditioned, the interrupt flag will be set on the next active transition of the interrupt input pin.

## PIA PERIPHERAL INTERFACE LINES

The PIA provides two 8-bit bidirectional data buses and four interrupt/control lines for interfacing to peripheral devices.

**Section A Peripheral Data (PA0-PA7)** — Each of the peripheral data lines can be programmed to act as an input or output. This is accomplished by setting a "1" in the corresponding Data Direction Register bit for those lines which are to be outputs. A "0" in a bit of the Data Direction Register causes the corresponding peripheral data line to act as an input. During an MPU Read Peripheral Data Operation, the data on peripheral lines programmed to act as inputs appears directly on the corresponding MPU Data Bus lines. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

The data in Output Register A will appear on the data lines that are programmed to be outputs. A logical "1" written into the register will cause a "high" on the corresponding data line while a "0" results in a "low." Data in Output Register A may be read by an MPU "Read Peripheral Data A" operation when the corresponding lines are programmed as outputs. This data will be read properly if the voltage on the peripheral data lines is greater than 2.0 volts for a logic "1" output and less than 0.8 volt for a logic "0" output. Loading the output lines such that the voltage on these lines does not reach full voltage causes the data transferred into the MPU on a Read operation to differ from that contained in the respective bit of Output Register A.

**Section B Peripheral Data (PB0-PB7)** — The peripheral data lines in the B Section of the PIA can be programmed to act as either inputs or outputs in a similar manner to PA0-PA7. They have three-state capabiity, allowing them to enter a high-impedance state when the peripheral data line is used as an input. In addition, data on the peripheral data lines

PB0-PB7 will be read properly from those lines programmed as outputs even if the voltages are below 2.0 volts for a "high" or above 0.8 V for a "low". As outputs, these lines are compatible with standard TTL and may also be used as a source of at least 1 milliampere at 1.5 volts to directly drive the base of a transistor switch.

**Interrupt Input (CA1 and CB1)** — Peripheral input lines CA1 and CB1 are input only lines that set the interrupt flags of the control registers. The active transition for these signals is also programmed by the two control registers.

**Peripheral Control (CA2)** — The peripheral control line CA2 can be programmed to act as an interrupt input or as a peripheral control output. As an output, this line is compatible with standard TTL; as an input the internal pullup resistor on this line represents 1.5 standard TTL loads. The function of this signal line is programmed with Control Register A.

**Peripheral Control (CB2)** — Peripheral Control line CB2 may also be programmed to act as an interrupt input or peripheral control output. As an input, this line has high input impedance and is compatible with standard TTL. As an output it is compatible with standard TTL and may also be used as a source of up to 1 milliampere at 1.5 volts to directly drive the base of a transistor switch. This line is programmed by Control Register B.

## INTERNAL CONTROLS

### INITIALIZATION

A $\overline{\text{RESET}}$ has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

Details of possible configurations of the Data Direction and Control Register are as follows:

TABLE 1 — INTERNAL ADDRESSING

| | | Control Register Bit | | |
|---|---|---|---|---|
| RS1 | RS0 | CRA-2 | CRB-2 | Location Selected |
| 0 | 0 | 1 | X | Peripheral Register A |
| 0 | 0 | 0 | X | Data Direction Register A |
| 0 | 1 | X | X | Control Register A |
| 1 | 0 | X | 1 | Peripheral Register B |
| 1 | 0 | X | 0 | Data Direction Register B |
| 1 | 1 | X | X | Control Register B |

X = Don't Care

### PORT A-B HARDWARE CHARACTERISTICS

As shown in Figure 17, the MC6821 has a pair of I/O ports whose characteristics differ greatly. The A side is designed to drive CMOS logic to normal 30% to 70% levels, and incorporates an internal pullup device that remains connected even in the input mode. Because of this, the A side requires more drive current in the input mode than Port B. In contrast, the B side uses a normal three-state NMOS buffer which cannot pullup to CMOS levels without external resistors. The B side can drive extra loads such as Darlingtons without problem. When the PIA comes out of reset, the A port represents inputs with pullup resistors, whereas the B side (input mode also) will float high or low, depending upon the load connected to it.

Notice the differences between a Port A and Port B read operation when in the output mode. When reading Port A, the actual pin is read, whereas the B side read comes from an output latch, ahead of the actual pin.

### CONTROL REGISTERS (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines CA1, CA2, CB1, and CB2. In addition they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1, or CB2. The format of the control words is shown in Figure 18.

### DATA DIRECTION ACCESS CONTROL BIT (CRA-2 and CRB-2)

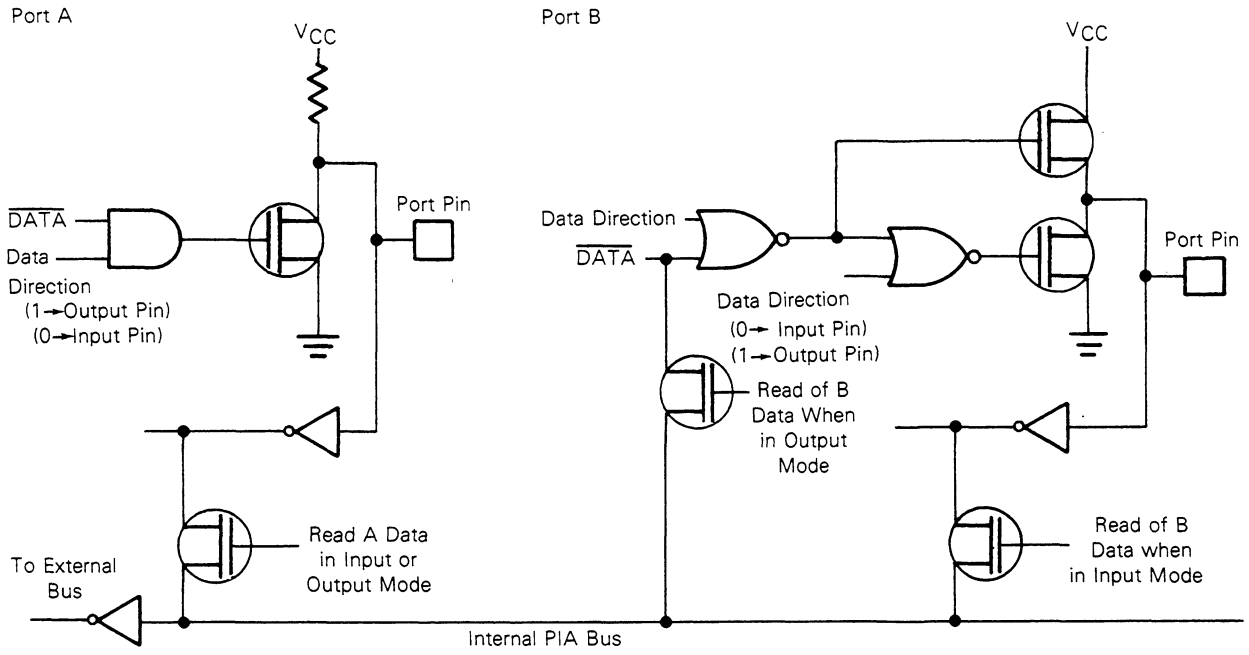
Bit 2, in each Control Register (CRA and CRB), determines selection of either a Peripheral Output Register or the corresponding Data Direction E Register when the proper register select signals are applied to RS0 and RS1. A "1" in bit 2 allows access of the Peripheral Interface Register, while a "0" causes the Data Direction Register to be addressed.

**Interrupt Flags (CRA-6, CRA-7, CRB-6, and CRB-7)** — The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Control lines when those lines are programmed to be inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

**Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4, and CRB-5)** — Bits 3, 4, and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CRB-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different loading characteristics.

**Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1, and CRB-1)** — The two lowest-order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1.

FIGURE 17 — PORT A AND PORT B EQUIVALENT CIRCUITS




ORDERING INFORMATION

MC68A21CP

- Motorola Integrated Circuit
- M6800 Family
- Blanks = 1.0 MHz
- A = 1.5 MHz
- B = 2.0 MHz
- Device Designation In M6800 Family
- Temperature Range
  - Blank = 0° → +70°C
  - C = −40° → +85°C
- Package
  - P = Plastic
  - S = Cerdip
  - L = Ceramic

BETTER PROGRAM

Better program processing is available on all types listed. Add suffix letters to part number.

Level 1 add "S" Level 2 add "D" Level 3 add "DS"

Level 1 "S" = 10 Temp Cycles — (−25 to 150°C); Hi Temp testing at $T_A$ max.
Level 2 "D" = 168 Hour Burn-in at 125°C
Level 3 "DS" = Combination of Level 1 and 2.

FIGURE 18 — CONTROL WORD FORMAT

**Determine Active CA1 (CB1) Transition for Setting Interrupt Flag IRQA(B)1 — (bit 7)**

b1=0: IRQA(B)1 set by high-to-low transition on CA1 (CB1)

b1=1: IRQA(B)1 set by low-to-high transition on CA1 (CB1).

**CA1 (CB1) Interrupt Request Enable/Disable**

b0=0: Disables IRQA(B) MPU Interrupt by CA1 (CB1) active transition.[1]

b0=1: Enable IRQA(B) MPU Interrupt by CA1 (CB1) active transition.

1. IRQA(B) will occur on next (MPU generated) positive transition of b0 if CA1 (CB1) active transition occurred while interrupt was disabled.

**IRQA(B) 1 Interrupt Flag (bit 7)**

Goes high on active transition of CA1 (CB1); Automatically cleared by MPU Read of Output Register A(B). May also be cleared by hardware Reset.

Control Register

| b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|
| IRQA(B)1 Flag | IRQA(B)2 Flag | CA2 (CB2) Control | | | DDR Access | CA1 (CB1) Control | |

**IRQA(B)2 Interrupt Flag (bit 6)**

When CA2 (CB2) is an input, IRQA(B) goes high on active transition CA2 (CB2); Automatically cleared by MPU Read of Output Register A(B). May also be cleared by hardware Reset.

CA2 (CB2) Established as Output (b5=1): IRQA(B) 2=0, not affected by CA2 (CB2) transitions.

**Determines Whether Data Direction Register Or Output Register is Addressed**

b2=0: Data Direction Register selected.

b2=1: Output Register selected.

**CA2 (CB2) Established as Output by b5=1**

(Note that operation of CA2 and CB2 output functions are not identical)

b5 b4 b3

1 0 → CA2

b3=0: **Read Strobe with CA1 Restore**
CA2 goes low on first high-to-low E transition following an MPU read of Output Register A; returned high by next active CA1 transition, as specified by bit 1.

b3=1: **Read Strobe with E Restore**
CA2 goes low on first high-to-low E transition following an MPU read of Output Register A; returned high by next high-to-low E transition during a deselect.

→ CB2

b3=0: **Write Strobe with CB1 Restore**
CB2 goes low on first low-to-high E transition following an MPU write into Output Register B; returned high by the next active CB1 transition as specified by bit 1. CRB-b7 must first be cleared by a read of data.

b3=1: **Write Strobe with E Restore**
CB2 goes low on first low-to-high E transition following an MPU write into Output Register B; returned high by the next low-to-high E transition following an E pulse which occurred while the part was deselected.

b5 b4 b3

1 1 → **Set/Reset CA2 (CB2)**

CA2 (CB2) goes low as MPU writes b3=0 into Control Register.

CA2 (CB2) goes high as MPU writes b3=1 into Control Register.

**CA2 (CB2) Established as Input by b5=0**

b5 b4 b3

0 → **CA2 (CB2) Interrupt Request Enable/Disable**

b3=0: Disables IRQA(B) MPU Interrupt by CA2 (CB2) active transition.*

b3=1: Enables IRQA(B) MPU Interrupt by CA2 (CB2) active transition.

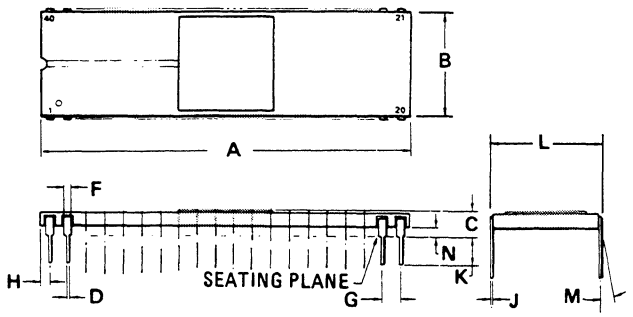
*IRQA(B) will occur on next (MPU generated) positive transition of b3 if CA2 (CB2) active transition occurred while interrupt was disabled.

→ **Determines Active CA2 (CB2) Transition for Setting Interrupt Flag IRQA(B)2 — (Bit b6)**

b4=0: IRQA(B)2 set by high-to-low transition on CA2 (CB2).

b4=1: IRQA(B)2 set by low-to-high transition on CA2 (CB2).

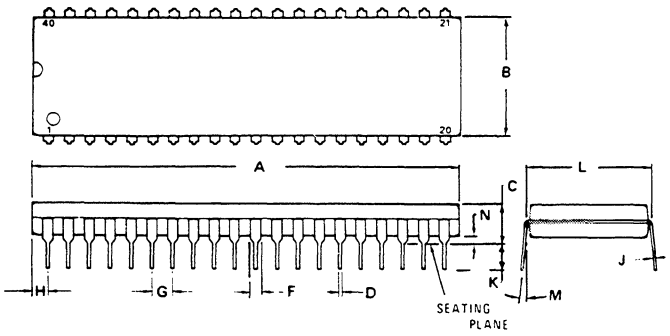
## PACKAGE DIMENSIONS




**L SUFFIX**
CERAMIC PACKAGE
CASE 715-04

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 50.29 | 51.31 | 1.980 | 2.020 |
| B | 14.94 | 15.34 | 0.588 | 0.604 |
| C | 3.05 | 4.06 | 0.120 | 0.160 |
| D | 0.38 | 0.53 | 0.015 | 0.021 |
| F | 0.76 | 1.40 | 0.030 | 0.055 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 0.76 | 1.78 | 0.030 | 0.070 |
| J | 0.20 | 0.33 | 0.008 | 0.013 |
| K | 2.54 | 4.19 | 0.100 | 0.165 |
| L | 14.99 | 15.49 | 0.590 | 0.610 |
| M | – | 10° | – | 10° |
| N | 1.02 | 1.52 | 0.040 | 0.060 |

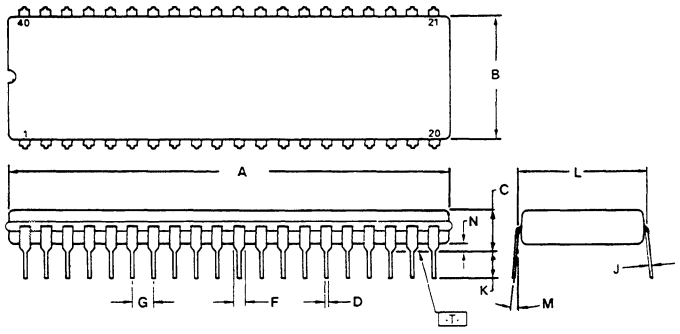
NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA (AT SEATING PLANE), AT MAX MAT'L CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.




**P SUFFIX**
PLASTIC PACKAGE
CASE 711-03

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 51.69 | 52.45 | 2.035 | 2.065 |
| B | 13.72 | 14.22 | 0.540 | 0.560 |
| C | 3.94 | 5.08 | 0.155 | 0.200 |
| D | 0.36 | 0.56 | 0.014 | 0.022 |
| F | 1.02 | 1.52 | 0.040 | 0.060 |
| G | 2.54 BSC | | 0.100 BSC | |
| H | 1.65 | 2.16 | 0.065 | 0.085 |
| J | 0.20 | 0.38 | 0.008 | 0.015 |
| K | 2.92 | 3.43 | 0.115 | 0.135 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.51 | 1.02 | 0.020 | 0.040 |

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.




**S SUFFIX**
CERDIP PACKAGE
CASE 734-03

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 51.31 | 53.24 | 2.020 | 2.096 |
| B | 12.70 | 15.49 | 0.500 | 0.610 |
| C | 4.06 | 5.84 | 0.160 | 0.230 |
| D | 0.38 | 0.56 | 0.015 | 0.022 |
| F | 1.27 | 1.65 | 0.050 | 0.065 |
| G | 2.54 BSC | | 0.100 BSC | |
| J | 0.20 | 0.30 | 0.008 | 0.012 |
| K | 3.18 | 4.06 | 0.125 | 0.160 |
| L | 15.24 BSC | | 0.600 BSC | |
| M | 5° | 15° | 5° | 15° |
| N | 0.51 | 1.27 | 0.020 | 0.050 |

NOTES:
1. DIMENSION-A-IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSION A AND B INCLUDES MENISCUS.

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MC6821/D

