S1985

MSX-SYSTEM II

APPLICATION MANUAL

— YAMAHA CORPORATION —

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1. MSX-SYSTEM II

Overview

The Yamaha S1985 is an LSI device designed for use with MSX2 computers. It is capable of memory control with expansion according to MSX2 specifications taken into account, and control of peripheral equipment such as a VDP, keyboard, printer, etc. It also has a built-in SSG for generation of music signals and a clock.

Features

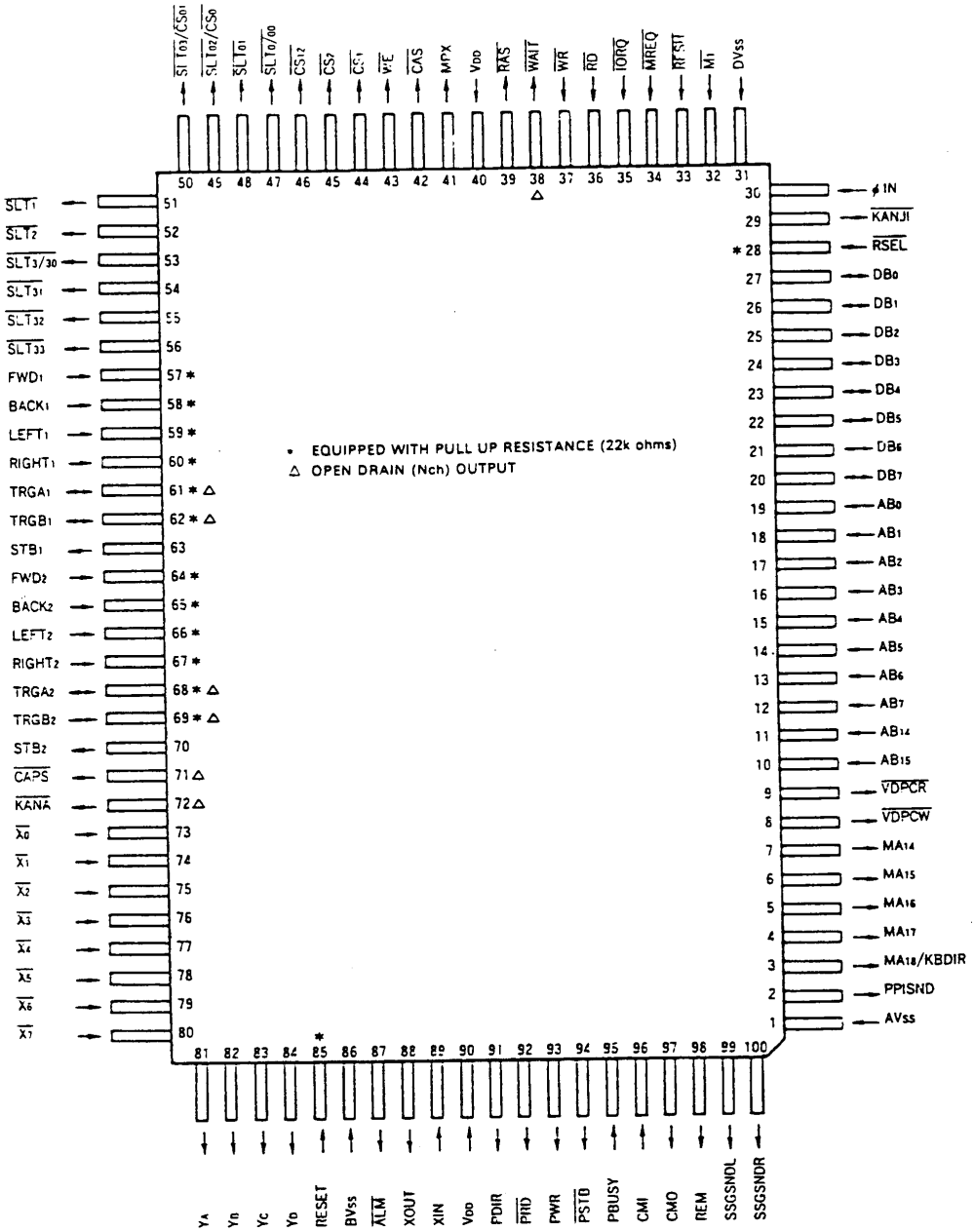
Slot control can be expanded to slots 0 and 3
Mapper function allowing memory expansion up to 512K bytes
Built-in MSX2 standard clock functions
16 byte (8 bit) back-up RAM
Registers for foreground and background color reading as bit mapped functions
DRAM refresh can be selected as RAS only refresh and hidden refresh
VDP select signal output
Keyboard access
Two built-in joystick port
Built-in SSG (Yamaha YM2149 equivalent)

Voicing range	: 8 octaves
Voicing systems	: 3 sine waves voicing systems and 1 noise voicing system
Envelope control	: 5 bit
D-A convertor	: 5 bit

Bi-directional printer mode
CMOS device with Si gates
100 pin flat plastic package

2. Functional Overview

Pin layout

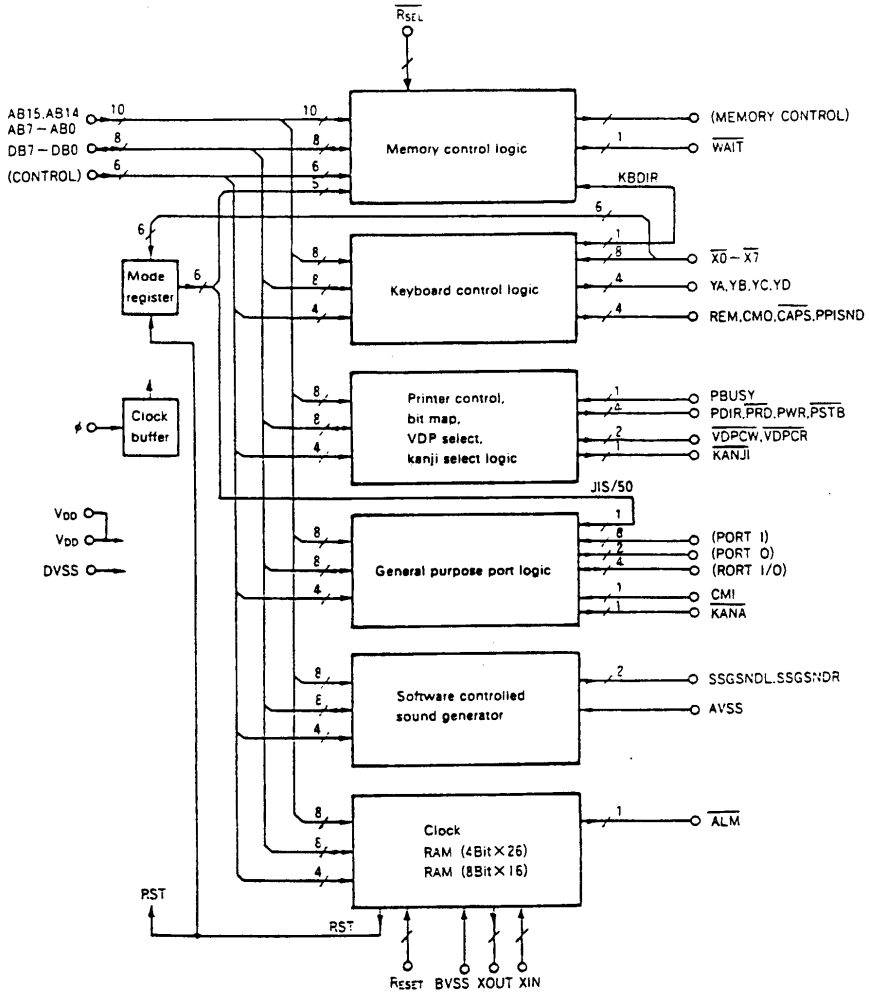


Pin functions

Pin name	I/O	Function
AB15, AB14, AB7~AB0	i	Address bus input (10 bits) for Z80A CPU
DB7~DB0	i/o	Data bus input/output (8 bits) for Z80A CPU
$\overline{M1}$	i	$\overline{M1}$ input for Z80A CPU
$\overline{RFSH}$	i	$\overline{RFSH}$ input for Z80A CPU
$\overline{MREQ}$	i	$\overline{MREQ}$ input for Z80A CPU
$\overline{IORQ}$	i	$\overline{IORQ}$ input for Z80A CPU
$\overline{RD}$	i	$\overline{RD}$ input for Z80A CPU
$\overline{WR}$	i	$\overline{WR}$ input for Z80A CPU
$\overline{WAIT}$	o	$\overline{WAIT}$ signal output to Z80A CPU (can have wired logic)
MPX	o	Multiplex signal output for DRAM address
$\overline{RAS}$	o	DRAMS $\overline{RAS}$ signal output
$\overline{CAS}$	o	DRAMS $\overline{CAS}$ signal output
$\overline{WE}$	o	DRAM $\overline{WE}$ signal output
$\overline{SLT33}$	o	Slot # 33 select signal output
$\overline{SLT32}$	o	Slot # 32 select signal output
$\overline{SLT31}$	o	Slot # 31 select signal output
$\overline{SLT3/30}$	o	Slot # 3 or 30 select signal output
$\overline{SLT2}$	o	Slot # 2 select signal output
$\overline{SLT1}$	o	Slot # 1 select signal output
$\overline{SLT03/CS01}$	o	Slot # 03 select or ROM select 0000H~7FFFH signal output
$\overline{SLT02/CS0}$	o	Slot # 02 select or ROM select 0000H~3FFFH signal output
$\overline{SLT01}$	o	Slot # 01 select signal output
$\overline{SLT0/00}$	o	Slot # 0 or 00 select signal output
$\overline{CS2}$	o	ROM select 8000H~BFFFH signal output
$\overline{CS1}$	o	ROM select 4000H~7FFFH signal output
$\overline{CS12}$	o	ROM select 4000H~BFFFH signal output
MA18/KBDIR	o	Mapper address or keyboard bus direction signal output
MA17~14	o	Mapper address address signal output
YD~YA	o	Keyboard drive signal input
$\overline{X7}$~$\overline{X0}$	i	Keyboard return signal input
$\overline{CAPS}$	o	Caps LED signal output
$\overline{KANA}$	o	Kana LED signal output
CMI	i	Cassette read signal input
CMO	o	Cassette write signal output
REM	o	Cassette control signal output
PBUSY	i	Printer busy signal input
$\overline{PSTB}$	o	Printer strobe signal output
PWR	o	Printer write signal output
$\overline{PRD}$	o	Printer read signal output
PDIR	o	Printer direction signal output
FWD1, FWD2	i	Joystick FWD signal input (general purpose port input)
BACK1, BACK2	i	Joystick BACK signal input (general purpose port input)

LEFT1, LEFT2	i	Joystick LEFT signal input (general purpose port input)
RIGHT1, RIGHT2	i	Joystick RIGHT signal input (general purpose port input)
TRGA1, TRGA2	i/o	Joystick TRGA signal input/output (general purpose port input/output)
TRGB1, TRGB2	i/o	Joystick TRGB signal input/output (general purpose port input/output)
STB1, STB2	o	General purpose port output
$\overline{\text{VDPSW}}$	o	VDP write signal output
$\overline{\text{VDPCR}}$	o	VDP read signal output
$\overline{\text{KANJI}}$	o	Kanji ROM select signal output
$\overline{\text{RSEL}}$	i	Signal input for expansion slot designation register control
RESET	i	Reset signal input
PPISND	o	PPI sound signal output
SSGSNDL	o	SSG sound LEFT signal output
SSGSNDR	o	SSG sound RIGHT signal output
ø	i	Clock signal input
VDD		+5V
DVSS		0^{V} (GND)
AVSS		GND for sound generation
XIN	i	Input from clock crystal
XOUT	o	Output to clock crystal
$\overline{\text{ALM}}$	o	Alarm signal output
BVSS		Power supply for clock back-up

Block diagram



(CONTROL) :$\overline{MI}$, $\overline{RFSH}$, $\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$, $\overline{WR}$

(MEMORY CONTROL): $\overline{RAS}$, MPX, $\overline{CAS}$, $\overline{WE}$, $\overline{CS1}$, $\overline{CS2}$, $\overline{CS12}$, $\overline{SLT0/00}$, $\overline{SLT01}$, $\overline{SLT02/CS0}$, $\overline{SLT03/CS01}$, $\overline{SLT1}$, $\overline{SLT30/30}$, $\overline{SLT2}$, $\overline{SLT31}$, $\overline{SLT32}$, $\overline{SLT33}$, MA14, MA15, MA16, MA17, MA18/KBDIR

(PORTI) :FWD1, FWD2, BACK1, BACK2, LEFT1, LEFT2, RIGHT1, RIGHT2.

(PORTO) :STB1, STB2

(PORTI/O) :TRGA1, TRGA2, TRGB1, TRGB2

3. Description of functions

Selection of functions

When the reset signal is input, the levels applied to the keyboard return input pins are latched by the internal reset signals to select the default functions.

Table of initial levels and functions

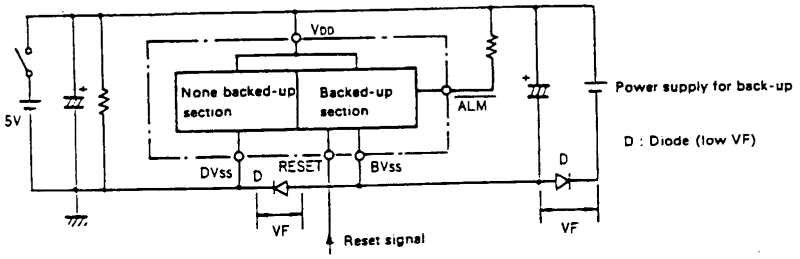
Pin name	Level	Function
$\overline{X2}$	0	RAS only refresh mode selected
	1	Hidden refresh mode selected
$\overline{X5}$	0	Mapper address output to MA18/KBDIR pin
	1	Keyboard bus direction output to MA18/KBDIR pin
$\overline{X6}$	0	Kana JIS layout
	1	Kana syllabary layout
$\overline{X7}$	0	Single wait requested for VDP read or write
	1	Single wait not requested for VDP read or write
$\overline{X3}$	0	$\overline{SLT03}/\overline{CS01}$ and $\overline{SLT02}/\overline{CS0}$ pins output slot select signals
	1	$\overline{SLT03}/\overline{CS01}$ and $\overline{SLT02}/\overline{CS0}$ pins output ROM select signals
$\overline{X1}$	0	Expansion to slot 0
	1	No expansion to slot 0 when $\overline{X3}$ = 1

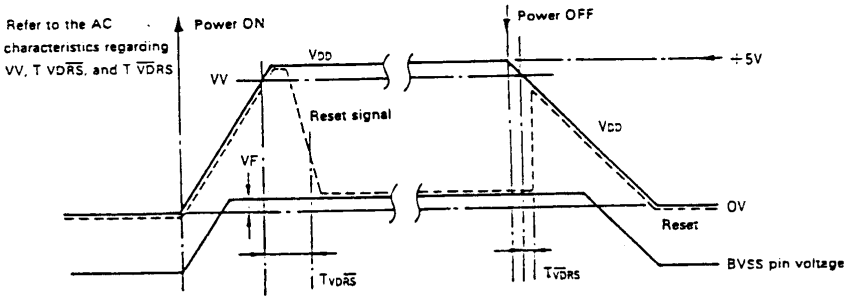
Back-up and reset

This devices uses the BVSS pin of the negative potential side to allow for back-up of the RAM data (4 bit x 26 and 8 bit x16).
Although a reset occurs when voltage of level "1" is applied to the RESET pin, the following precautions must be heeded to prevent loss of data and improper clock operation during switching between the back-up power supply and 5V power supply, and vice versa.

- When turning on the power supply with the device in the backed- up state, release the reset signal only after the level of the 5V power supply fully approaches 5V and all input levels to the device have stabilized.
- When switching off the power supply and shifting to the backed- up state, apply the reset signal and shift to back-up when the level of the 5V power supply starts to drop but is still close to 5V, and all input signals to the device are still stable.

There are various methods available for switching between the 5V power supply and back-up power supply. An example of a possible circuit and its operation are shown below.



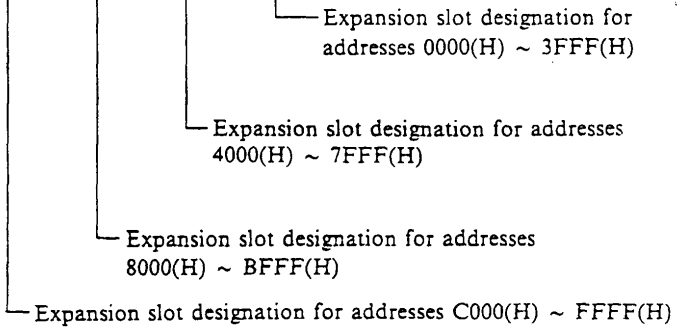


As shown in this diagram, there are no problems as the forward direction electrical potential (VF) for the diodes is merely shifted so that voltage to the BVSS pin of the backed-up section is supplied from the 5V power supply when it is operating, or the back-up battery when it is not. However, when the alarm function is activated and output is fetched from the $\overline{\text{ALM}}$ pin, this current will alter the VF value. This will cause the power supply voltage for the backed-up section to fluctuate according to the output from the $\overline{\text{ALM}}$ pin. This problem can be solved by having the resistance of the load connected to the $\overline{\text{ALM}}$ pin as high as possible, by using a circuit which limits fluctuations in the electrical potential corresponding to VF in relation to the current from the $\overline{\text{ALM}}$ pin, or by not connecting load resistance to the $\overline{\text{ALM}}$ pin when the alarm function is not used.

Expansion slot register

There are two registers for designation of the expansion slot: one for slot 0 and the other for slot 3. Expansion to both of the slots at the same time is possible. The inverse value of the contents is output when the registers are read. The address of the registers is FFFF(H) allowing slot expansion by input of the symbol obtained from NAND logic addresses AB8 ~ AB13 to the $\overline{\text{RSEL}}$ pin.

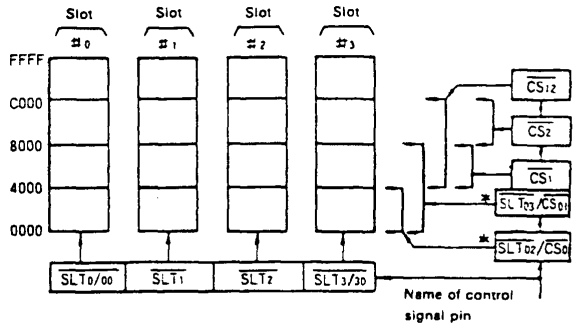
Expansion slot	Address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
Slot 0	FFFF(8H)	R/W								
Slot 3	FFFF(8H)	R/W								



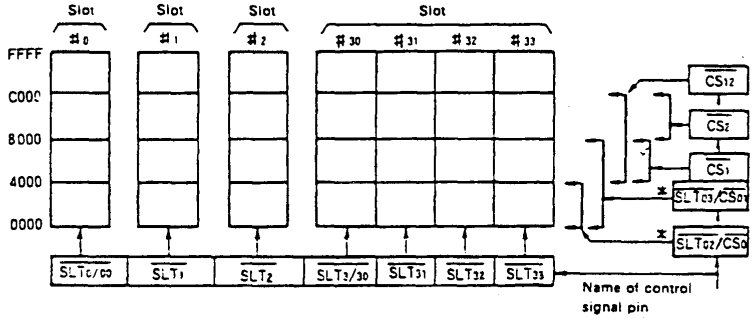
The slot expansion function is controlled by the level of the $\overline{\text{X1}}$ and $\overline{\text{X3}}$ pins when the device is reset. Refer to section on selection of this function.

Address map and slot expansion

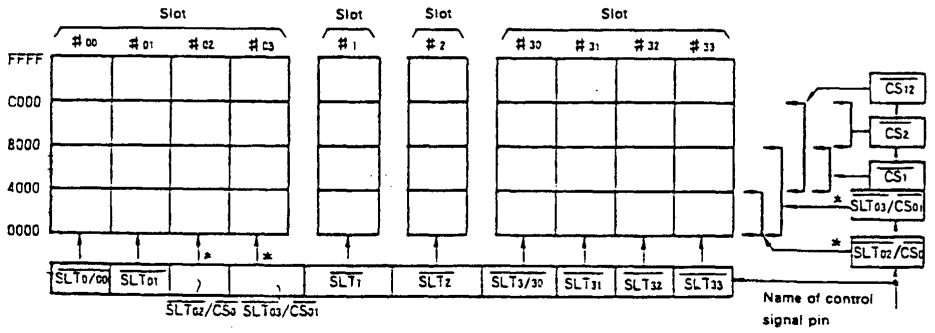
No expansion



Expansion to slot 3



Expansion to slots 0 and 3



Note: The prescribed input is made to the $\overline{\text{RSEL}}$ pin for slot expansion.
The function of the signals marked with asterisks is selected when the device is reset. They cannot be used at the same time when expansion is to slot 0.

I/O addresses and functions

Function	I/O address	W/R	Description
Back-up RAM	40(H)	W/R	Manufacturer ID number register
	41	W	Back-up RAM address latch
	42	W/R	Back-up RAM write/read
Bit map	46	W	Foreground/background color write
	47	W/R	Pattern and foreground/background color read
Printer	90	W/R	Printer strobe write, printer status read
	91	W/R	Printer data write/read
	93	W	Printer bus direction
VDP	98～9F	W	VDP write
	98～9F	R	VDP read
SSG	AB0	W	SSG address latch
	AB1	W	SSG data write
	AB2	R	SSG data read
Keyboard and Slot designation register	A8	W/R	slot designation
	A9	R	Keyboard return signal read
	AA	W/R	Keyboard drive, cassette and PPI sound write/read
	AB	W	Mode designation
Clock and slot designation	B4	W	Clock and back-up RAM address latch
	B5	W/R	Clock and back-up RAM write/read
Kanji	D8, D9	W/R	Kanji write/read
System control	F5	W	System control
Mapper	FC	W/R	Mapper register page 0
	FD	W/R	Mapper register page 1
	FE	W/R	Mapper register page 2
	FF	W/R	Mapper register page 3

Bit allocations of keyboard and slot designation registers

Function	Bit	W/R	Description
Slot designation register	0 1	W/R	Slot designation signal for addresses 0000(H)～3FFF(H)
	2 3		Slot designation signal for addresses 4000(H)～7FFF(H)
	4 5		Slot designation signal for addresses 8000(H)～BFFF(H)
	6 7		Slot designation signal for addresses C000(H)～FFFF(H)
Keyboard return	0 1 2 3 4 5 6 7	R	$\overline{X_0}$ $\overline{X_1}$ $\overline{X_2}$ $\overline{X_3}$ $\overline{X_4}$ $\overline{X_5}$ $\overline{X_6}$ X_7 } Keyboard return signal
Registers for keyboard drive, etc.	0 1 2 3	W/R	YA YB YC YD } YA～YD signals for keyboard drive
	4		REM signal for cassette control
	5		CMO signal for cassette write
	6		$\overline{\text{CAPS}}$ signal for CAPS lamp (LED)
	7		PPISND signal for sound
Mode setting	0 1 2 3 4 5 6 7	W	0 1 0 0 0 0 0 1 — The slot designation register and register for keyboard drive and other functions are cleared when the level shown on the left is given. This is the equivalent function to setting the PA and PC ports to output and PB port to input for MODE 0 of the 8255A.
	0 1 2 3 4 5 6 7	W	B_0 B_1 B_2 B_3 0 0 0 0 — Bits of the register for keyboard drive, etc., can be set and reset when the level shown on the left is given. B_1～B_3 express the bit numbers and the bits are set when B_0 is "1", and reset when "0".

Back-up RAM (8 bit X 16)

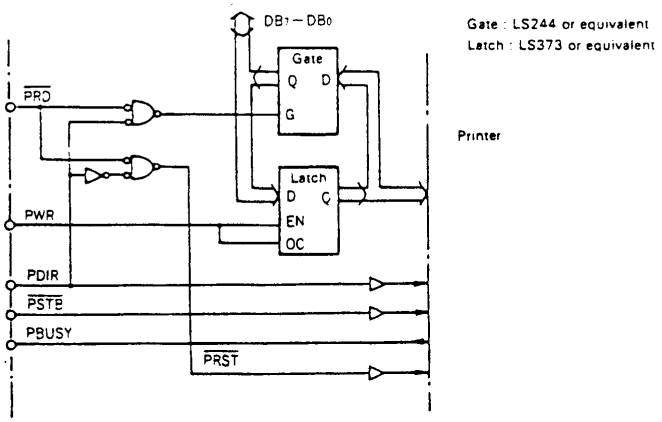
After the ASCII ID number FE (H) is written to the I/O address 40 (H), the inverted value of 01 (H) can be obtained when I/O address 40 (H) is read, indicating that the back-up RAM (8 bit X 16) and bit map function can be used. If the RAM address (X0 (H) - XF (H)) is then set by the lower four bits of the address data of I/O address 40 (H), data can be written or read at I/O address 42 (H).

Bit map function

As was indicated in the above section on the back-up RAM (8 bit X 16), writing data two or more times in succession to I/O address 46 (H) after access of I/O address 40 (H), also writes data to I/O address 46 (H). When I/O address 47 (H) is then read, the last data written to I/O address 46 (H) is obtained when bit 7 of the data written to I/O address 47 (H) is "0". The data which was written second to last is obtained when bit 7 is "0". Then, the data written to I/O address 47 (H) is shifted up one bit so that data of bit 7 becomes bit 0. This allows for data to be obtained according to the level of bit 7 each time I/O address 47 (H) is read.

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The following external circuit is necessary for bi-directional operation.



PBUSY: If a signal is input to the PBUSY pin and read, the same level as input to B1 is output.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
90 (H)	R								

$\overline{\text{PSTB}}$: When B0 is set to "0" are written to, the level at the $\overline{\text{PSTB}}$ pin goes to "0" at the point when the WR sihnal returns "1".

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
90 (H)	W								

PWR: If data is written when PDIR is "1" in the output state, a PWR signal having positive polarity according to the pulse width of the $\overline{\text{WR}}$ signal is output to the PWR pin. The data is latched and output to the external circuit when this signal returns to "0".
The level at the PWR pin is held at "1" if the input state is selected while PDIR is "0". When the output state is returned to again, the PWR pin remains at this level. The level goes to "0" when access of 91 (H) is completed.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
91 (H)	W	Data							

$\overline{PRD}$: If data is written when PDIR is "0" in the input state, a $\overline{PRD}$ signal having negative polarity according to the pulse width of the $\overline{RD}$ signal is output to the $\overline{PRD}$pin. This signal opens the gate of the external circuit allowing for data to be read.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
91 (R)	W	Data							

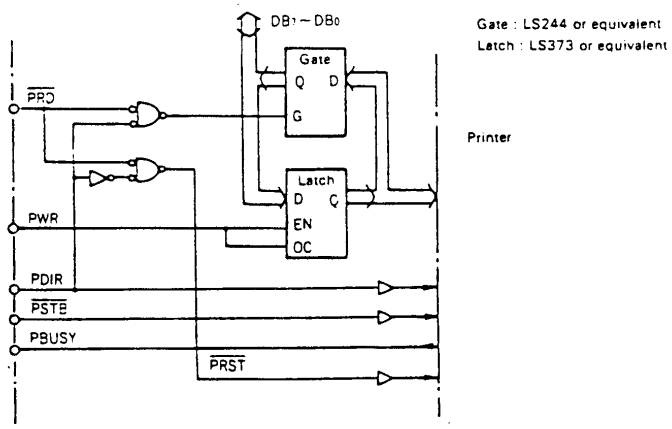
PDIR: If data is written with B1 = "1" and B0 = "1", a level of "1" is output continuously from the PDIR pin, and the MSX device is set to the output state. If data is written with B1 = "1" and B0 = "0" a level of "0" is output continuously from the PDIR pin, and the MSX device is set to the input state.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0	
93 (H)	W							1	1	→ Output state or $\overline{PRST}$ release
								1	0	→ Input state or $\overline{PRST}$ release
								0	1	→ $\overline{PRST}$ output
								0	0	→ $\overline{PRST}$ release

The $\overline{PRST}$ signal can be generated by the external circuit.
When the device is reset, and data is written with B1 = "0" and B0 = "1", the $\overline{PRD}$ pin outputs "0" continuously and the PDIR pin outputs "1". The $\overline{PRST}$ signal is created from these two signals.
The $\overline{PRST}$ signal is released by writing data with the levels of the two bits set to another combination than B1 = "0" and B0 = "1".

Printer

The following external circuit is necessary for bi-directional operation.



PBUSY: If a signal is input to the PBUSY pin and read, the same level as input to B1 is output.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
90 (H)	R								

$\overline{\text{PSTB}}$: When B0 is set to "0" are written to, the level at the $\overline{\text{PSTB}}$ pin goes to "0" at the point when the WR sihnal returns "1".

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
90 (H)	W								

PWR: If data is written when PDIR is "1" in the output state, a PWR signal having positive polarity according to the pulse width of the $\overline{\text{WR}}$ signal is output to the PWR pin. The data is latched and output to the external circuit when this signal returns to "0".
The level at the PWR pin is held at "1" if the input state is selected while PDIR is "0". When the output state is returned to again, the PWR pin remains at this level. The level goes to "0" when access of 91 (H) is completed.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
91 (H)	W	Data							

$\overline{PRD}$: If data is written when PDIR is "0" in the input state, a $\overline{PRD}$ signal having negative polarity according to the pulse width of the $\overline{RD}$ signal is output to the $\overline{PRD}$pin. This signal opens the gate of the external circuit allowing for data to be read.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
91 (R)	W	Data							

PDIR: If data is written with B1 = "1" and B0 = "1", a level of "1" is output continuously from the PDIR pin, and the MSX device is set to the output state. If data is written with B1 = "1" and B0 = "0" a level of "0" is output continuously from the PDIR pin, and the MSX device is set to the input state.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0	
93 (H)	W							1	1	→ Output state or $\overline{PRST}$ release
								1	0	→ Input state or $\overline{PRST}$ release
								0	1	→ $\overline{PRST}$ output
								0	0	→ $\overline{PRST}$ release

The $\overline{PRST}$ signal can be generated by the external circuit.
When the device is reset, and data is written with B1 = "0" and B0 = "1", the $\overline{PRD}$ pin outputs "0" continuously and the PDIR pin outputs "1". The $\overline{PRST}$ signal is created from these two signals.
The $\overline{PRST}$ signal is released by writing data with the levels of the two bits set to another combination than B1 = "0" and B0 = "1".

Kanji ROM select signal and system control

I/O addresses D8 and D9 (H) are kanji ROM selection signal outputs. The level of these outputs is controlled by the system control indicated below.
Output to the $\overline{\text{KANJI}}$ pin is enabled when data is written when B0 of the system control data is "1".

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0
F5 (H)	W								

Mapper

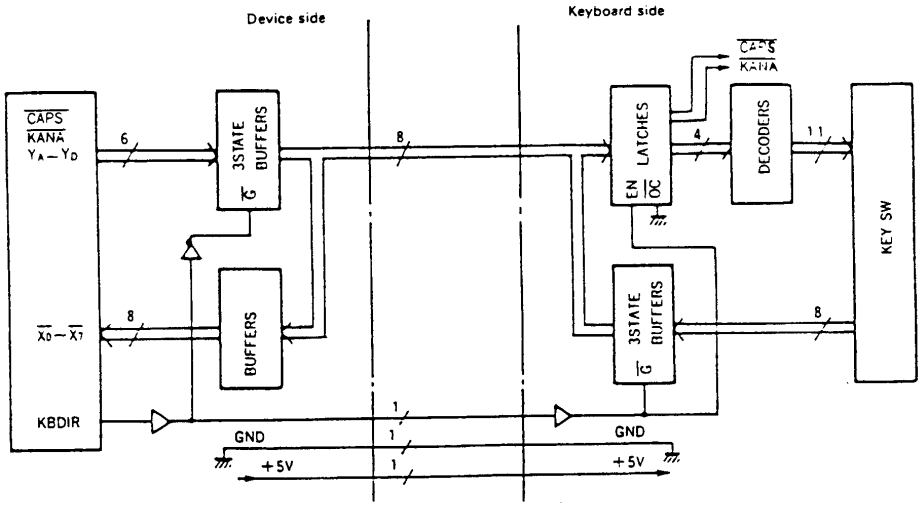
There are four mapper registers (0~3) located at I/O addresses FC (H) through FF (H). The effective bits is five for each, B4~B0, and these correspond to mapper addresses MA18~14. Mapper register pages 0~3 are selected according to addresses AB15 and AB14, and the contents are output as an address.
Thus, for example, if mapper addresses MA18~14 are used for 512K byte of RAM, the 512K byte indicated by the mapper register is divided into 32 sections. Each of these 16K byte areas can be selectively accessed by AB15 and AB14, making the addresses seem to increase.

I/O address	R/W	B7	B6	B5	B4	B3	B2	B1	B0	Register	AB15	AB14
FC (H)	R/W									Mapper register page 0	0	0
FD	R/W									Mapper register page 1	0	1
FE	R/W									Mapper register page 2	1	0
FF	R/W									Mapper register page 3	1	1

Mapper address					MA18	MA17	MA16	MA15	MA14	

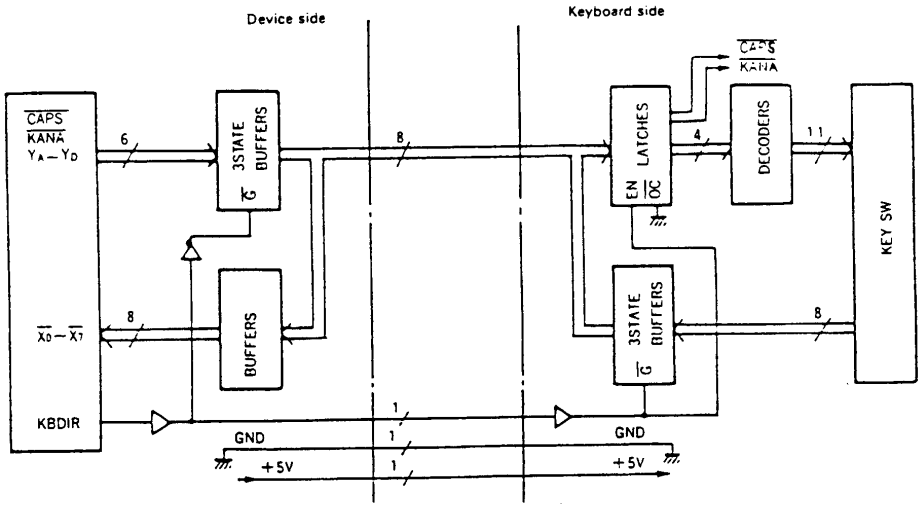
Keyboard bus direction

This signal outputs 1 1/2 bits at the end of the I/O cycle when data is written to I/O address AA (H) or AB (H). Use of a circuit similar to that shown below allows for the number of signal lines between the keyboard and main system to be reduced.



Keyboard bus direction

This signal outputs 1 1/2 bits at the end of the I/O cycle when data is written to I/O address AA (H) or AB (H). Use of a circuit similar to that shown below allows for the number of signal lines between the keyboard and main system to be reduced.



4. SSG and general purpose ports

The SSG (Software-controlled Sound Generator) is controlled by 14 registers (these registers can be read with no effect on sound).
Sound generation uses three square wave generator capable of voicing over 8 octaves, a pseudo-random noise generator, 5 bit envelope generator for single shot and repetitious attenuation , volume controller, mixer for combining music (tones) and noise, and a 5 bit D-A convertor. The general purpose port section consists of an input and output port which can be accessed through R/W registers.

Register array

When the upper bits, DB7~DB0, of the 8 bit address data is 0(H), the lower four bits, DB3~DB0, select the 15 registers. Address data which is fetched is held until the next address is fetched, and is not affected by read or write operations.
The contents of the register array is shown below.

Register array

Register	Address (H)	Function / Bit	B7	B6	B5	B4	B3	B2	B1	B0
R0	00	Frequency of channel A	8 bit fine tone adjustment							
R1	01						4 bit rough tone adjustment			
R2	02	Frequency of channel B	8 bit fine tone adjustment							
R3	03						4 bit rough tone adjustment			
R4	04	Frequency of channel C	8 bit fine tone adjustment							
R5	05						4 bit rough tone adjustment			
R6	06	Frequency of noise					5 bit noise frequency			
R7	07	General purpose port and mixer settings	Port *		Noise			Tone		
			"1"	"0"	C	B	A	C	B	A
R8	08	Level of channel A				M	L3	L2	L1	L0
R9	09	Level of channel B				M	L3	L2	L1	L0
RA	0A	Level of channel C				M	L3	L2	L1	L0
RB	0B	Frequency of envelope	8 bit fine adjustment							
RC	0C		8 bit rough adjustment							
RD	0D	Shape of envelope					CONT	ATT	ALT	HOLD
	0E	Data of general purpose input port	Refer to general purpose port bit allocation table							
RF	0F	Data of general purpose output port								

* Make sure that the section of R7 for ports is at the indicated levels.

General purpose ports

The input port is at address 0E (H) and the output port at address 0F (H). These ports are controlled by the register for output port data hold register RF. The general purpose port bit allocation table on the right shows the relationship between each of the bits, and the input/output pins.

General purpose port bit allocation table

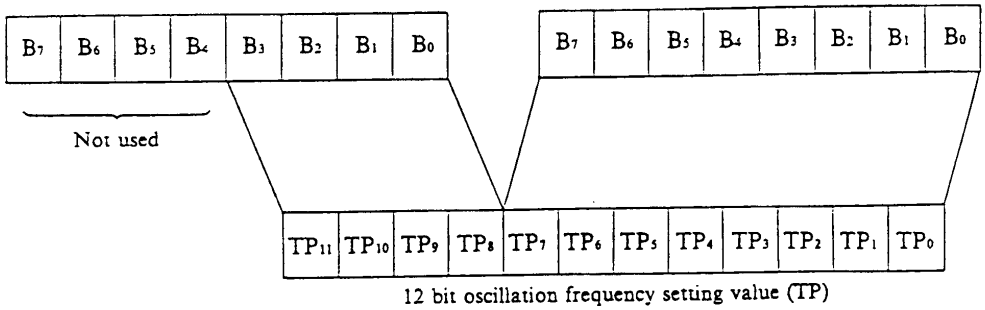
Port	Bit	Input	Names of connected pins
Input	B_0	i	FW1 or FW2 — FWD1 or FWD2 is selected by B6 of the output port. Input is from the FWD2 side when B6 = "1".
	B_1		BACK1 or BACK2
	B_2		LAFT1 or LAFT2
	B_3		RIGHT or RIGHT2
	B_4		TRGA1 or TRGA2
	B_5		TRGB1 or TRGB2
	B_6		JIS/50
	B_7		CM1
Output	B_0	o	TRGA1
	B_1		TRGB1
	B_2		TRGA2
	B_3		TRGB2
	B_4		STB1
	B_5		STB2
	B_6		Input selection for input port B0 ~ B5 (not externally output)
	B_7		$\overline{\text{KANA}}$

Setting of music frequencies (controlled by registers $R_0 \sim R_5$)

The frequencies of the square wave generated by the music generators for the three channels (A, B, and C) are set by registers R_0 through R_5 R_0 and R_1 control channel A, R_2 and R_3 are used for channel B, and R_4 and R_5 control channel C. The oscillation frequency F_T is obtained in the following manner from value of the register TP (decimal). Fø is the clock frequency.

$$F_T = \frac{F\text{ø}}{32TP}$$

Rough tone adjustment register [R_1, R_3, R_5] Channel [A, B, C] Fine tone adjustment register [R_0, R_2, R_4]



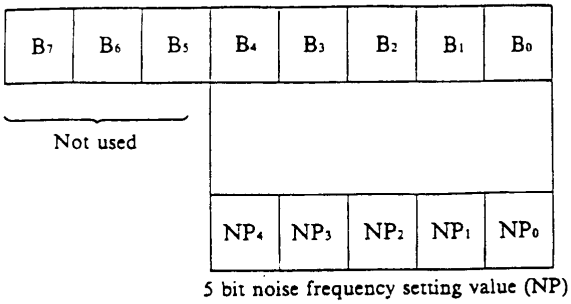
12 bit oscillation frequency setting value (TP)

Setting of noise generator (controlled by register R_6)

The noise frequency F_N is obtained from the register value NP (decimal) in the following manner. Fø is the clock frequency.

$$F_N = \frac{F\text{ø}}{32NP}$$

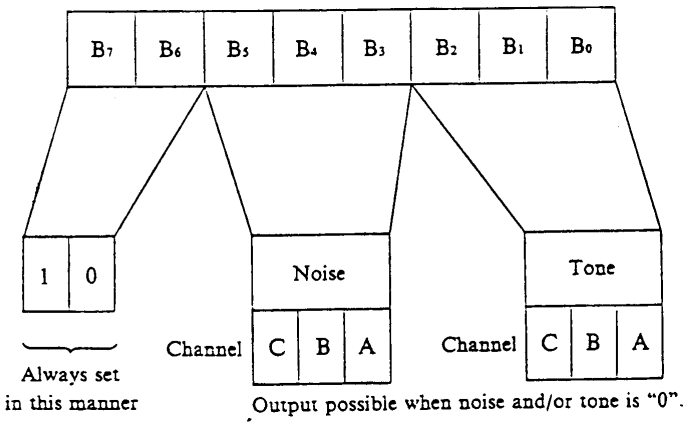
Noise frequency register R_6



Settings of mixer (controlled by register R_7)

The mixer is used to combine music and noise components. The combination is determined by bits $B_5 \sim B_0$ of register R_7 Sound is output when a "0" is written to the register. Thus, when both the noise and tone are "0", the output is combined by the mixer. Whichever is "0" is output, and nothing is output when both are "1".

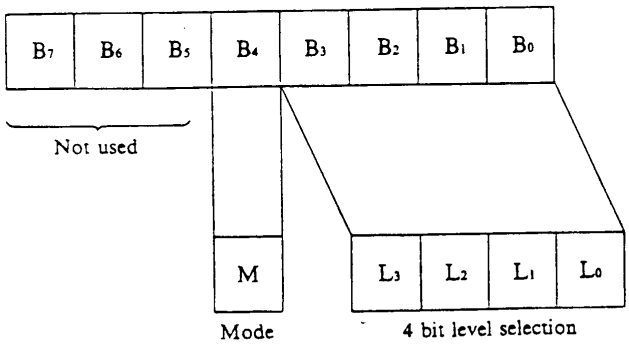
Mixer setting register R_7



Level control (controlled by registers R_8~R_A)

The audio level output from the D/A convertors for the three channels (A. B, and C) is adjusted by registers R_8, R_9, and R_A). Mode M selects whether the level is fixed (when M = 0) or variable (M = 1). When M = 0, the level is determined from one of 16 by level selection signals L_3, L_2, L_1, and L_0 which compromise the lower four bits. When M = 1, the level is determined by the 5 bit output of E_4, E_3, E_2, E_1, and E_0 of the built-in envelope generator. This level is variable as E_4~E_0 change over time.

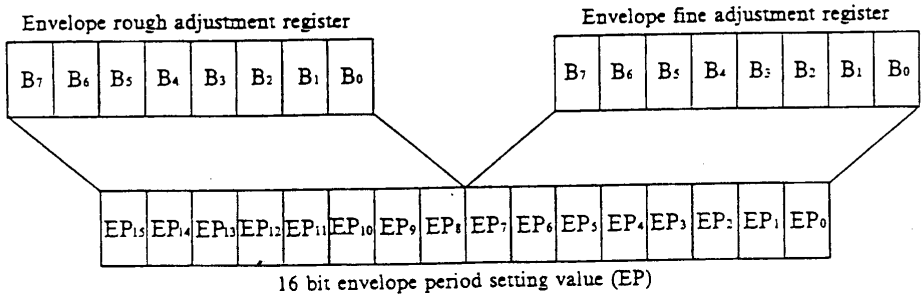
Level setting registers
- R_8 : Channel A
- R_9 : Channel B
- R_A : Channel C



Setting of envelope frequency (controlled by registers R_B and R_C)

The envelope repetition frequency F_E is obtained as follows from the envelope frequency setting value E_P (decimal). Fø is the clock frequency.

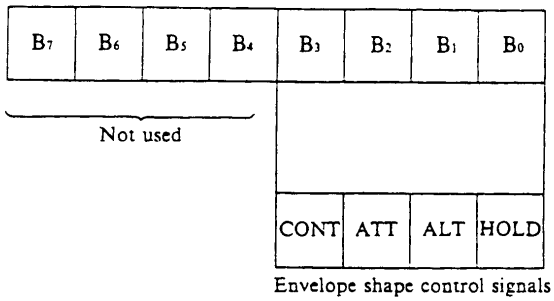
$$F_E = \frac{F\text{ø}}{512\ EP}$$



Envelope shape control (controlled by register R_D)

The envelope level is determined by the envelope generator using the 5 bits $L_4 \sim L_0$. The shape of this envelope is created by increasing, decreasing, stopping, or repeating the counter for the envelope generator. The shape is controlled by bits $B_3 \sim B_0$ of the register R_D.

Envelope shape control register R_D



The envelope can take the shapes shown in the table below according to combinations of the CONT, ATT, ALT, and HOLD signals.

Table of envelope shapes

B_3	B_2	B_1	B_0	Envelope shape
CONT	ATT	ALT	HOLD	
0	0	x	x	
0	1	x	x	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

→ | $1/f_E$ | ← Repetition period of envelope

D-A Convertor

When the D-A convertor normalizes the maximum amplitude to 1V, the output changes as shown in the diagrams below. This conversion from linear input to logarithmic output provides a wide dynamic range and a natural feeling of attenuation.

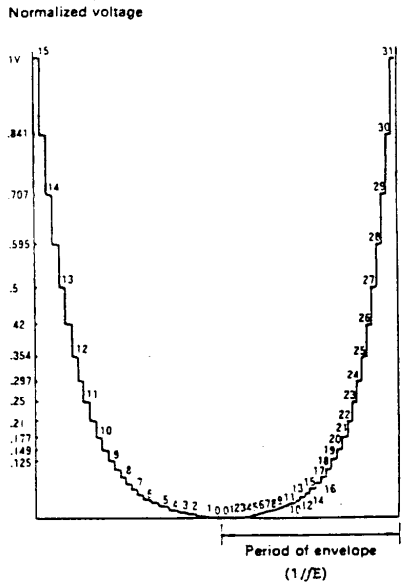


Fig. 1 Output level of DA convertor
The subscripts on the left half of the diagram are the fixed levels of the selection signals L_3, L_2, L_1, and L_0 converted into decimal values. The subscripts on the right side are decimal expressions of the envelope counter output signals E_4, E_3, E_2, E_1, and E_0.

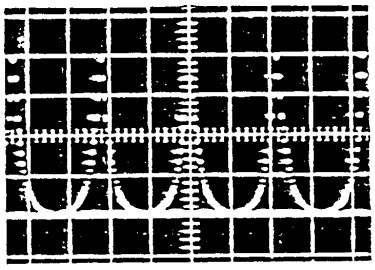


Fig. 2 Output waveform of single tone with envelope (R_D = XXXX1110)

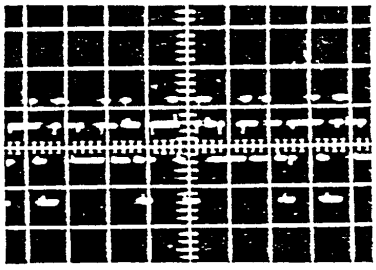
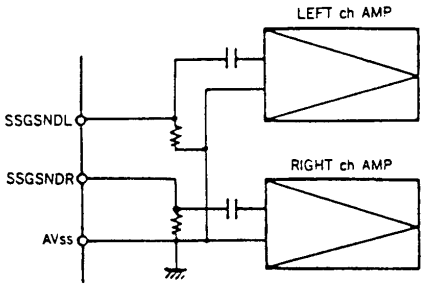


Fig. 3 Output waveform from mixing of three sounds with fixed level ($R_D \sim R_A$ = XXXX1100)

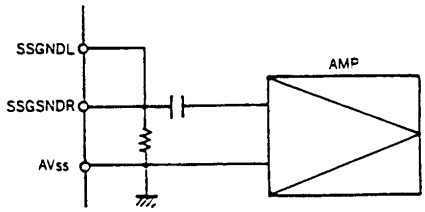
Sound output SSGSNDL and SSGSNDR

Of the music signals generated on channels A, B, and C by the data set in the registers, channel B is output from the SSGSNDL pin and channel C is output from the SSGSNDR pin. Channel A is the mixed signal from the SSGSNDL and SSGSNDR pins. Output is thus stereo output having left and right output signals. Monaural output is also possible by shorting the the SSGSNDL and SSGSNDR pins when not in use.

Possible configuration for stereo output



Possible configuration for monaural output



5. Clock and RAM (4 bit x 26)

The clock section is connected to the crystal oscillation circuit and provides second, minute, hour, day of the week, day, month, and year clock counter functions, and minute, hour, day of the week, and day alarm registers. Control such as setting and reading the clock data for time and calender and alarm data is carried out in this section. All of this data can be backed up.

Address allocations and initial state of counters and registers

Regardless of the value of the upper four bits of the 8 bit address data, the mode is selected from the low four bits $DB_3 \sim DB_0$ and the four modes indicated by the address X D (H) modes registers M1 and M0. Addresses X 0 (H) ~ X C (H) can be are both writable and readable. Address X D (H) ~ X F (H) is write only, and has no effect on the mode.
The state of the counters and registers is indeterminate when the power is turned on. They must be set by writing the prescribed values.

Allocation of addresses and functions

Mode	0					1					2	3
Adress (H)	Function / Bit	B_3	B_2	B_1	B_0	Function / Bit	B_3	B_2	B_1	B_0	Function	Function
x 0	1 second counter											
x 1	10 second counter											
x 2	1 minute counter					1 minute alarm register					RAM	RAM
x 3	10 minute counter					10 minute alarm register					4 Bit	4 Bit
x 4	1 hour counter					1 hour alarm register					x	x
x 5	10 hour counter					10 hour alarm register					13	13
x 6	Day of the week counter					Day of the week alarm register						
x 7	1 day counter					1 day alarm register						
x 8	10 day counter					10 day alarm register						
x 9	1 month counter											
x A	10 month counter					12/24 hour selector						
x B	1 year counter					Leap year calender						
x C	10 year counter											

Address (H)	Function / Bit	B_3	B_2	B_1	B_0
x D	Mode register	Timer EN	Alarm EN	Mode M_1	Mode M_0
x E	Test register	Test T_3	Test T_2	Test T_1	Test T_0
x F	Reset controller 16/1Hz register	1HZ ON	16HZ ON		Alarm

Note: The day of the week counter counts between 0 and 7. The relationship between actual day of the week and counter value can be determined as desired.

Mode setting and alarm/timer EN function (address x D (H))

The 4 bit mode register consists of M_1 and M_0 for switching the mode functions and two bits for the timer EN and alarm EN.

Mode	M_1	M_0	Description
0	0	0	Time and calender can be set and read
1	0	1	Alarm, 12/24 selection, and leap year can be set and read
2	1	0	RAM (4 bit x13) is both readable and writable
3	1	1	RAM (4 bit x 13) is both readable and writable

Function	Level	Description
Alarm EN	0	Alarm signal not output to $\overline{AML}$ pin
	1	Alarm signal output to $\overline{AML}$ pin
Timer EN	0	Counter stopped for other than seconds
	1	Clock started

Reset control function and 16Hz/1Hz register setting (address x F (H))

Alarm reset and timer reset function during the data write, and not have registers. There are registers for 16Hz ON and 1Hz ON. These function in the following manner.

Function	Level	Description
Alarm RESET	1	All alarm registers reset upon write.
Timer RESET	1	Counter is reset from seconds upon write.
16Hz ON	0	16Hz signal output to $\overline{ALM}$ pin.
1Hz ON	0	1Hz signal output to $\overline{ALM}$ pin.

Test registers (addresses x E (H))

T_3~T_0 are registers for test purposes. Tests are performed for all except test 0 (operation as clock). When using the clock for the first time, set all bits to level "0" in order to perform test 0 (clock).

Test	T_3	T_2	T_1	T_0	Description
0	0	0	0	0	Operation as clock.
1	0	0	0	1	Test 1 selected.
2	0	0	1	0	Test 2 selected.
3	0	0	1	1	Test 3 selected. Output to $\overline{ALM}$ pin.
4	0	1	0	0	Test 4 selected.
8	1	0	0	0	Test 8 selected.

Setting of 12/24 selector (mode 1, address x A (H))

Selection of operation as a 12 hour clock or 24 hour clock is possible by writing the level shown in the table below. Set the time after making this setting.

Function	Level	Description
12/24 hour selector	0	Operation as 12 hour clock. When this mode is selected, the 10 hour counter and B1 of the alarm register indicated AM or PM. AM is selected when B1 is "0", and PM when "1".
	1	Operation as 24 hour clock.

Setting of leap year (mode 1, address x B (H))

The leap year setting can be made by setting the levels shown in the table below. The time and calender settings are made after this setting is made. This calender is incremented together with the year calender.

Function	B_1	B_0	Description
Leap year counter	0	0	Operation with this year as leap calender year
	0	1	Three years from now
	1	0	Year after next as leap year
	1	1	Next year as leap year

Setting and reading the time and calender (mode 0, address x 0 (H)~ x C(H))

The addresses can be fixed by the functions indicated in the table for address allocations and functions. The clock counter can be set by writing effective values for time and calender clock data. Data is read in the same manner. The address is fixed and the bits are read to obtain the clock data. The level of bits which are not effective is always "0".

If the time of the second, minute, hour, day of the week, day or year counter (clock counter) advances while setting or reading the clock data, it is not possible to set or read the proper values for the clock data.

Thus when setting the clock data, generate a timer reset and set all necessary clock data during this second. An alternate procedure is to generate a clock EN to stop incremention of all counters except seconds, generate a timer reset, set all necessary clock data within one second, and then update the clock with the timer EN. When reading the clock data, read it twice and compare the results to determine usable data. Another approach is to set the clock timer to the operational state again with the timer EN and read the data. The change in the 1 second signal which occurs while the counter is stopped for all counting above one second, will be adjusted when clock is restarted. Approximately 100&mu.s are required for this correction. Be sure not read the time again during this period.

Alarm setting and reading (mode 1, address x 2 (H) ~ x 8 (H))

The alarm registers can be set by fixing the addresses by the functions indicated in the table for address allocations and functions, and then by writing valid values to the bits for time and calender alarms. The data in the alarm registers can be obtained in the same manner by fixing the addresses, and reading the bits.
When the contents of the minute, hour, day of the week, day and year alarm registers is the same as the contents of the clock calender (and alarm EN register is set to output state), a level "0" signal is output to the $\overline{\text{ALM}}$ pin.
The alarm register is reset by the alarm RESET bit. Then, the data written to the alarm register and clock counter are made the same. Regarding alarm registers which were not written to, output is to the $\overline{\text{ALM}}$ pin as the data of both were already the same.

$\overline{\text{ALM}}$ pin output (external load resistance is needed as open drain)

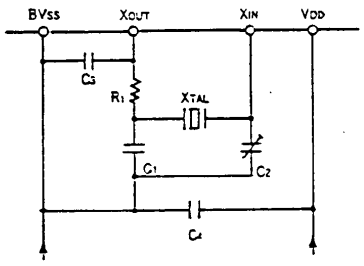
The signals controlled by the alarm En, 16HZON, 1HZON, and test registers can be output simultaneously from this pin. Set the level of the various registers so that only the required signals are output.

RAM (4 bit x 26) (mode 2 and 3, address x 0 (H) ~ x C (H))

This RAM area consists of a RAM area accessed at address X0 (H) ~ X C (H) in mode 2, and a RAM area accessed at address X 0 (H) ~ X C (H) in mode 3.

6. Oscillation circuit

A sample oscillation circuit is shown on the right.
Note that the accuracy of the clock will suffer if the oscillation circuit is effected by external noise.
The voltage characteristics and temperature characteristics of the clock oscillation circuit, back-up voltage and current characteristics and back-up current and C3 characteristics are shown below.
All parts other than the device itself are kept at room temperature during measurement of temperature characteristics.



X_{TAL} = 32.768KHz
C_1 = 68PF
C_2 = 60PF(MAX)
C_3 = 39PF
C_4 = 1 μF
R_1 = 120K Ω

9. Electrical characteristics

Absolute maximum ratings

Item	Rated value	Units
Power supply voltage (V_{DD})	−0.3 ~ 7.0	V
Input pin voltage	−0.3 ~ V_{DD} + 0.3	V
Operational surrounding temperature	0 ~ 70	°C

10. Recommended operating conditions

Item	Symbol	Minimum	Typical	Maximum	Units
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Data retention voltage	V_{DE}	2.0		5.25	V
Frequency for clock	F_X		32.768		KHz

11. DC characteristics

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
Low level input voltage 1	V_{IL1}	Other than ($\overline{X}_0$ ~ $\overline{X}_7$, XIN)	−0.3		0.8	V
High level input voltage 1	V_{IH1}	Other than ($\overline{X}_0$ ~ $\overline{X}_7$, XIN)	2.0		V_{DD}	V
Low level input voltage 2	V_{IL2}	($\overline{X}_0$ ~ $\overline{X}_7$, XIN)	−0.3		1.5	V
High level input voltage 2	V_{IH2}	($\overline{X}_0$ ~ $\overline{X}_7$, XIN)	3.5		V_{DD}	V
Low level output voltage 1	V_{OL}	I_{OL} = Note 0)	0		0.5	V
High level output voltage 1	V_{OH}	I_{OL} = Note 0)	4.0		V_{DD}	V
Input current	I_I	$V_{IN} = 0^V$	50		500	μA
Input leak current	I_{LI}	$V_{IN} = 0 \sim 5^V$			±10	μA
Output leak current	I_{LO}	$V_{IN} = 0 \sim 5^V$			±10	μA
Power supply voltage (hold)	I_{DB}	$V_{DB} = 2.0^V$			15	μA
Power supply voltage (operating)	I_{DD}	$V_{DB} = 5.25^V$			35	μA

Note 0) I_{OL} = 10mA : Applies to $\overline{WAIT}$, $\overline{CAPS}$, and $\overline{KANA}$ pins
I_{OL} = 2.4mA : Applies to output pins other than $\overline{WAIT}$, $\overline{CAPS}$, and $\overline{KANA}$
I_{OH} = 0.2mA : Applies to all output pins other than open drain.

12. AC characteristics Note 1)

Clock timing

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
Clock period	T_c			280		ns
Rise time of clock	$T_{\phi r}$				30	ns
Fall time of clock	$T_{\phi f}$				30	ns

Write timing

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
Assurred time prior to data $\overline{WR}$ off	T_{WRS}			300		ns
Hold time from data $\overline{WR}$ off	T_{WRH}			0		ns
Delay time from $\overline{WR}$ off of output data	T_{WRD}	Note 2) CL = 100PF			250	ns
Delay time from output data	T_{DD}	Note 3) CL = 100PF			250	ns

Read timing

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
Data delay time	$T_{\overline{RD}D}$				250	ns
Transition time to float state	T_{RDF}				100	ns
Assured time prior to input data $\overline{RD}$	$T_{\overline{RD}S}$	} Note 4)		0		ns
Hold time for input data $\overline{RD}$	T_{RDH}			0		ns

Note 1) The various timing characteristics assume that direct connection is made to the address bus, data bus, and control bus signals of the CPU.

Note 2) Applies to YA, YB, YC, YD, REM, CMO, $\overline{CAPS}$, and PPISND pins.

Note 3) Applies when TRGA1, TRGB1, STB1, STB2, TRGA2, TRGB2, $\overline{KANA}$, PDIR, PWR, and $\overline{PRD}$ pins are controlled by data bus.

Note 4) Applies to $\overline{X0}$, $\overline{X1}$, $\overline{X2}$, $\overline{X3}$, $\overline{X4}$, $\overline{X5}$, $\overline{X6}$, $\overline{X7}$, FWD1, BACK1, LEFT1, RIGHT1, TRGA1, TRGB1, FWD2, BACK2, LEFT2, RIGHT2, TRGA2, TRGB2, CMI, and PBUSY pins.

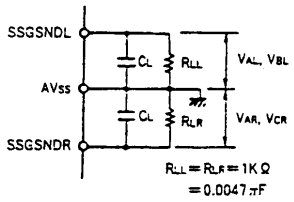
Reset timing

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
RESET ↑ $\overline{X_n}$ ↓ delay time	$T_{RS\overline{X}}$	$\overline{X_n}$ = ($\overline{X_1}$, $\overline{X_2}$, $\overline{X_3}$, $\overline{X_5}$ $\overline{X_6}$, $\overline{X_7}$)			150	ns
RESET ↓ $\overline{X_n}$ ↑ delay time	$T_{\overline{RS}X}$		50			ns
RESET ↑ RESET ↓ time	T_{RSW}		5.6			μs
V_{DD} (4.5) ↑ RESET ↓ delay time	$T_{VD\overline{RS}}$		5.6			μs
V_{DD} (4.5) ↓ RESET ↑ delay time	$T_{\overline{VD}RS}$				0	μs

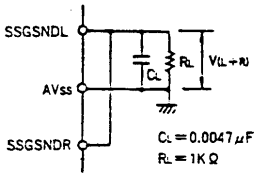
Analog output

Item	Symbol	Conditions	Minimum	Typical	Maximum	Units
Output voltage from channel A to SSGSNDL	V_{AL}	Note 7) and Note 9)	0.28	0.35	0.44	V_{pp}
Output voltage from channel A to SSGSNDR	V_{AR}		0.28	0.35	0.44	V_{pp}
Output voltage from channel B to SSGSNDL	V_{BL}		0.52	0.66	0.83	V_{pp}
Output voltage from channel C to SSGSNDR	V_{CR}		0.52	0.66	0.83	V_{pp}
Output voltage when SSGSNDR and SSGSNDL are connected	$V_{(L+R)}$	Note 8) and Note 9)	0.42	0.53	0.67	V_{pp}

Note 7) Circuit for separate output of L and R



Note 8) Circuit for combined output of L and R



Note 9) State of registers during SSGSNDL and SSGSNDR output voltage measurement

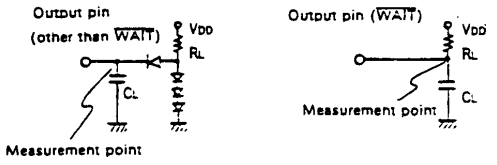
Music frequency setting register : 0FF (H) (≃440Hz)
Volume control register : 0F (H) (max. volume)
Mixer register : Separate output of A, B, and C channels

Timing of M1 cycle, Memory read/write cycle, and I/O cycle

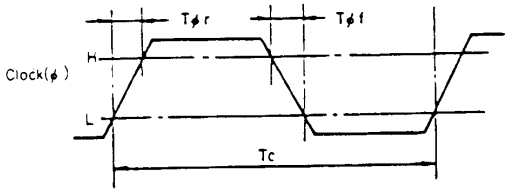
Item					Symbol	Conditions	Minimum	Maximum	Units
$\overline{MREQ}$	↓	$\overline{WAIT}$	↓	delay time	$T_{MRW\overline{A}}$	CL = 100PF R_L = 1 KΩ		150	ns
Clok	↓	$\overline{WAIT}$	↑	-	$T\overline{\emptyset}_{WA}$	-		150	ns
$\overline{MREQ}$	↓	$\overline{RAS}$	↓	-	$T_{MR\overline{RA}}$	CL = 100PF R_L = 3.9 KΩ		70	-
$\overline{MREQ}$	↑	$\overline{RAS}$	↑	-	T_{MRRA}	-		70	-
Clok	↑	$\overline{RAS}$	↓	-	$T\emptyset\overline{RA}$	-		70	-
Clok	↓	$\overline{RAS}$	↑	-	$T\overline{\emptyset}_{RA}$	-	90	180	-
Clok	↑	MPX	↑	-	$T\emptyset_{MX}$	-		70	-
$\overline{MREQ}$	↑	MPX	↓	-	$T_{MR\overline{MX}}$	-		70	-
$\overline{RAS}$	↓	MPX	↑	-	$T\overline{RA}_{MX}$	-	50		-
Clok	↓	$\overline{CAS}$	↓	-	$T\overline{\emptyset}\overline{CA}$	-		70	-
$\overline{MREQ}$	↑	$\overline{CAS}$	↑	-	T_{MRCA}	-		70	-
Clok	↓	$\overline{CAS}$	↑	-	$T\overline{\emptyset}_{CA}$	-		70	-
$\overline{RD}$	↓	$\overline{WE}$	↑	-	$T\emptyset_{WE}$	-		70	-
Clok	↓	$\overline{WE}$	↑	-	$T\overline{\emptyset}\overline{WE}$	-		70	-
$\overline{MREQ}$	↓	*$\overline{CSn}$	↓	-	$T_{MR\overline{CS}}$	-		70	-
$\overline{MREQ}$	↑	*$\overline{CSn}$	↑	-	T_{MRCS}	-		70	-
$\overline{MREQ}$	↓	*$\overline{SLTn}$	↓	-	$T_{MR\overline{SL}}$	-		70	-
$\overline{MREQ}$	↑	*$\overline{SLTn}$	↑	-	T_{MRSL}	-		70	-
$\overline{MREQ}$	↓	*$\overline{SLTnn}$	↓	-	$T_{MR\overline{ST}}$	-		70	-
$\overline{MREQ}$	↑	*$\overline{SLTnn}$	↑	-	T_{MRST}	-		70	-
ADR		*MAn		-	T_{DMA}	-		120	-
ADR(OFF)		*MAn(OFF)		-	T_{ADMA}	-		120	-
$\overline{RD}$	↓	$\overline{VDPCR}$	↓	-	$T_{R\overline{DVR}}$	-		70	-
$\overline{RD}$	↑	$\overline{VDPCR}$	↑	-	T_{RDVR}	-		70	-
Clok	↑	$\overline{VDPCW}$	↓	-	$T\emptyset_{\overline{VW}}$	-		70	-
$\overline{WR}$	↑	$\overline{VDPCW}$	↑	-	T_{WRVW}	-		40	-
$\overline{IORQ}$	↓	$\overline{KANJI}$	↓	-	$T_{IO\overline{KN}}$	-		70	-
$\overline{IORQ}$	↑	$\overline{KANJI}$	↑	-	T_{IOKN}	-		70	-
$\overline{RD}$	↓	$\overline{PRD}$	↓	-	$T_{R\overline{DPR}}$	-		150	-
$\overline{RD}$	↑	$\overline{PRD}$	↑	-	T_{RDPR}	-		150	-
$\overline{WR}$	↓	PWR	↑	-	$T_{W\overline{RPW}}$	-		150	-
$\overline{WR}$	↑	PWR	↓	-	$T_{WR\overline{PW}}$	-		150	-
Clok	↑	KBDIR	↑	-	$T\emptyset_{KD}$	-		150	-
Clok	↓	KBDIR	↓	-	$T\overline{\emptyset}_{\overline{KD}}$	-		150	-

Note 5: Refer to Note 10 for those marked with asterisks.

Note 6: The load circuit is shown on the right.

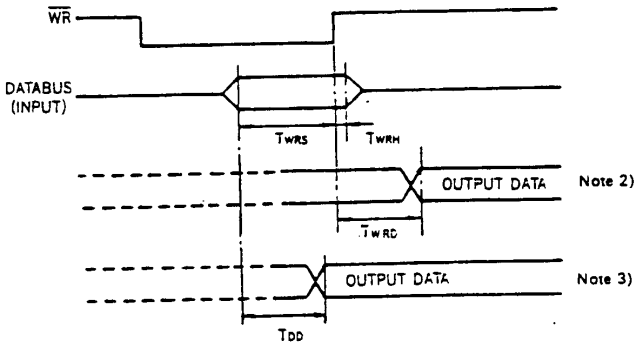


Clock timing

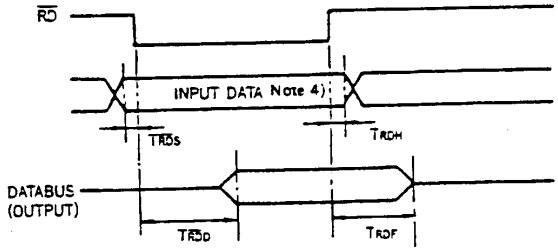


	"H"	"L"
CLOCK (ø)	$V_{DD}-0.6^{V}$	0.8^{V}
OUT PUT	2.0^{V}	0.8^{V}
IN PUT	2.0^{V}	0.8^{V}
FLOAT	Δ^{V}	$\pm 0.5^{V}$

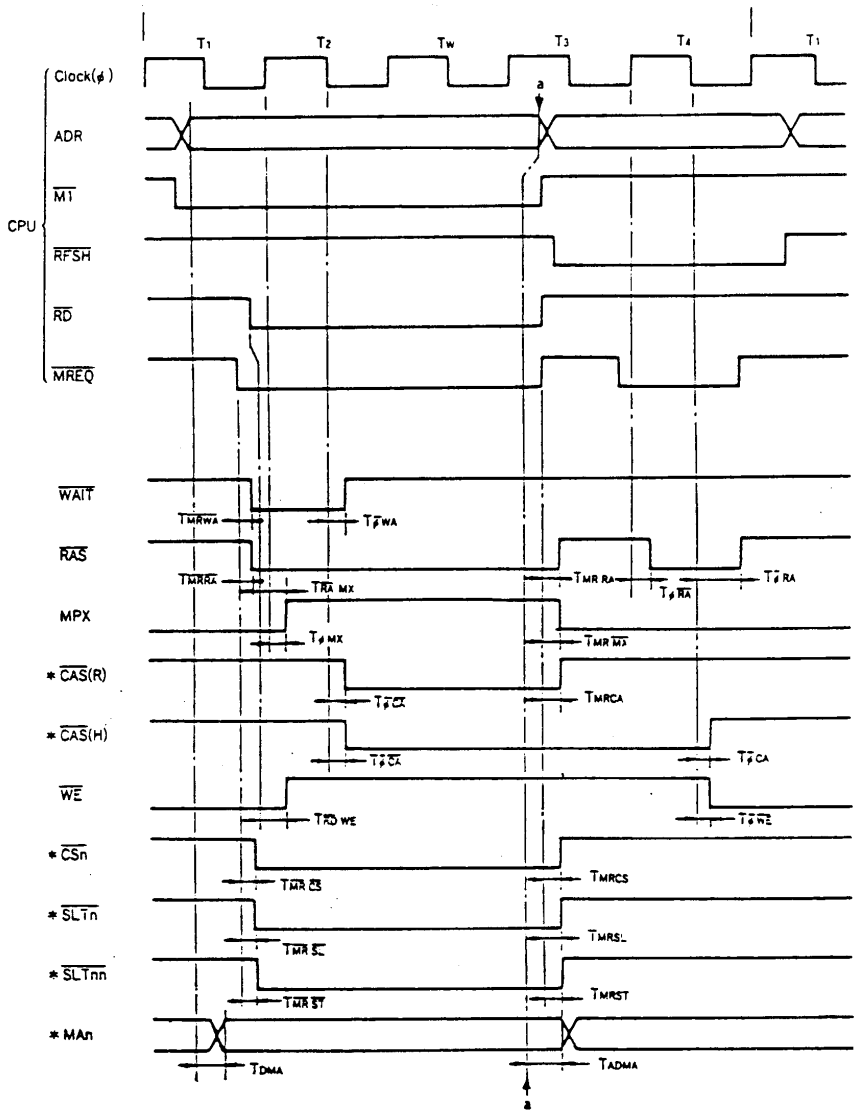
Write timing



Read timing



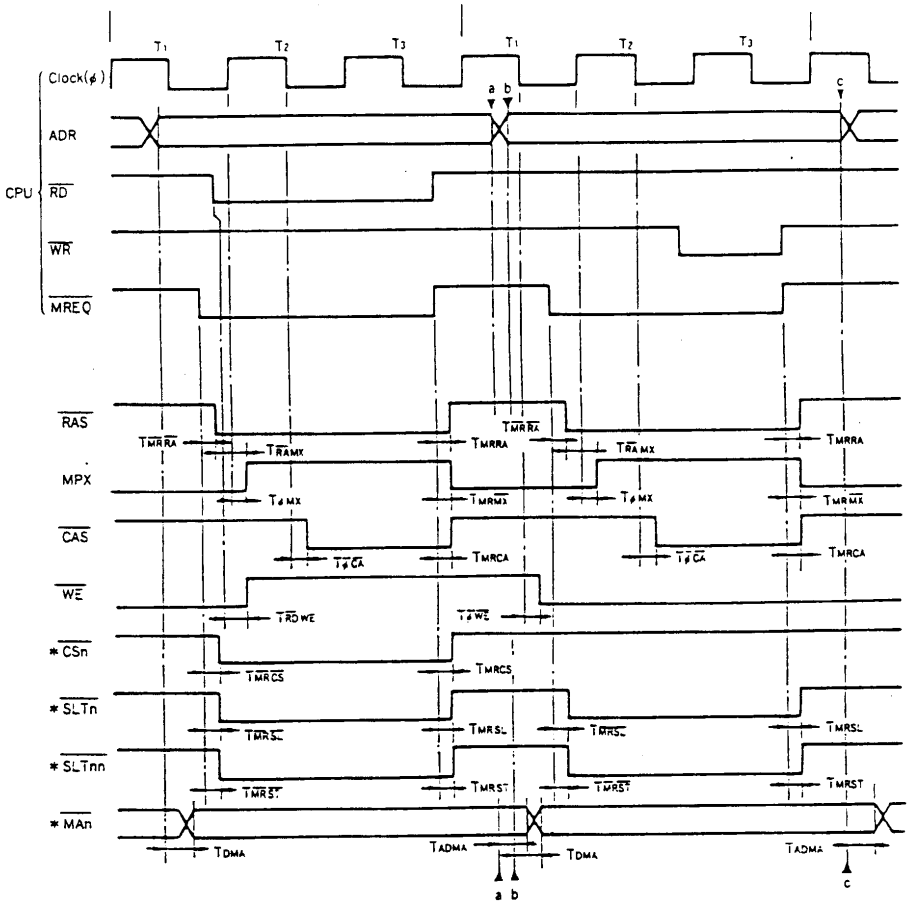
M1 cycle timing



Note 10: Refer to the following for signals marked with asterisks

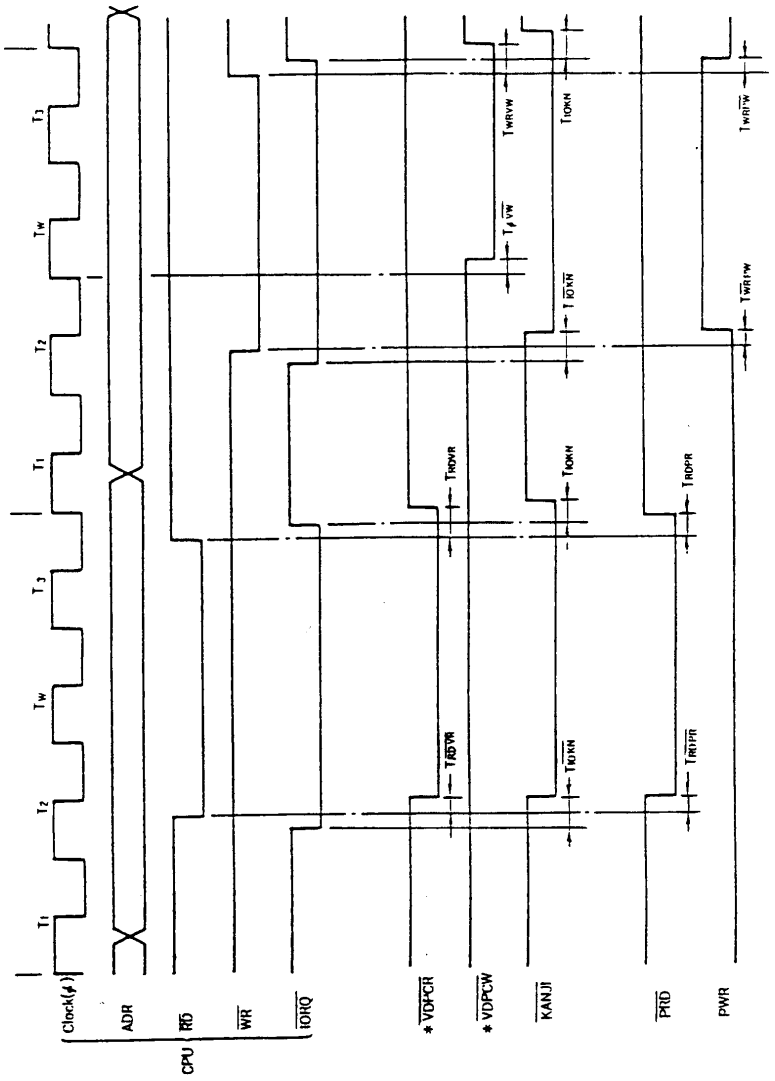
$\overline{\text{CAS}}$ (R) : $\overline{\text{CAS}}$ signal in RAS only refresh mode
$\overline{\text{CAS}}$ (H) : $\overline{\text{CAS}}$ signal in hidden refresh mode
$\overline{\text{CAn}}$: $\overline{\text{CS1}}$, $\overline{\text{CS2}}$, $\overline{\text{CS12}}$, and $\overline{\text{CS0}}$ and $\overline{\text{CS01}}$ of $\overline{\text{SLT02/CS0}}$ and ;us on$\overline{\text{SLT03/CS01}}$
$\overline{\text{SLTn}}$: $\overline{\text{SLT1}}$ and SLT2 output
$\overline{\text{SLTnn}}$: $\overline{\text{SLT3/30}}$, $\overline{\text{SLT31}}$, $\overline{\text{SLT32}}$, $\overline{\text{STL33}}$, $\overline{\text{SLT0/00}}$, $\overline{\text{SLT01}}$, $\overline{\text{SLT02/CS0}}$, $\overline{\text{SLT02 of SLT03/CS01}}$, and $\overline{\text{SLT03}}$ output
MAn : MA_{14}, MA_{15}, MA_{16}, MA_{17}, and MA_{18} output of MA_{18}/KBDIR

Memory read/write cycle timing



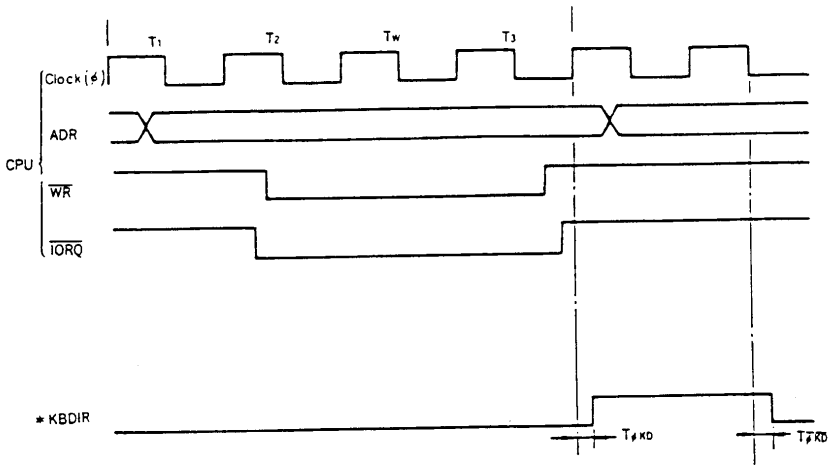
Note 11: Refer to Note 10 for signals marked with asterisk

I/O cycle timing (1)



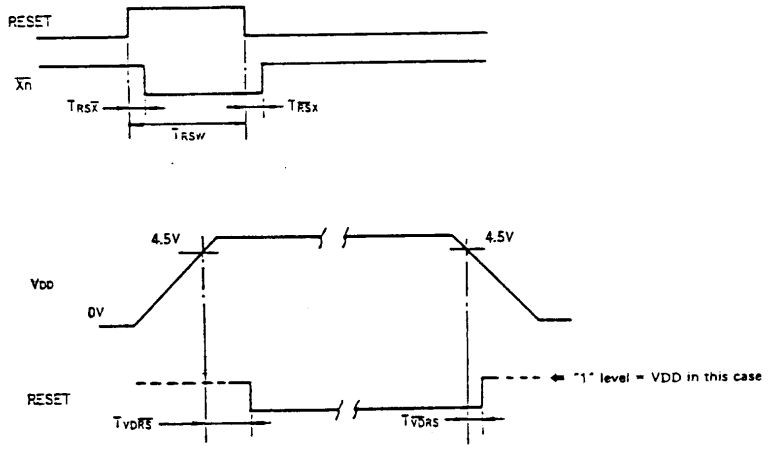
Note 12: The $\overline{\text{VDPCR}}$ and $\overline{\text{VDPCW}}$ signals marked with asterisks indicate the timing when "1" is applied to the $\overline{\text{X7}}$ pin during reset.
A 1 bit wait is inserted after Tw when "0" is applied to the $\overline{\text{X7}}$ pin during reset.

I/O cycle timing (2)



Note 13: The signal marked with an asterisk is the KBDIR output of MA18 when "1" is applied to the $\overline{X5}$ during reset.

Reset timing



14. External view

