YAMAHA LSI

V9958
MSX-VIDEO
TECHNICAL DATA BOOK

YAMAHA

V9958TECHNICAL DATA BOOK
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PREFACE

This booklet describes those specifications which have been added, modified or deleted on the basis of specifications of V9938. The ones not found here have remained the same as V9938 but note that some, even the same, may be included here due to the convenience of editing. For specifications of V9938, refer to "V9938 MSX-VIDEO Technical Data Book".

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Semiconductor Division

TABLE OF CONTENTS

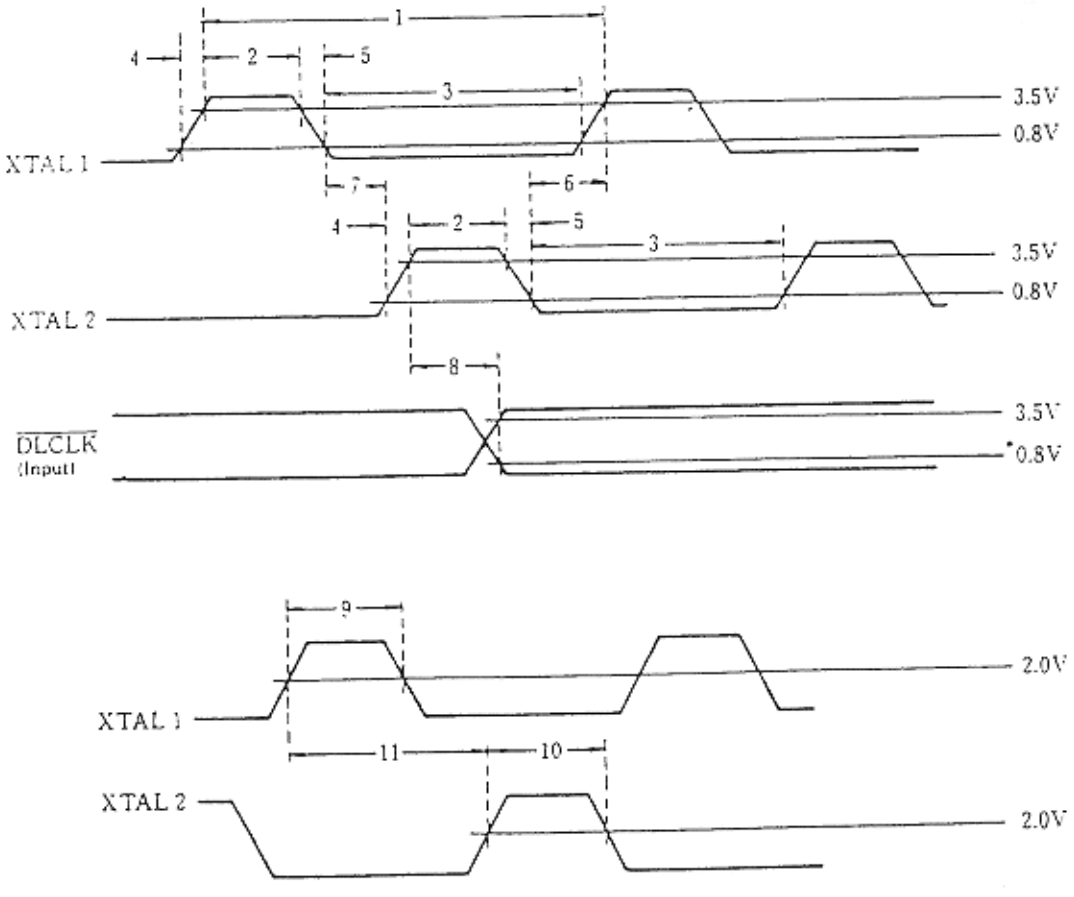
ページ

1 GENERAL DESCRIPTION 1
2 FEATURES 1
3 INTERNAL STRUCTURE BLOCK DIAGRAM 2
4 PIN LAYOUT AND FUNCTIONS 3
5 REGISTER DESCRIPTION 5
5-1 Added Registers 5
5-1-1 Horizontal Scroll Function 5
5-1-2 Wait Function 7
5-1-3 Command Function 8
5-1-4 YJK-Type Data Display Function 8
5-2 Modified Register 10
5-3 Deleted Functions 11
6 MODIFIED TERMINALS DESCRIPTION 12
7 ELECTRICAL CHARACTERISTICS 13
7-1 Maximum Ratings 13
7-2 Recommended Operating Conditions 13
7-3 Electrical Characteristics Under Recommended Operating Conditions 14
7-3-1 External Input Clock Timing 14
7-3-2 DC Characteristics 15
7-3-3 Input/Output Capacity 15
7-3-4 External Output Clock Timing 16
7-3-5 CPU-MSX-VIDEO Interface 17
7-3-6 MSX-VIDEO-VRAM Interface 20
7-3-7 RGB Output Level 23
7-3-8 Sync. Signal Output Level 23
7-3-9 RGB Signal AC Characteristics 23
7-3-10 Sync. Signal AC Characteristics 24
7-3-11 Color Bus 27
7-3-12 VDS 28
8 MSX-VIDEO CIRCUIT DIAGRAM 29
9 PACKAGE DIMENSIONAL DIAGRAM 30

7-3 Electrical Characteristics Under Recommended Operating Conditions

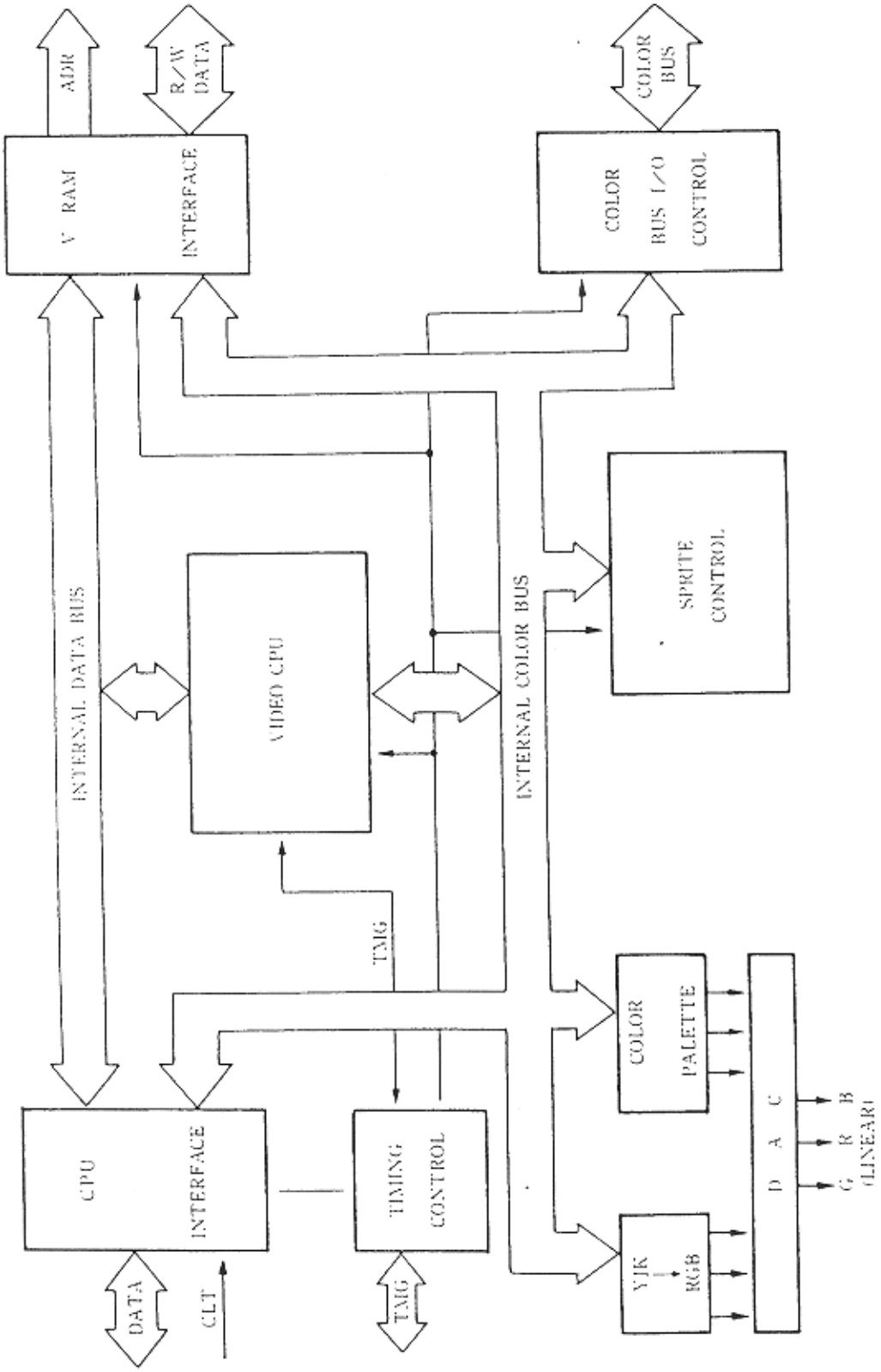
7-3-1 External Input Clock Timing

No.	Symbol	Item	Min.	Typ.	Max.	Unit
1	fXTAL	XTAL clock frequency	20.26	21.48	22.55	MHz
2	TXWH	XTAL clock high-level pulse width	5			ns
3	TXWL	XTAL clock low-level pulse width	5			ns
4	TXR	XTAL clock rise time			10	ns
5	TXF	XTAL clock fall time			10	ns
6	TXD21	XTAL clock delay time2→1	0			ns
7	TXD12	XTAL clock delay time1→2	0			ns
8	TLIXD	$\overline{DLCLK}$ (input)-XTAL clock delay time	20		50	ns
9	TW1	XTAL1 pulse width	12			ns
10	TW2	XTAL2 pulse width	20			ns
11	TPD	XTAL1-XTAL2 relative delay time	15		24	ns



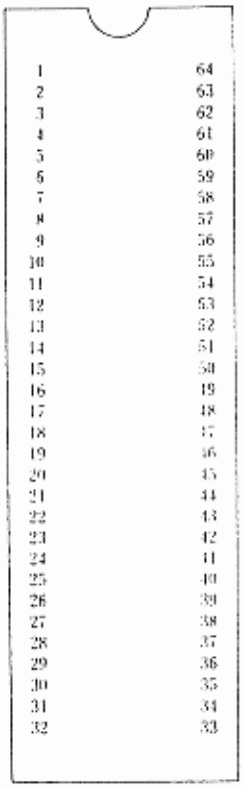
External Input Clock Timing

3 INTERNAL STRUCTURE BLOCK DIAGRAM



4 PIN LAYOUT AND FUNCTIONS

Pin Name	Pin No.	I/O	Function
CD0 LSB	40	I/O	CPU data bus
CD1	39	I/O	"
CD2	38	I/O	"
CD3	37	I/O	"
CD4	36	I/O	"
CD5	35	I/O	"
CD6	34	I/O	"
CD7 MSB	32	I/O	"
MODE 0	29	I	CPU interface-mode select
MODE 1	28	I	"
$\overline{CSR}$	31	I	CPU-MSX-VIDEO read strobe
$\overline{CSW}$	30	I	CPU-MSX-VIDEO write strobe
RD0 LSB	41	I/O	VRAM data bus
RD1	42	I/O	"
RD2	43	I/O	"
RD3	44	I/O	"
RD4	45	I/O	"
RD5	46	I/O	"
RD6	47	I/O	"
RD7 MSB	48	I/O	"
AD0 LSB	49	O	VRAM address bus
AD1	50	O	"
AD2	51	O	"
AD3	52	O	"
AD4	53	O	"
AD5	54	O	"
AD6	55	O	"
AD7 MSB	56	O	"
$\overline{RAS}$	62	O	VRAM row address strobe
$\overline{CAS\ 0}$	61	O	VRAM column address strobe 0 (first half of VRAM)
$\overline{CAS\ 1}$	60	O	VRAM column address strobe 1 (last half of VRAM)
$\overline{CAS\ X}$	59	O	VRAM column address strobe X (for expansion VRAM)
R/$\overline{W}$	57	O	VRAM write strobe
G	22	O	Linear RGB signal output
R	23	O	"
B	24	O	"
$\overline{YS}$	10	O	Signal for switching between MSX-VIDEO RGB output and external video signals. (For superimpose) $\overline{YS}$ = High: MSX-VIDEO output is transparent $\overline{YS}$ = Low ; MSX-VIDEO output is not transparent
BLEO	7	O	Indicates No. 1 field/No. 2 field blanking with 3-value output. Open drain output High ; No. 2 field and active. Middle: No. 1 field and active. Low ; Linear erase interval.



Pin Name	Pin No.	I/O	Function
$\overline{\text{HSYNC}}$	5	O	High: Timig other than HSYNC or color burst timing. Low : HSYNC or timing other than color burst.
$\overline{\text{CSYNC}}$	6	O	Composite SYNC output.
CBDR	11	O	Indicates color bus direction. High: Color bus is input Low : Color bus is output
C0 LSB	19	I/O	Color bus.
C1	18	I/O	Normally color code is output. Used as input port when digitizing.
C2	17	I/O	"
C3	16	I/O	"
C4	15	I/O	"
C5	14	I/O	"
C6	13	I/O	"
C7 MSB	12	I/O	"
$\overline{\text{DHCLK}}$	2	O	Dot clock output at high resolution. Approx. 10.74MHz open drain output.
$\overline{\text{DLCLK}}$	3	I/O	Dot clock output at low resolution. Approx. 5.37MHz open drain output. As input is also possible by using the mode register, it is used for multi MSX-VIDEO.
XTAL 1	63	I	Used for XTAL connection. Also used for input when using an externally generated clock.
XTAL 2	64	I	
CPUCLK/ $\overline{\text{VDS}}$	8	O	1/6 of XTAL frequency is output. VRAM data select $\overline{\text{VDS}}$ = Low : VRAM access for display data. $\overline{\text{VDS}}$ = High: VRAM access for other than the above.
$\overline{\text{INT}}$	25	O	CPU interrupt output, open drain output Low: Generates interrupt.
$\overline{\text{RESET}}$	9	I	Each circuit in MSX-VIDEO is initial reset.
$\overline{\text{VRESET}}$	4	I	VSYNC input.
$\overline{\text{HRESET}}$	27	I	HSYNC input.
$\overline{\text{WAIT}}$	26	O	Wait signal to CPU is output.
V_{DD}	58	I	5V power supply.
GND	1	I	Ground 0V.
GND•DAC	20	I	Ground 0V.
V_{DD}•DAC	21	I	5V power supply.
V_{BB}	33	O	Baseboard voltage.

5 REGISTER DESCRIPTION

5-1 Added Registers

Shown below are the registers newly added to the existing V9938 registers.

	b7	b6	b5	b4	b3	b2	b1	b0
#25		CMD	VDS	YAE	YJK	WTE	MSK	SP2
#26			HO8	HO7	HO6	HO5	HO4	HO3
#27						HO2	HO1	HO0

The above three registers are cleared to "0" by the RESET signal and if used in that state, will function compatibly with V9938.

#25 b7
#26 b6, b7
#27 b3～b7
} Make sure to set "0" for these empty bit positions.

5-1-1 Horizontal Scroll Function.

	b7	b6	b5	b4	b3	b2	b1	b0	
#25							MSK	SP2	
#26			HO8	HO7	HO6	HO5	HO4	HO3	by character units
#27						HO2	HO1	HO0	by dot units

HO8～HO0 Used to set the scroll volume of still pictures in the horizontal direction one dot at a time.
(In G5 and G6 modes, scrolling is in 2-dot units.)

SP2 0 : Sets the horizontal screeen size to 1 page. (Initial value)
Scrolling is done within one page and the non-displayed left side of the page is displayed on the right hand side of the screen.

1 : Sets the horizontal screen size to two pages.
Scrolling is done within 2 pages and if the first page is displayed first, then the second page will appear at the scroll operation.

MSK 0 : The left 8 dots are not masked. (Initial value)

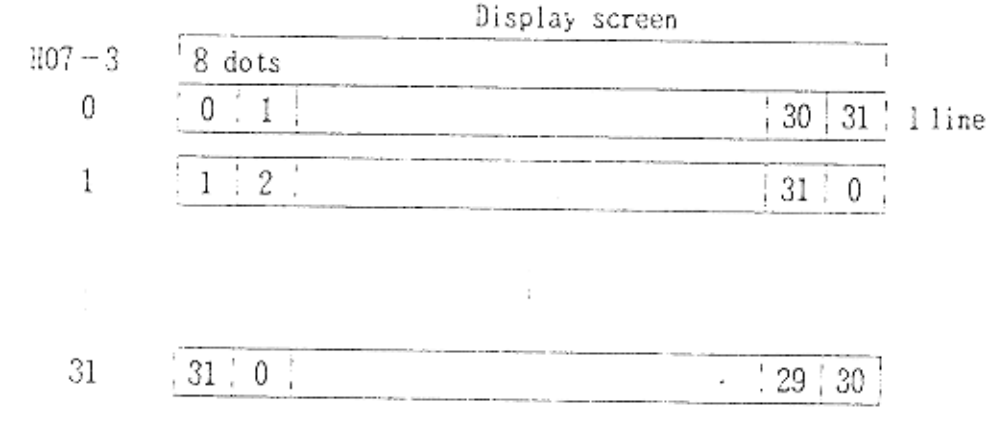
1 : The left 8 dots are masked and the border color is output.
There is no need to mask if the value in #27 is "0".
(In G5 and G6 modes, the number of masked dots is 16.)

During scrolling, once the dots disappear to the left of the screen or once the dots 1 to 7 appear on the screen, their data are not controlled by V9958 and there is no guarantee on what will be displayed.
To ensure proper display on the screen, therefore, masking is necessary.

◎ Screen dispaly for H08-H03

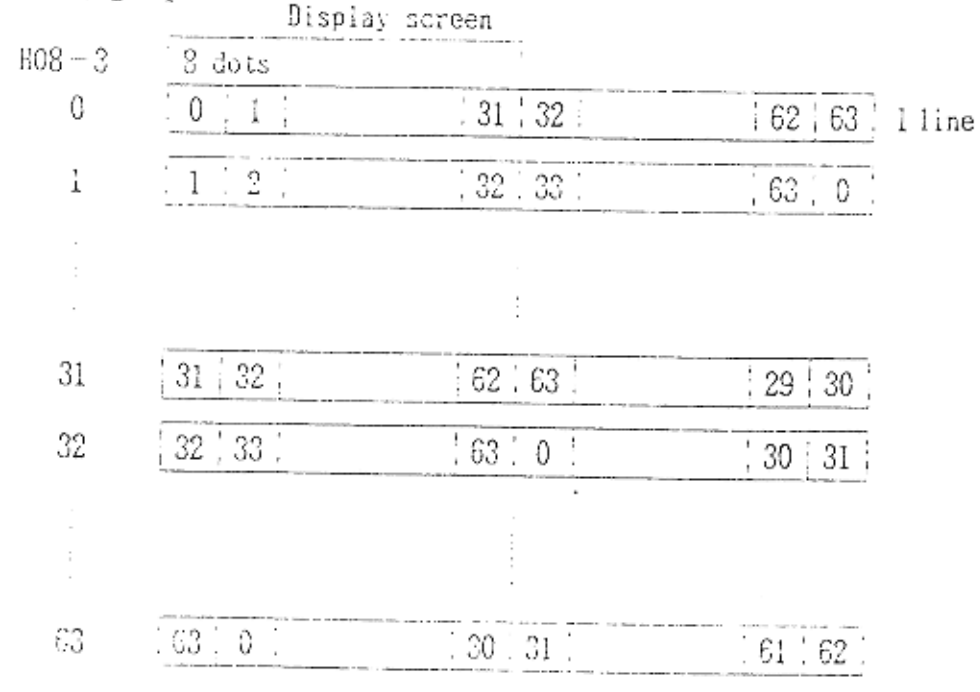
The screen is shifted to the left as specified in 8-dot units (in G5 and G6 modes, the screen is shifted in 16-dot units).

· When SP2 = 0



Note) H08 is ignored

· When SP2 = 1



Note) When SP2 = 1, bit 5 (A15) of the pattern name table base address register (R#2) should be set to "1".
The base address of each table will be as follows.

Pattern name table(PNT) : 0 to 31(when A15 is set to "0")
32 to 63(when A15 is set to "1")
Pattern generator table (PGT) : The base address remains unchanged even when scroll value is changed.
Color table (CT) : The base address remains unchanged even when scroll value is changed.

◎ Screen display for H02-H00
The screen is shifted to the right as specified in 1-dot unit (in G5 and G6 modes. the screen is shifted in 2-dot units).

(Example) ① When scrolling to the left one dot at a time

	RESET	Initial				
#26	0	1	1	.....	1	2 (Count up)
#27	0	7	6		0	7 (Count down)
		1 dot to the left	2 dots to the left		8 dots to the left	9 dots to the left

② When scrolling to the right one dot at a time

	RESET	Initial				
#26	0	0	0	.....	31	31 (Count down)
#27	0	1	2		0	1 (Count up)
		1 dot to the right	2 dots to the right		8 dots to the right	9 dots to the right

5-1-2 Wait Function (to speed up the writing time of data from CPU to VRAM)

	b7	b6	b5	b4	b3	b2	b1	b0
#25						WTE		

WTE 0 : Disables the WAIT function. (Initial value)
Works in the same way as V9938.
1 : Enables the WAIT function.
When the CPU accesses the VRAM, accesses to all ports on V9958 is held in the WAIT state until access to the VRAM of V9958 is completed.

However, WAIT function is not provided for incomplete access to the register and the color palette or for the data ready status of commands.

5-1-3 Command Function

	b7	b6	b5	b4	b3	b2	b1	b0
#25		CMD						

CMD 0 : The command function is not expanded.
The command function can be used only in G4 to G7 modes as with the conventional type. (Initial value)

1 : Enables the command function in all display modes.
In G4 to G7 modes, it works in the same way as with the conventional type and as G7 mode in any other mode. Therefore, it is necessary to set the parameters by using x-y coordinates of G7 mode.

5-1-4 YJK-Type Data Display Function

	b7	b6	b5	b4	b3	b2	b1	b0
#25				YAE	YJK			

YJK 0 : Handles the data on VRAM as RGB type data. (Initial value)
(Example : G7 mode = 3,3 and 2 bits each)
Displayed colors of the sprite are the same sa the conventional type.

1 : Handles the data on VRAM as YJK type data, converts them to RGB signals (5 bits each) and outputs them through RGB terminals as analog signals.
The color palette is used to display colors of the sprite in G7 mode.

YAE 0 : Without attributes

	C7	C6	C5	C4	C3	C2	C1	C0
1 dot	Y_1					KL		
1 dot	Y_2					KH		
1 dot	Y_3					JL		
1 dot	Y_4					JH		

: Indicates color data for 1 dot and color specification can be made up to 2^{17}.

YJK type data is categorized based on the data on 4 continuous dots as follows.

Y_1 · KL · KH · JL · JH : color data for the 1st dot
Y_2 · KL · KH · JL · JH : color data for the 2nd dot
Y_3 · KL · KH · JL · JH : color data for the 3rd dot
Y_4 · KL · KH · JL · JH : color data for the 4th dot

1 : With attributes

	C7 C6 C5 C4	C3	C2 C1 C0
1 dot	Y_1	A	KL
1 dot	Y_2	A	KH
1 dot	Y_3	A	JL
1 dot	Y_4	A	JH

A : Attribute

When A = 0

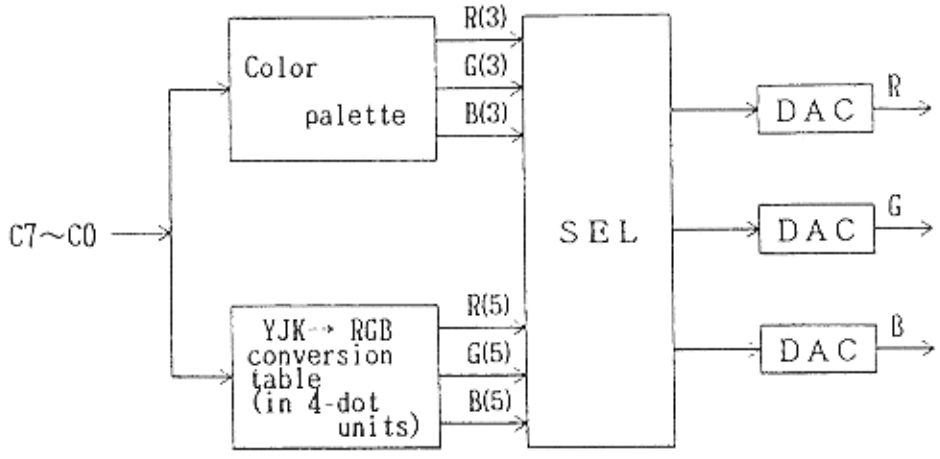
Just like when YAE="0", ▩ indicates color data for 1 dot and color specification can be made up to 2^{16}. (The "A" bit is ignored.)

When A = 1

Y_1, Y_2, Y_3, and Y_4 become color codes respectively and they are output as RGB signals through the color palette. (16 colors)
The KL, KH, JL and JH data are ignored then.

© Combination of YJK and YAE data

YJK	YAE	VRAM data
0	0	Via the conventional color palette
	1	Via the conventional color palette
1	0	Via the YJK → RGB conversion table
	1	A=0 : Via the YJK → RGB conversion table A=1 : Via the color palette



◎ The formulas for YJK-RGB conversion are as follows.

1) From YJK to RGB

$$R = Y + J$$

$$G = Y + K$$

$$B = \frac{5}{4}Y - \frac{J}{2} - \frac{K}{4}$$

2) From RGB to YJK

$$Y = \frac{B}{2} + \frac{R}{4} + \frac{G}{8}$$

$$J = R - Y$$

$$K = G - Y$$

5-2 Modified Register

Shown below is the register whose function has been modified from V9938.

	b7	b6	b5	b4	b3	b2	b1	b0	
S#1	FL	LPS	0	0	0	1	0	FH	Status Register 1
			ID#						

When the power is turned ON, the ID# is returned to b1 to b5 of the status register 1, indicating that V9938 is connected at "0" and V9958 is connected at "2".

5-3 Deleted Functions

1) Composite video output
2) Mouse/lightpen interface

As a result of these deletions, the following bits of the internal register become meaningless. Therefore, set these meaningless bits to "0" when writing into the registers.

	b7	b6	b5	b4	b3	b2	b1	b0	
R#0	0	DG	IE2	IE1	M5	M4	M3	0	Mode Register 0
R#8	MS	LP	TP	CB	VR	0	SPD	BW	Mode Register 2
S#1	FL	LPS			ID #			FH	Status Register 1

6 MODIFIED TERMINALS DESCRIPTION

The following table shows those terminals whose function has been modified and those whose function has been deleted and then newly added.

Pin No.	V9958		V9938		
	Terminal name	I/O	Terminal name	I/O	Remarks
4	$\overline{\text{VRESET}}$	I	$\overline{\text{VDS}}$	O	Added after deleted
5	$\overline{\text{HSYNC}}$	O	$\overline{\text{HSYNC}}$	I/O	Modified
6	$\overline{\text{CSYNC}}$	O	$\overline{\text{CSYNC}}$	I/O	Modified
8	CPUCLK/$\overline{\text{VDS}}$	O	CPUCLK	O	Modified
21	VDD/DAC	I	VIDEO	O	Added after deleted
26	$\overline{\text{WAIT}}$	O	$\overline{\text{LPS}}$	I	Added after deleted
27	$\overline{\text{HRESET}}$	I	$\overline{\text{LPD}}$	I	Added after deleted

The rest of the terminals remain the same as those of V9938.

1. Deleted terminal
   - VIDEO
   - LPS
   - LPD
   - VDS

2. Added terminal function
   - VDD/DAC ⇨ Analog power source
   - WAIT ⇨ I/O WAIT output
   - HRESET, VRESET ⇨ Tri-level logic input of HSYNC and CSYNC separated.

3. Modified terminal functions
   - HSYNC ⇨ HSYNC output or burst flag output
   - CSYNC ⇨ CSYNC output
   - CPUCLK/VDS⇨ CPUCLK output or VDS output

© Output selection between CPUCLK and $\overline{\text{VDS}}$

	b7	b6	b5	b4	b3	b2	b1	b0
#25			VDS					

VDS 0 : The CPUCLK signal is output. (Initial value)
1 : The VDS signal is output.

7 ELECTRICAL CHARACTERISTICS

7-1 Maximum Ratings

Symbol	Item	Rating	Unit
V_{DD}	Power supply voltage	−0.5 − +7.0	V
Vin	Input voltage	−0.5 − +7.0	V
Ts	Storage temperature	−50 − +125	°C
To	Operating temperature	0 − +70	°C

7-2 Recommended Operating Conditions

Symbol	Item	Minimum	Typical	Maximum	Unit
V_{DD}	Power supply voltage	4.75	5.00	5.25	V
V_{SS}	Power supply voltage		0		V
T_A	Operating ambient temperature	0		70	°C
V_{IL} 1	Low level input voltage (group 1)	−0.3		0.8	V
V_{IL} 2	Low level input voltage (group 2)	−0.3		0.8	V
V_{IL} 3	External clock low level input voltage (group 3)	−0.3		0.6	V
V_{IH} 1	High level input voltage (group 1)	2.2		V_{DD}	V
V_{IH} 2	High level input voltage (group 2)	2.2		V_{DD}	V
V_{IH} 3	External clock high level input voltage (group 3)	3.5		V_{DD}	V

Note: Group 1 $\overline{CSR}$, RD0-7, C0-7, $\overline{LPS}$, $\overline{LPD}$, $\overline{RESET}$, $\overline{DLCLK}$, $\overline{VRESET}$, $\overline{HRESET}$
Group 2 CD0-7, MODE 0, MODE 1, $\overline{CSW}$
Group 3 XTAL 1, XTAL 2

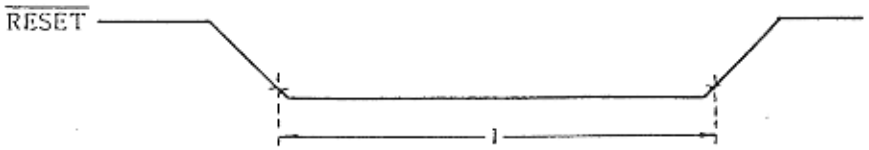
1 GENERAL DESCRIPTION

This LSI is a video display Processor(VDP) which is applicable to new media. It uses an N-channel silicon gate MOS and has a linear RGB output. It is software compatible with TMS9918A and V9938.

2 FEATURES

- 5V power supply.
- Outputs linear RGB.
- Built-in color palette for display in up to 512 colors.
- Capable of simultaneous display of 19,268 colors by using YJK system display.
- Capable of displaying up to 512×424 Pixels and 16 colors.
- Bit mapped graphics.
- Capable of displaying maximum of 256 colors simultaneously.
- 16K byte～128K byte useable for display memory.
- 16K×1b,16K×4b,64K×1b and 64K×4b DRAMs are useable.
- 256 addresses,4ms auto refresh function of DRAM.
- Expansion video memory can be connected.
- Eight sprites can be displayed for each horizontal line.
- Colors for sprites can be specified for each horizontal line.
- Area move, line, search and other commands.
- Command function usable in every display mode.
- Logical operation function.
- Addresses can be specified by coordinates.
- Capable of external synchronization.
- Capable of superimposition.
- Capable of digitization.
- Multi MSX-VIDEO configurations are possible.
- External color palettes can be added by utilizing color bus output.
- Vertical and horizontal scroll function.
- Wait function to CPU.

$\overline{\text{RESET}}$ Input Timing



No.	Symbol	Item	Min.	Typ.	Max.	Unit
1	TRESET	$\overline{\text{RESET}}$ low level pulse width	10			ms

7-3-2 DC Characteristics

Symbol	Item	Condition	Minimum	Typical	Maximum	Unit
VOL 4	Low level output voltage (group 4)	IOL = 1.6mA			0.4	V
VOL 5	Low level output voltage (group 5)	IOL = 1.6mA			0.4	V
VOL 6	Low level output voltage (group 6)	IOL = 10mA			0.4	V
VOL 7	Low level output voltage (group 7)	IOL = 1.6mA			0.4	V
VOH 4	High level output voltage (group 4)	IOH = 100μA	2.4			V
VOH 5	High level output voltage (group 5)	IOH = 60μA	2.7			V
ILI	Input leak current				10	μA
ILO	Output leak current (when floating)				25	μA
IDD	Current consumption				230	mA

Note: Group 4 $\overline{\text{CD0-7}}$, $\overline{\text{RD0-7}}$, $\overline{\text{AD0-7}}$, $\overline{\text{VDS}}$, CBDR, CPUCLK/$\overline{\text{VDS}}$, $\overline{\text{C0-7}}$, $\overline{\text{HSYNC}}$, $\overline{\text{CSYNC}}$, $\overline{\text{WAIT}}$, $\overline{\text{YS}}$
Group 5 $\overline{\text{RAS}}$, $\overline{\text{CAS 0}}$, $\overline{\text{CAS 1}}$, $\overline{\text{CASX}}$, R/$\overline{\text{W}}$
Group 6 $\overline{\text{DLCLK}}$, $\overline{\text{DHCLK}}$
Group 7 $\overline{\text{INT}}$

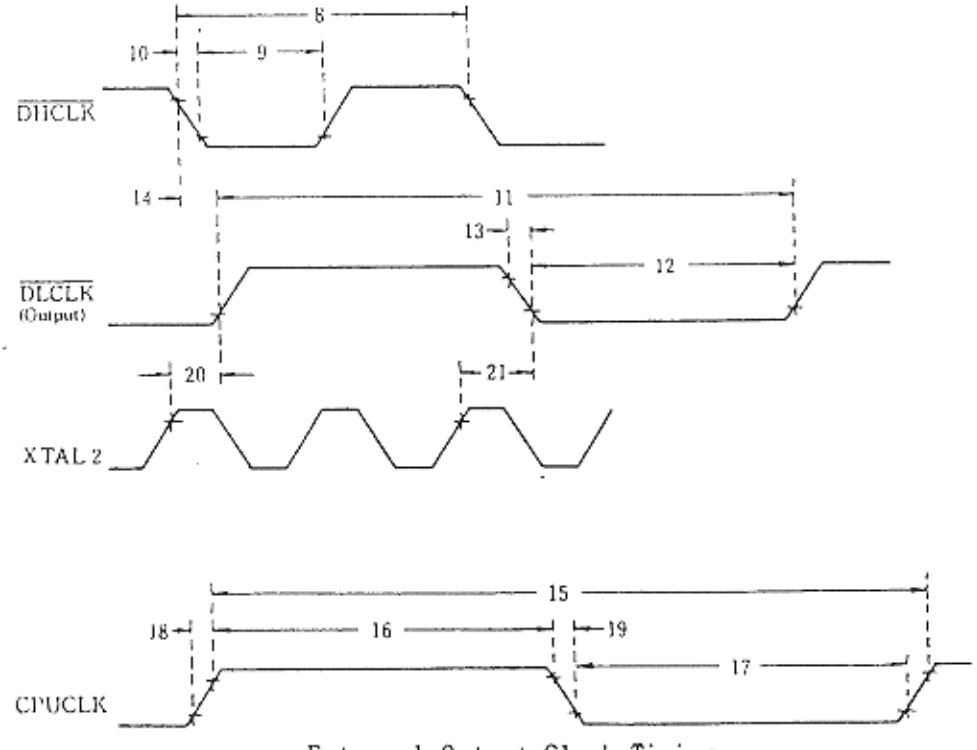
7-3-3 Input/Output Capacity

Symbol	Item	Condition	Min.	Typ.	Max.	Unit
CIN	Input capacity	VIN =0 V			10	PF
COUT	Output capacity	VOUT=0 V			10	PF

7-3-4 External Output Clock Timing

No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
8	fDHCLK	$\overline{DHCLK}$ frequency	CL=50 PF	10.13	10.74	11.28	MHz
9	THWL	$\overline{DHCLK}$ low-level pulse width		20			ns
10	THF	$\overline{DHCLK}$ fall time				25	ns
11	fDLCLK	$\overline{DLCLK}$ frequency		5.06	5.37	5.64	MHz
12	TLOWL	$\overline{DLCLK}$(output) low-level pulse width		60			ns
13	TLOF	$\overline{DLCLK}$(output) fall time				15	ns
14	THLOD	$\overline{DHCLK}$-$\overline{DLCLK}$(output) delay time		-15		15	ns
15	fCPUCLK	CPUCLK frequency	CL=100PF	3.37	3.58	3.76	MHz
16	TCWH	CPUCLK high-level pulse width		110			ns
17	TCWL	CPUCLK low-level pulse width		110			ns
18	TCR	CPUCLK rise time				25	ns
19	TCF	CPUCLK fall time				25	ns
20	TLOHXD	$\overline{DLCLK}$(output) high-XTAL delay time	CL=50PF	20		50	ns
21	TLOLXD	$\overline{DLCLK}$(output) low-XTAL delay time		20		50	ns

Note : The values shown for $\overline{DHCLK}$ and $\overline{DLCLK}$ assume that RL = 1 k ohm.

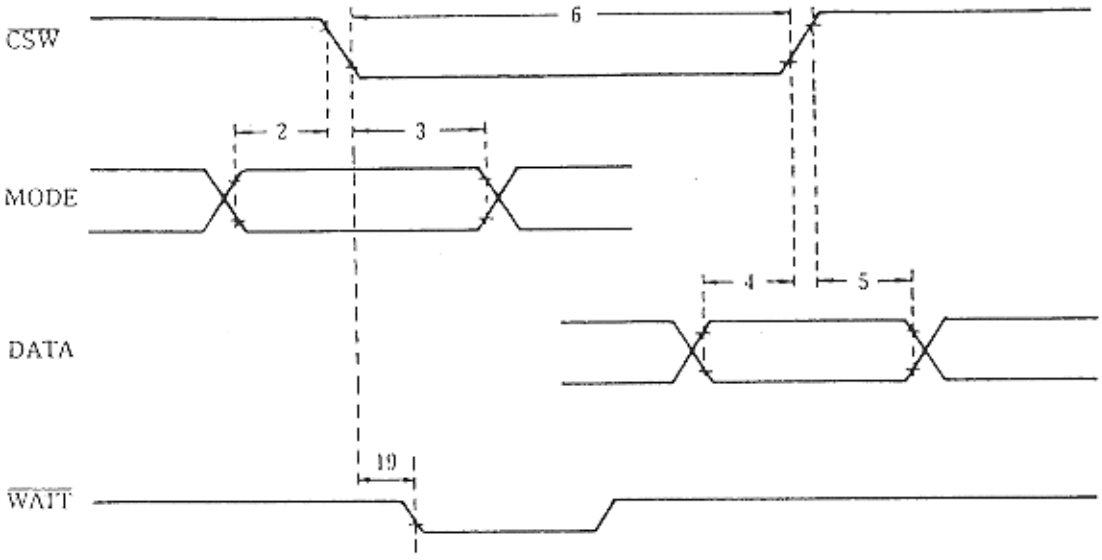


External Output Clock Timing

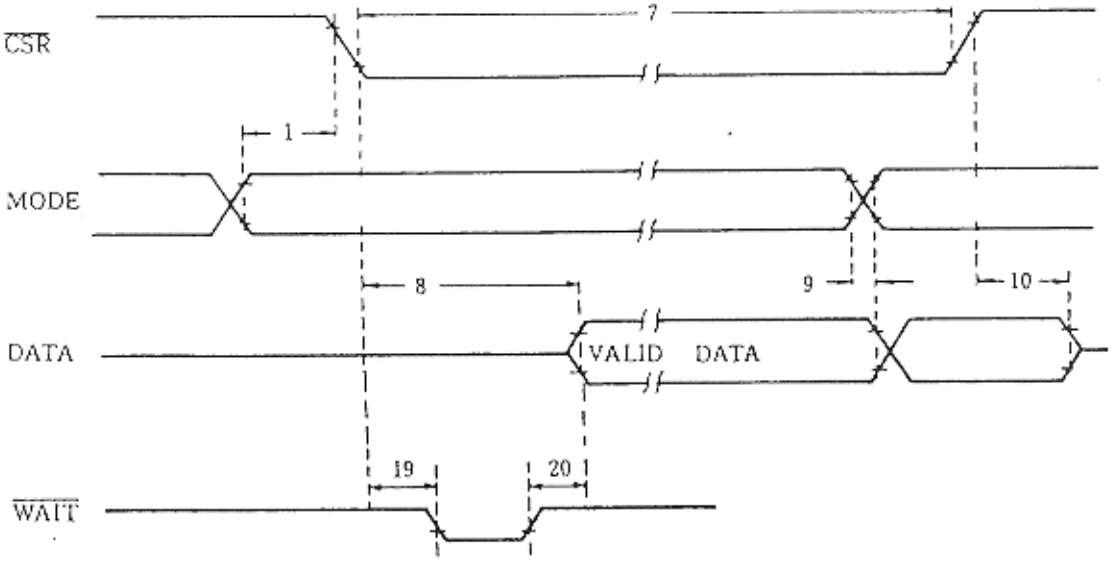
7-3-5 CPU-MSX-VIDEO Interface

No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
1	TASR	Address setup time (related to $\overline{CSR}$)		0			ns
2	TASW	Address setup time (related to $\overline{CSW}$)		30			ns
3	TAHW	Address hold time		50			ns
4	TDSW	Data setup time		30			ns
5	TDHW	Data hold time		30			ns
6	TCSW	$\overline{CSW}$ pulse width		186	700	2000	ns
7	TCSR	$\overline{CSR}$ pulse width		186	700	2000	ns
8	TRAC	Data access time	CL=300PF		100	150	ns
9	TPVX,A	Data invalid time		0			ns
10	TPVX	Data disable time			65	100	ns
11	TW1W	$\overline{CSW}$ pulse width high, 2nd-1st, 1st-2nd byte		2			us
12	TW2W	$\overline{CSW}$ pulse width high, 2nd-3rd, 3rd-3rd, 3rd-1st byte		8			us
13	TS1RW	$\overline{CSR}$-$\overline{CSW}$ setup time, 1st-1st byte		2			us
14	TS2RW	$\overline{CSR}$-$\overline{CSW}$ setup time, 3rd-1st byte		8			us
15	TS1WR	$\overline{CSW}$-$\overline{CSR}$ setup time, 2nd-1st byte		2			us
16	TS2WR	$\overline{CSW}$-$\overline{CSR}$ setup time, 2nd-3rd byte		8			us
17	TW1R	$\overline{CSR}$ pulse width high, 1st-1st byte		2			us
18	TW2R	$\overline{CSR}$ pulse width high, 3rd-1st, 3rd-3rd byte		8			us
19	TWCS	$\overline{WAIT}$ delay time (for $\overline{CSR}$ and $\overline{CSW}$)				120	ns
20	TRACW	Data access time (from $\overline{WAIT}$)				100	ns

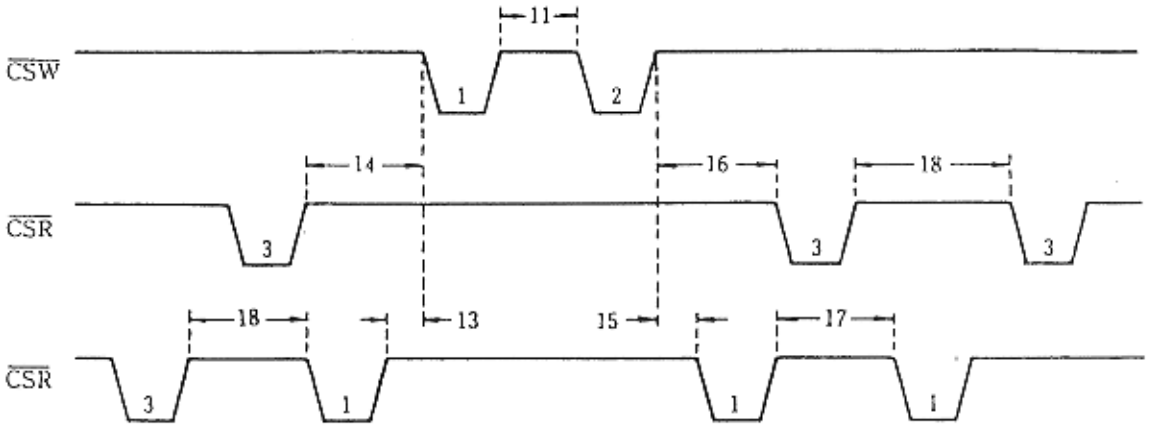
Note) 8 indicates the value when $\overline{WAIT}$ does not become low.



CPU-MSX-VIDEO Write Cycle Interface

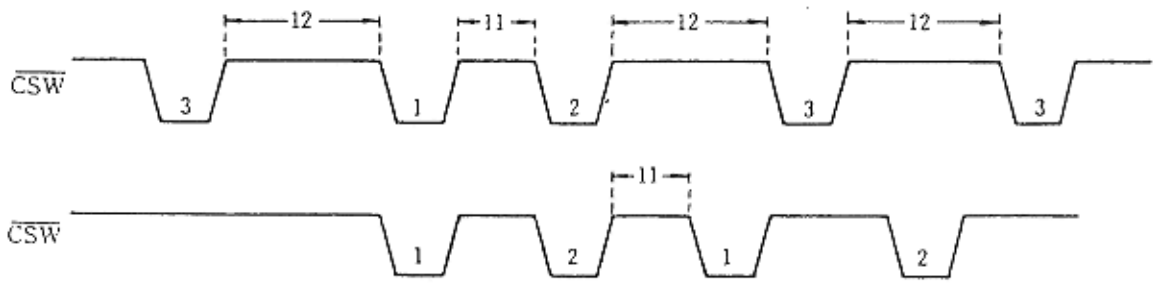


CPU-MSX-VIDEO Read Cycle Interface



Note) The value n (n=1,2,3) in each pulse indicates the "n"th byte transmitted from CPU.

MSX-VIDEO Register Read Timing

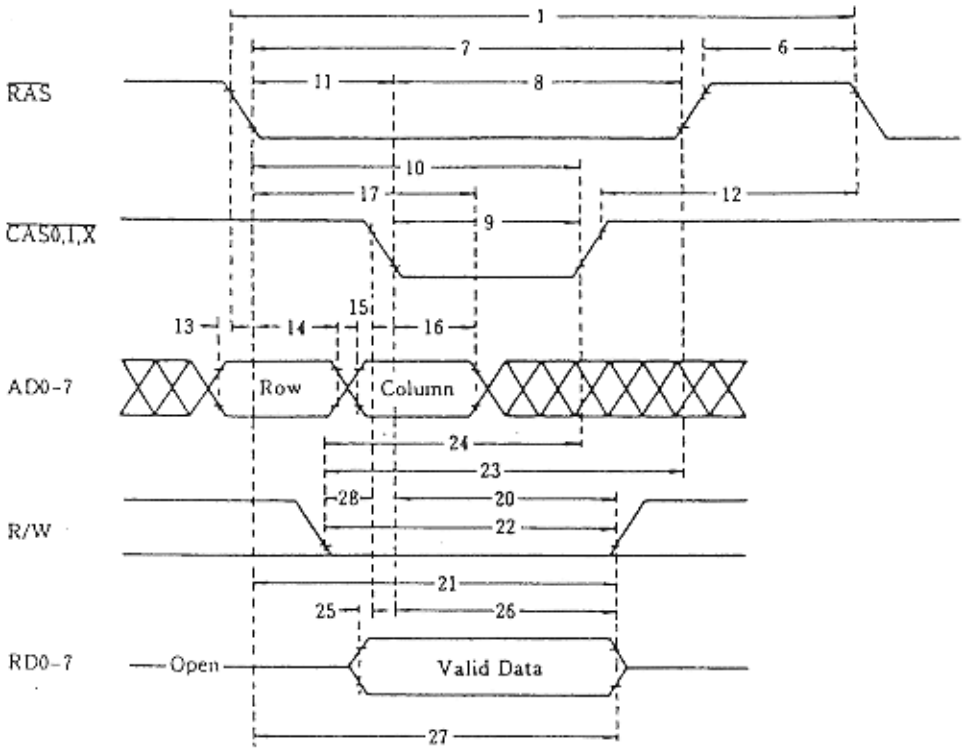


Note) The value n (n=1,2,3) in each pulse indicates the "n"th byte transmitted from CPU.

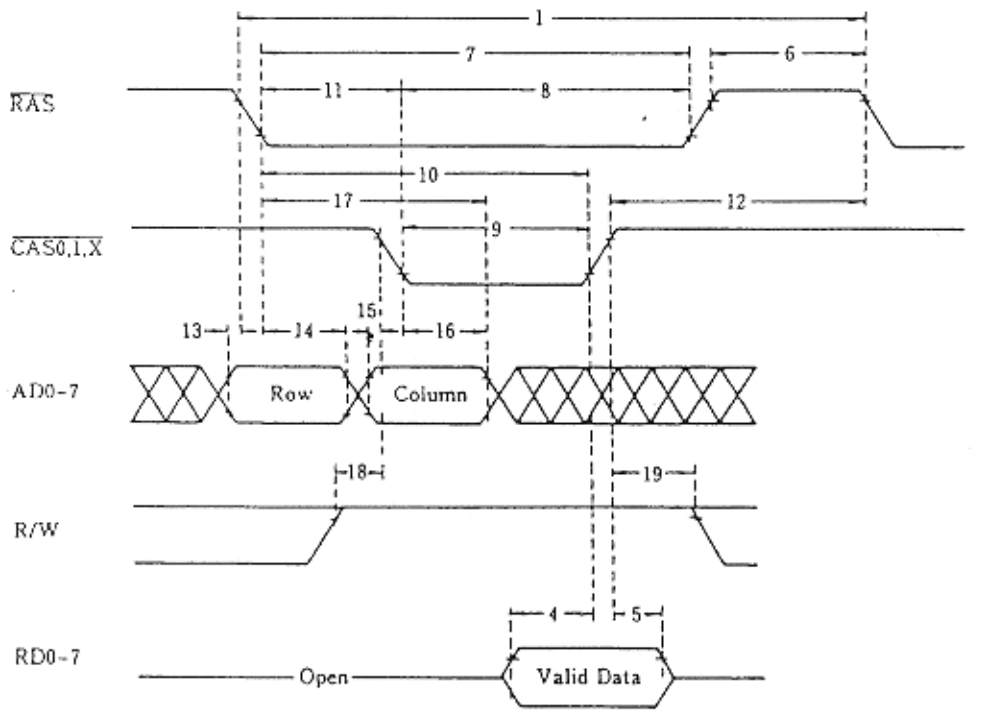
MSX-VIDEO Register Write Timing

7-3-6 MSX-VIDEO-VRAM Interface

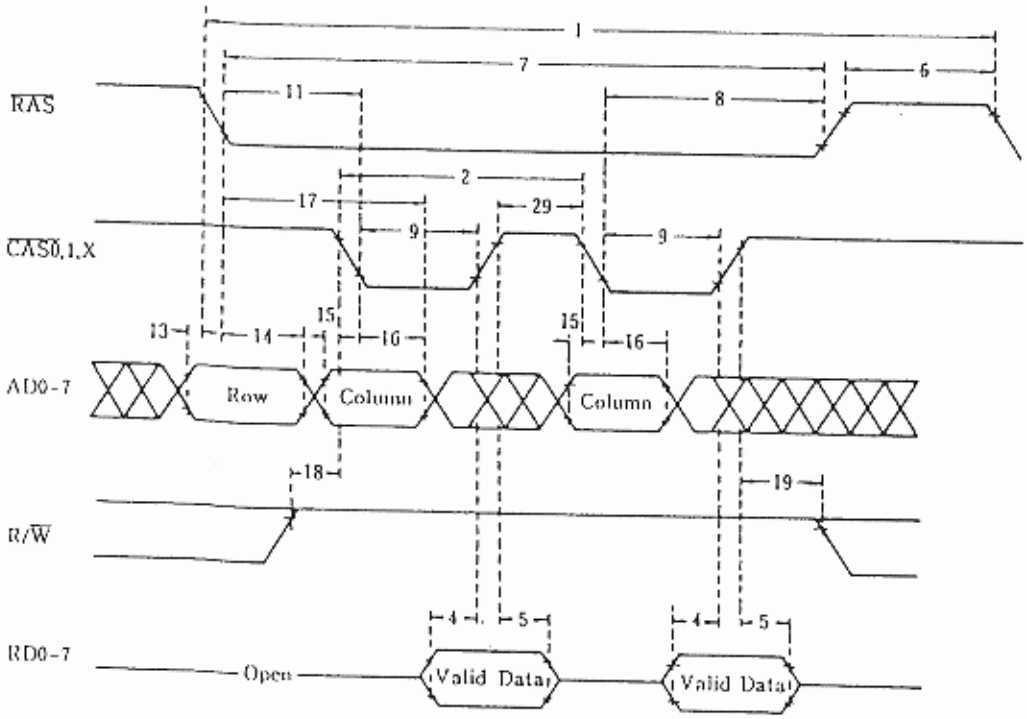
No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
1	TRC	Memory read/write cycle time		266	279		
2	TPC	Page mode cycle time		177	186		
4	TDSC	Read data setup time		20			
5	TDHC	Read data hold time		0			
6	TRP	$\overline{RAS}$ precharge time		90			
7	TRAS	$\overline{RAS}$ pulse width		130			
8	TRSH	$\overline{RAS}$ hold time		60			
9	TCAS	$\overline{CAS}$ pulse width		85			
10	TCSH	$\overline{CAS}$ hold time		140			
11	TRCD	$\overline{RAS}$-$\overline{CAS}$ delay time		40			
12	TCRP	$\overline{CAS}$-$\overline{RAS}$ precharge time		90			
13	TRARD	Row address-$\overline{RAS}$ delay time		50			
14	TRAH	Row address hold time		12			
15	TCACD	Column address-$\overline{CAS}$ delay time	CL=130PF	0			
16	TCAH	Column address hold time		100			ns
17	TCAR	Column address hold time(for $\overline{RAS}$)		130			
18	TRCD	Read command-$\overline{CAS}$ delay time		30			
19	TRCH	Read command hold time		30			
20	TWCH	Write command hold time		70			
21	TWRH	Write command hold time (for $\overline{RAS}$)		150			
22	TWP	Write command pulse width		120			
23	TRWL	Write command-$\overline{RAS}$ read time		150			
24	TCWL	Write command-$\overline{CAS}$ read time		120			
25	TDCD	Write data-$\overline{CAS}$ delay time		0			
26	TDH	Write data hold time		50			
27	TDHR	Write data hold time (for $\overline{RAS}$)		110			
28	TWCD	Write command-$\overline{CAS}$ delay time		30			
29	TCP	$\overline{CAS}$ precharge time (page mode cycle)		70			



VRAM Write Cycle (Early Write)



VRAM Read Cycle



VRAM Page Mode Cycle

7-3-7 R.G.B. Output Level

Symbol	Item	Measurement Conditions	Minimum	Typical	Maximum	Unit
VRGB 31	R.G.B. maximum output voltage	RL = 470Ω	2.8	3.1	3.5	V
VRGB 0	R.G.B. minimum output voltage (black level)		1.9	2.2	2.5	V
VP-P	R.G.B. VRGB31-VRGB0 potential difference		0.8	0.9	1.1	V
DRGB	R.G.B. VP-P deviation				5.0	%

*Typical values are given under conditions of V_{DD} = 5.00V, T_A = 25°C.

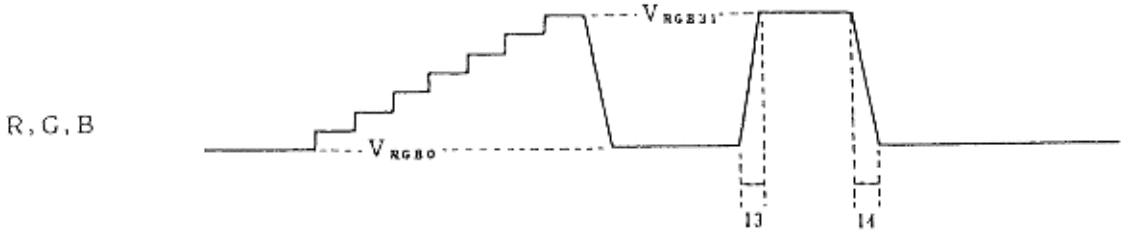
7-3-8 Sync Signal Output Level

Symbol	Item	Measurement Conditions	Minimum	Typical	Maximum	Unit
V_{TLVH} 1	3-value output high level BLEO	RL = 1KΩ	4.5		V_{DD}	V
V_{TLVM} 1	3-value output intermediate level BLEO		2.5		3.5	V
V_{TLVL} 1	3-value output low level BLEO				0.4	V

7-3-9 R.G.B. Signal AC Characteristics

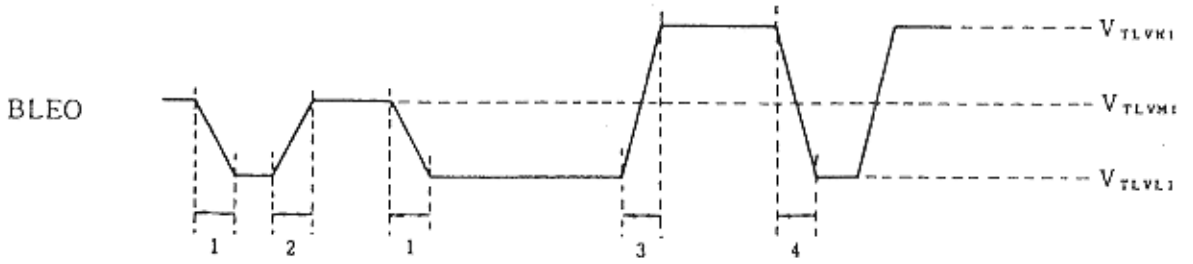
No.	Symbol	Item	Measurement Conditions	Minimum	Typical	Maximum	Unit
13	TrRGB	R.G.B. signal rise time (VRGB0→VRGB31)	RL = 470Ω CL = 150pF			60	ns
14	TfRGB	R.G.B. signal fall time (VRGB31→VRGB0)				60	ns

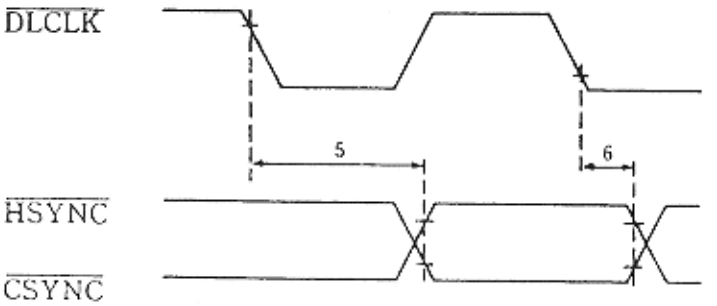
Note) Measurement is 10%→90%

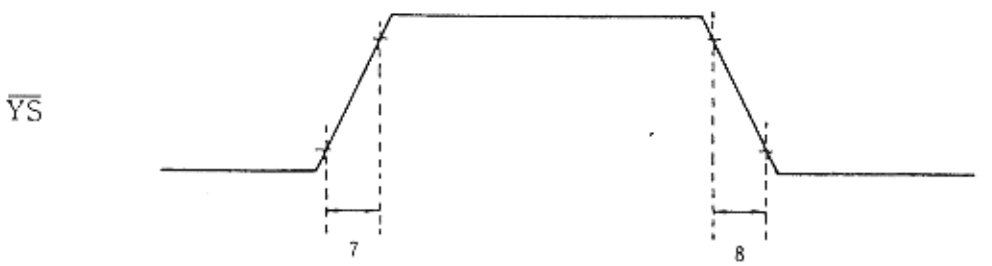


7-3-10 Sync. Signal AC Characteristics

No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
1	TfSY 1	BLEO intermediate level-low level fall time	CL=50PF			100	ns
2	TrSY 1	BLEO low level-intermediate level rise time				140	
3	TrSY 2	BLEO low level-high level rise time				220	
4	TfSY 2	BLEO high level-low level fall time				110	
5	TDSY	$\overline{\text{CSYNC}}$, $\overline{\text{HSYNC}}$ Output delay time				100	
6	THSY	$\overline{\text{CSYNC}}$, $\overline{\text{HSYNC}}$ Output hold time		20			
7	TrSY 6	$\overline{\text{YS}}$ rise time				25	
8	TfSY 6	$\overline{\text{YS}}$ fall time				25	

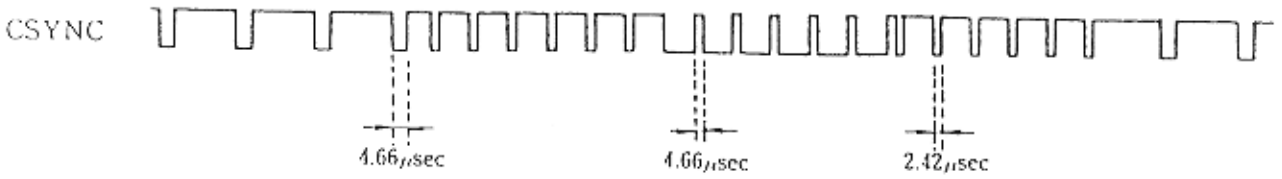

BLEO
V_{TLVH1}
V_{TLVM1}
V_{TLVL1}
1
2
1
3
4


$\overline{DLCLK}$
5
6
$\overline{HSYNC}$
$\overline{CSYNC}$

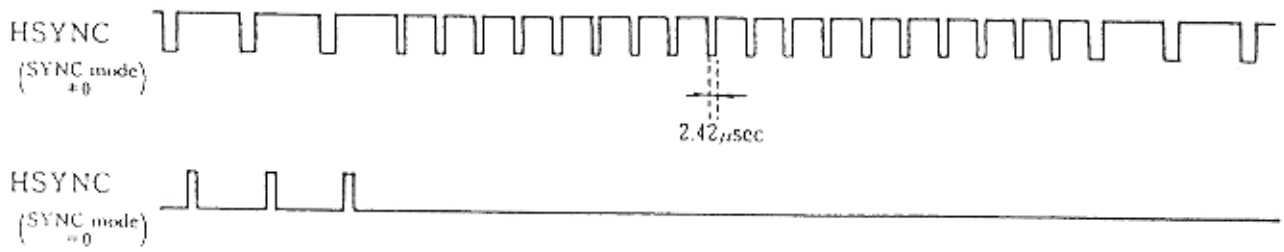

$\overline{YS}$
7
8



1st Field

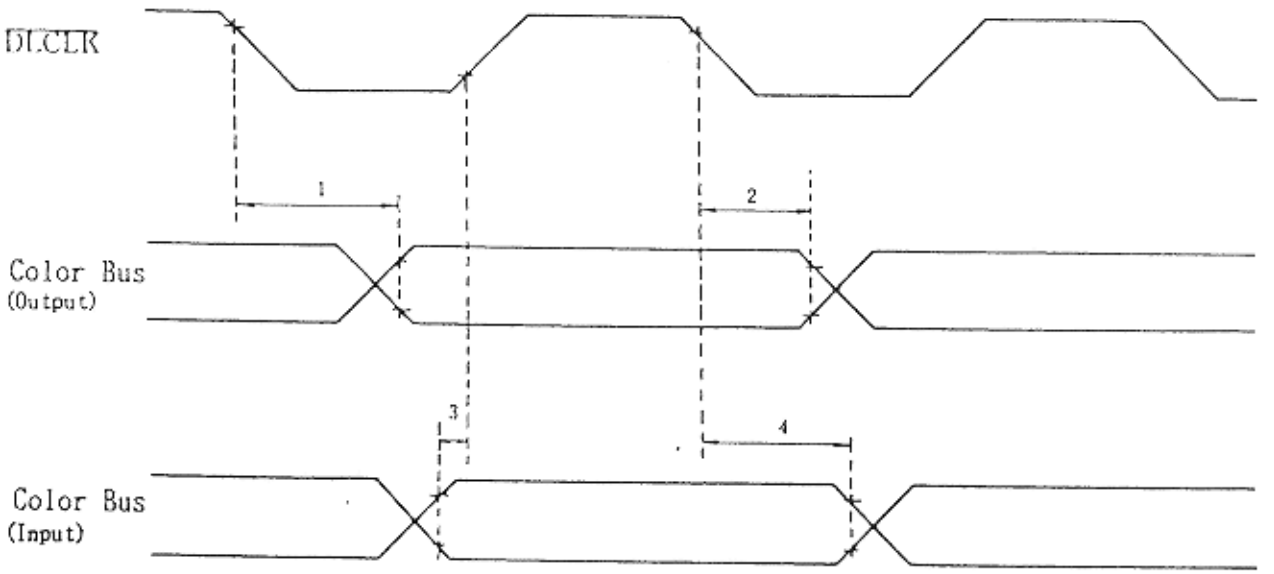


2nd Field



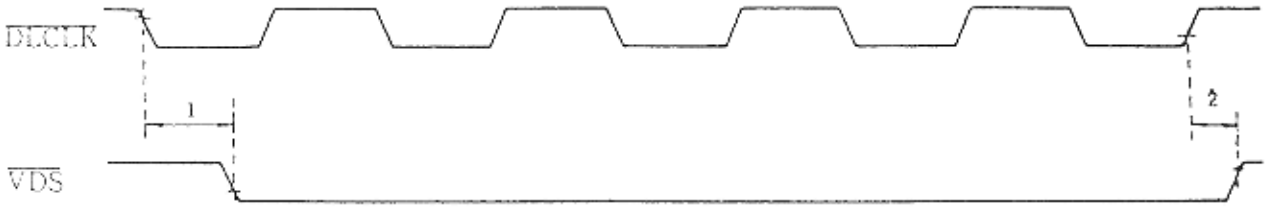
7-3-11 Color Bus

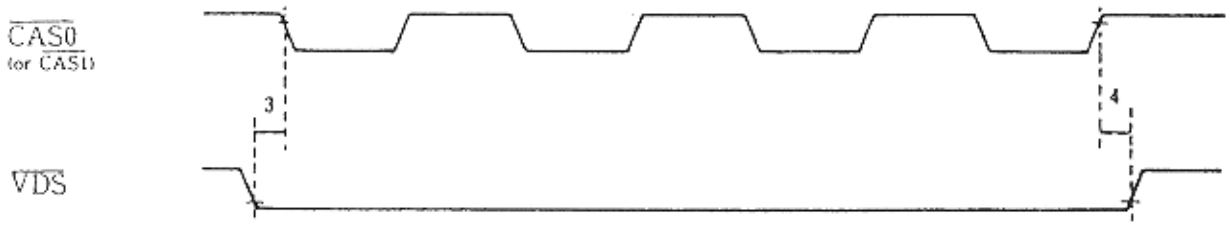
No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
1	TDCBO	$\overline{\text{DLCLK}}$-color bus output delay time	CL=50PF			190	ns
2	THCBO	$\overline{\text{DLCLK}}$-color bus output hold time		40			
3	TSCBI	Color bus input setup time		0			
4	THCBI	Color bus input hold time		20			



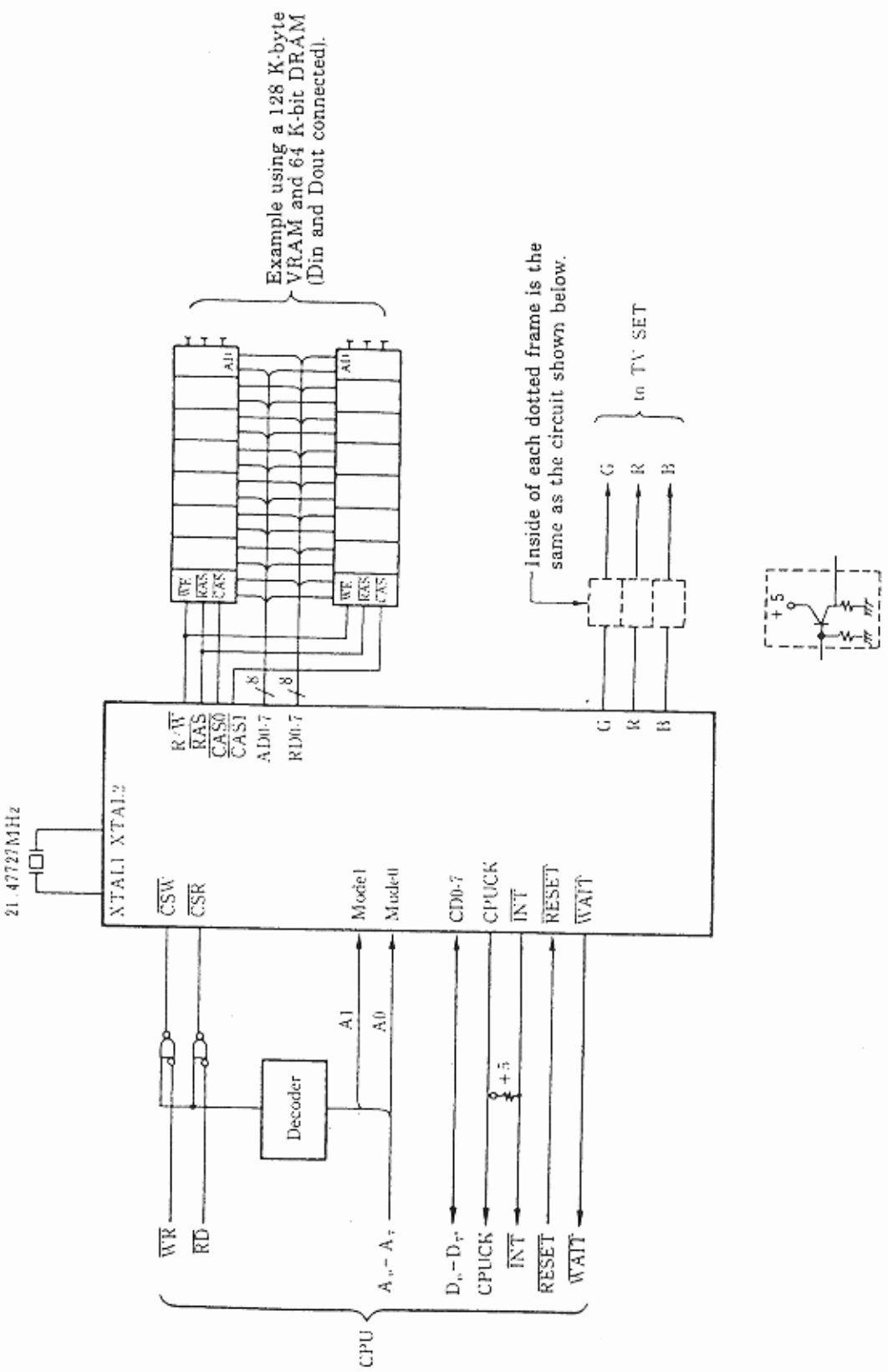
7-3-12 VDS

No.	Symbol	Item	Condition	Min.	Typ.	Max.	Unit
1	TDVDSL	$\overline{DLCLK}$-$\overline{VDS}$ low level delay time	CL=50PF	50		100	ns
2	TDVDSH	$\overline{DLCLK}$-$\overline{VDS}$ high level delay time		50		100	
3	TSVDS	$\overline{VDS}$ setup time (for $\overline{CAS0}$ and $\overline{CAS1}$)		20			
4	THVDS	$\overline{VDS}$ hold time (for $\overline{CAS0}$ and $\overline{CAS1}$)		0			

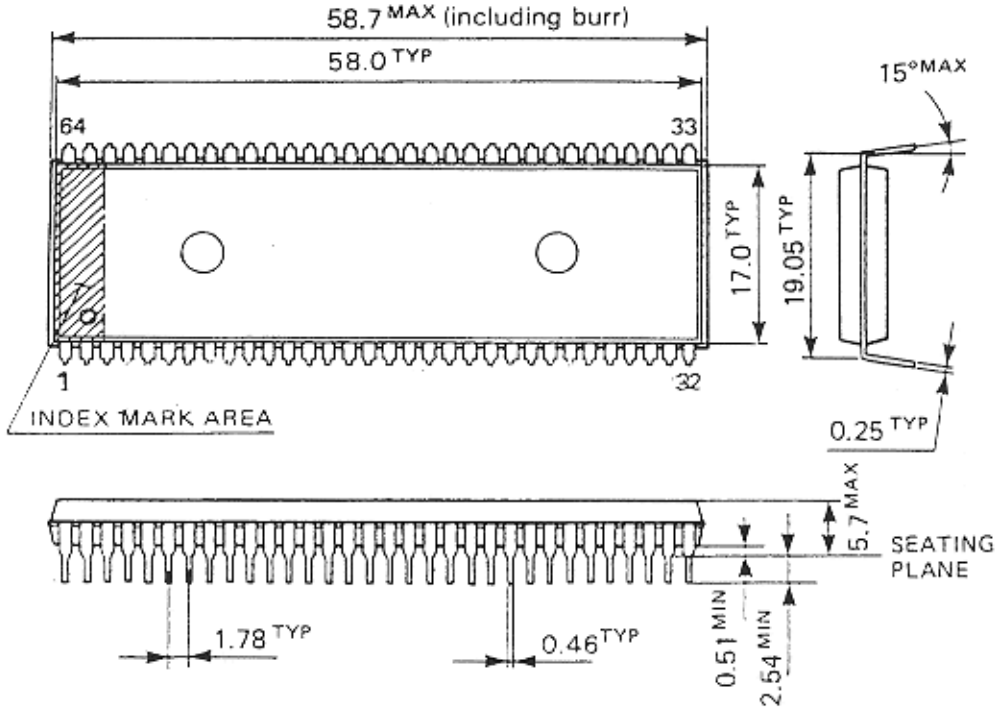




8 MSX-VIDEO CIRCUIT DIAGRAM



9 PACKAGE DIMENSIONAL DIAGRAM



DIMENSIONS IN MM

The specifications of this product are subject to improvement changes without prior notice.

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