
ATARI
CENTIPEDE



1000 POINTS



100 POINTS

10 POINTS



1 POINT



200 POINTS



? POINTS

ATARI®

- Shoot to destroy advancing creatures for points.
- Collisions with any creature will destroy you.
- In a two player game, players alternate until his supply of lives is exhausted.
- Hold fire button down for repetitive fire.

INSTRUCTIONS

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ATARI®

Drawing Package Supplement

to

Centipede™

Operation, Maintenance and Service Manual

Contents of this Drawing Package

Game Coin Door and Power Supply Wiring Diagram	Sheet 1, Side A
Microprocessor, Signature Analysis Procedure, Sync Generator, CAT Box™, and Power Inputs	Sheet 1, Side B
Playfield Address Selector, Playfield Memory and Playfield Code Multiplexer	Sheet 2, Side A
Coin Door Inputs, Switch Inputs, Video Outputs and Trak Ball™ Circuitry	Sheet 2, Side B

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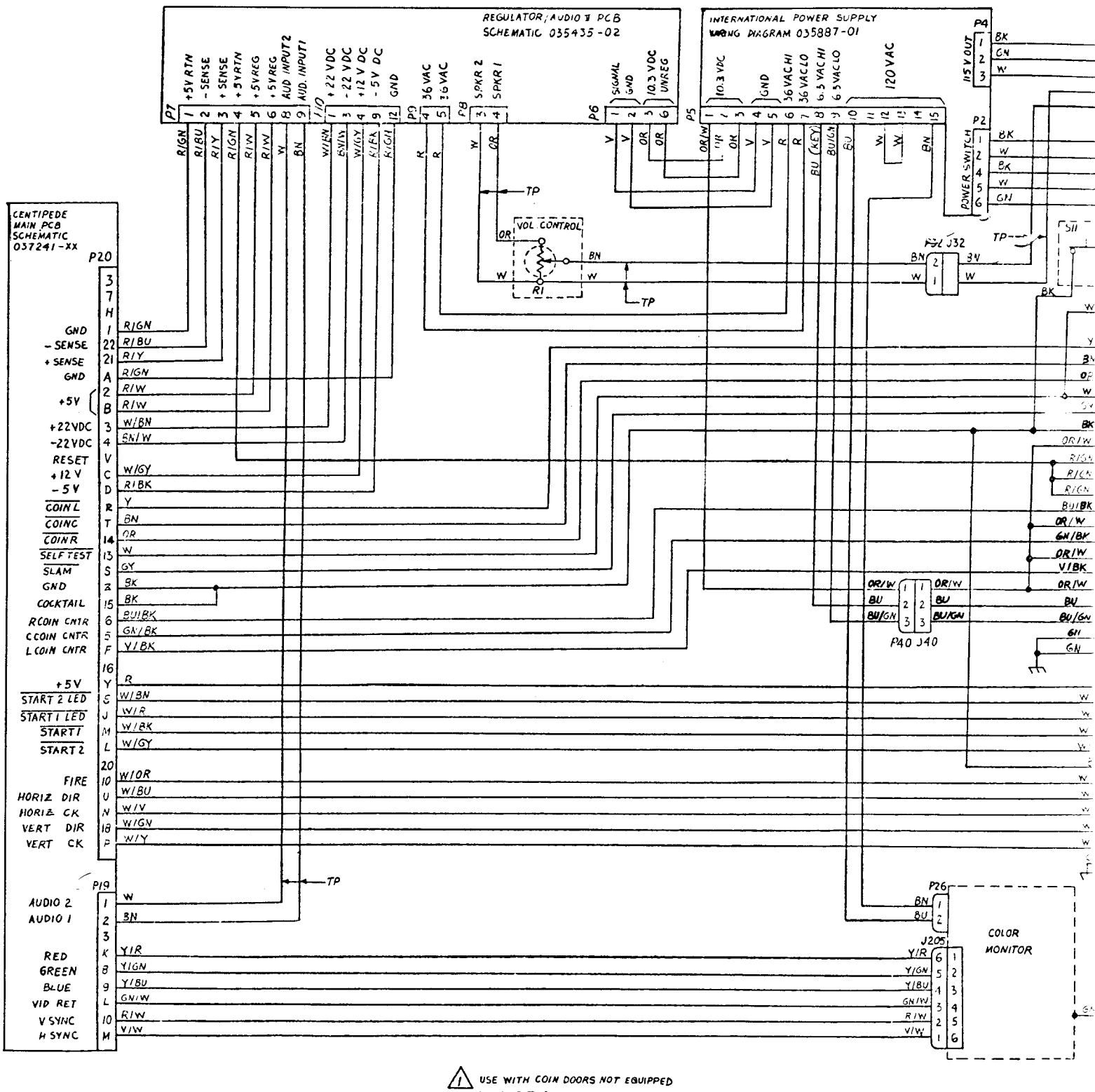
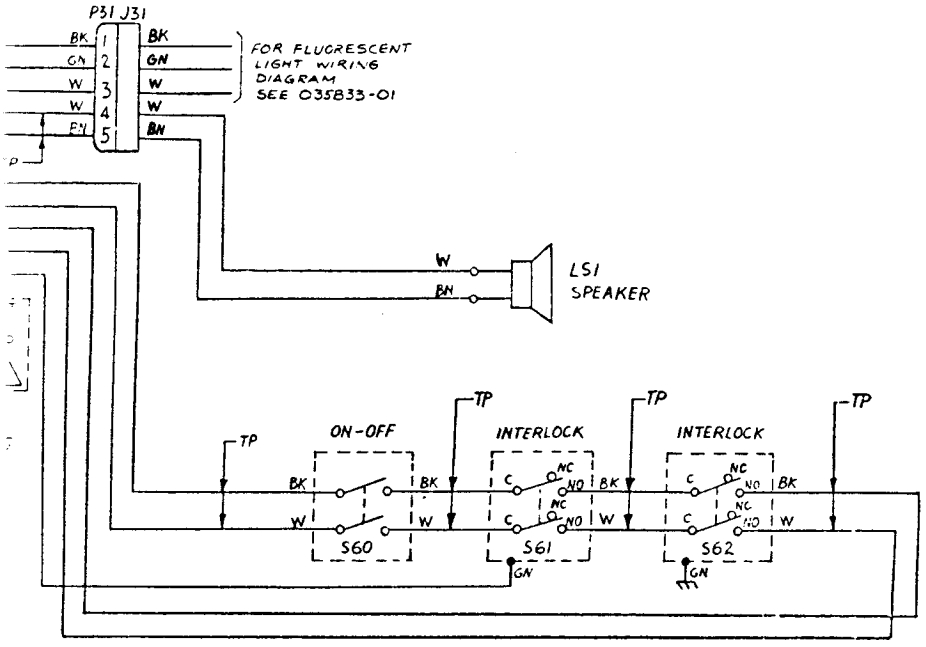
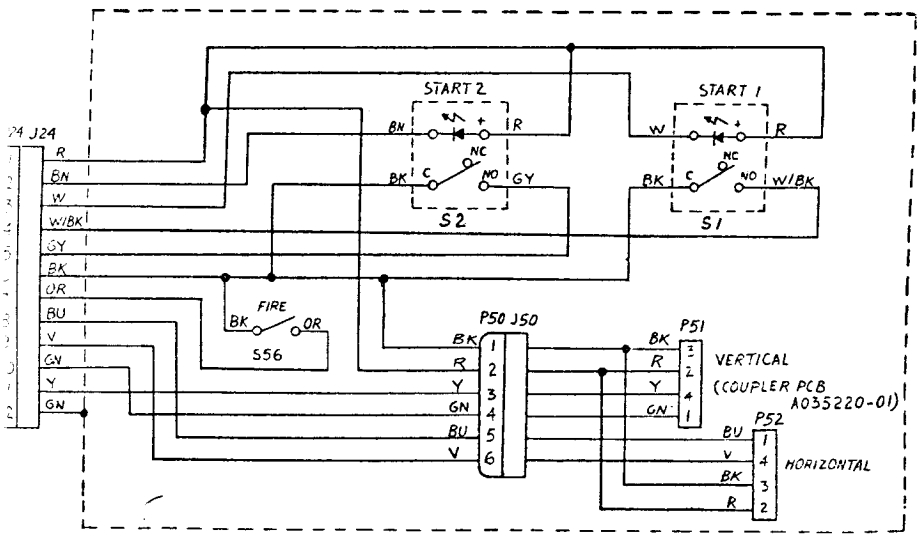
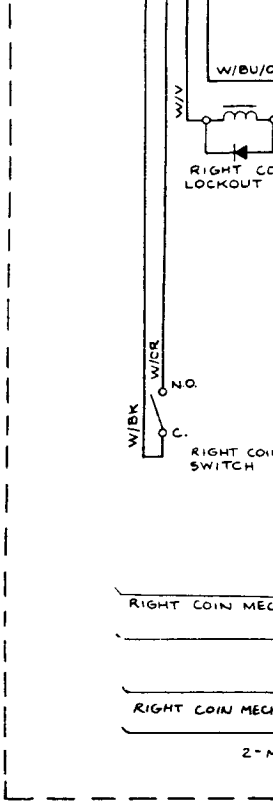
Centipede Wiring Diagram (037432-01 A)



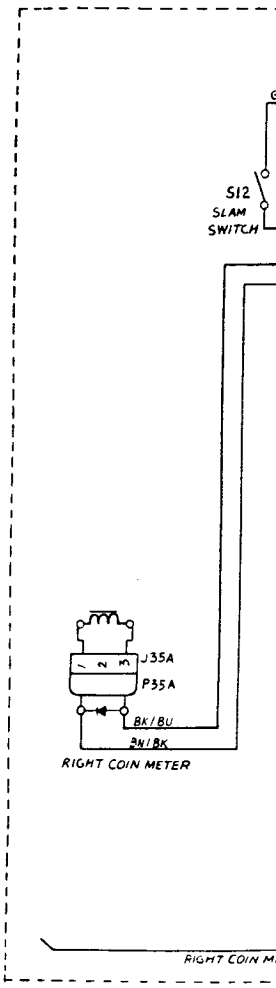


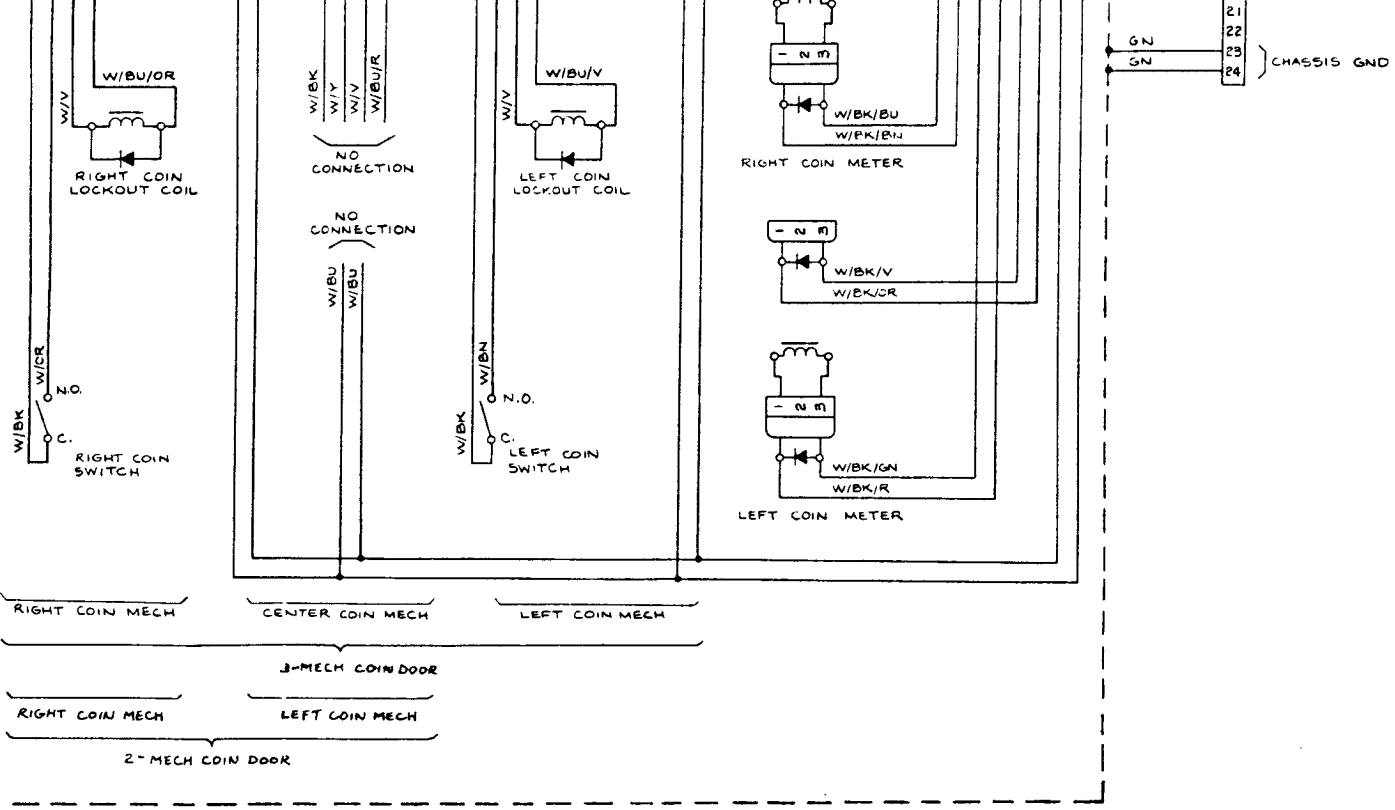
FOR COIN DOOR SCHEMATIC SEE 036835 -01



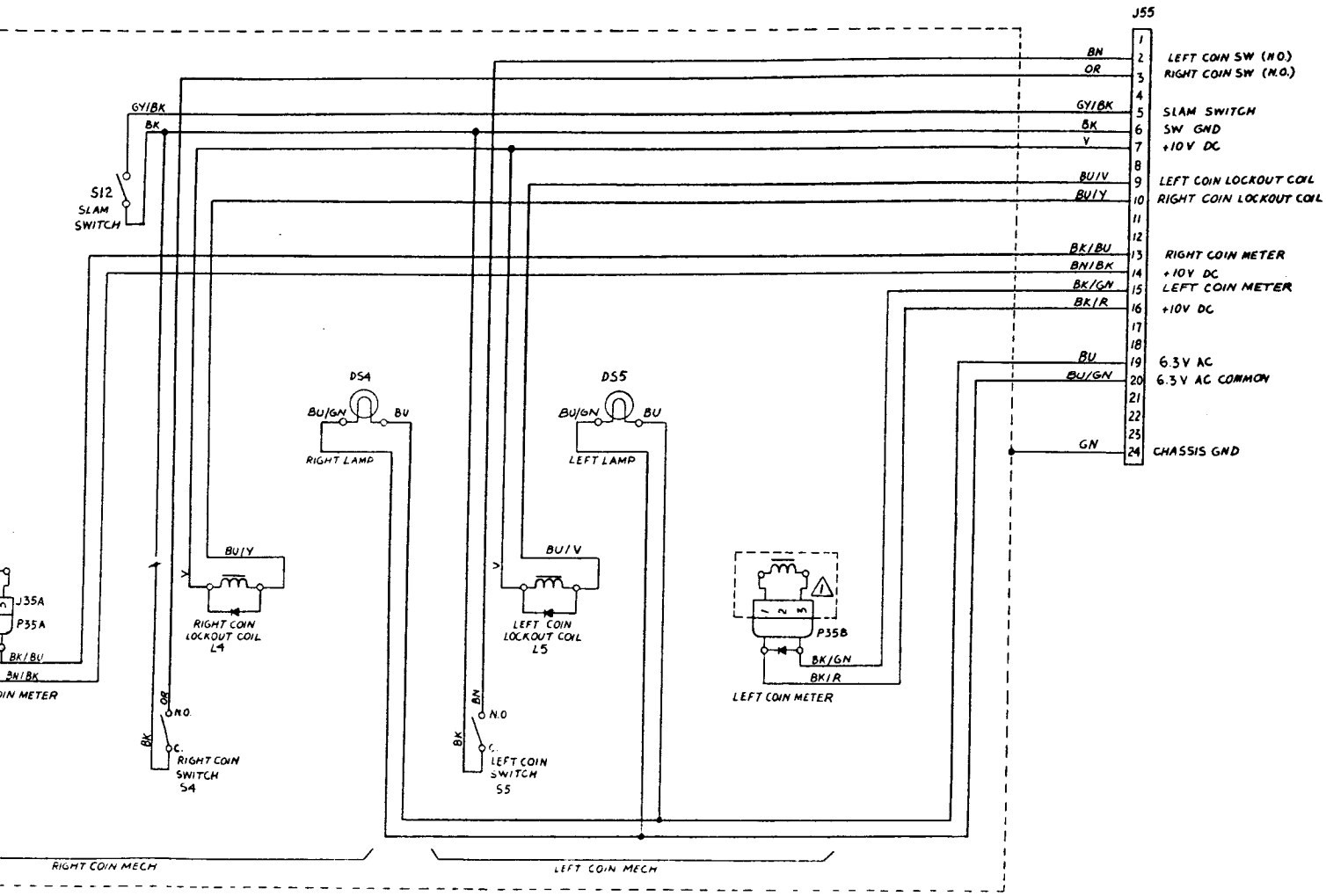


British-Made Coin D

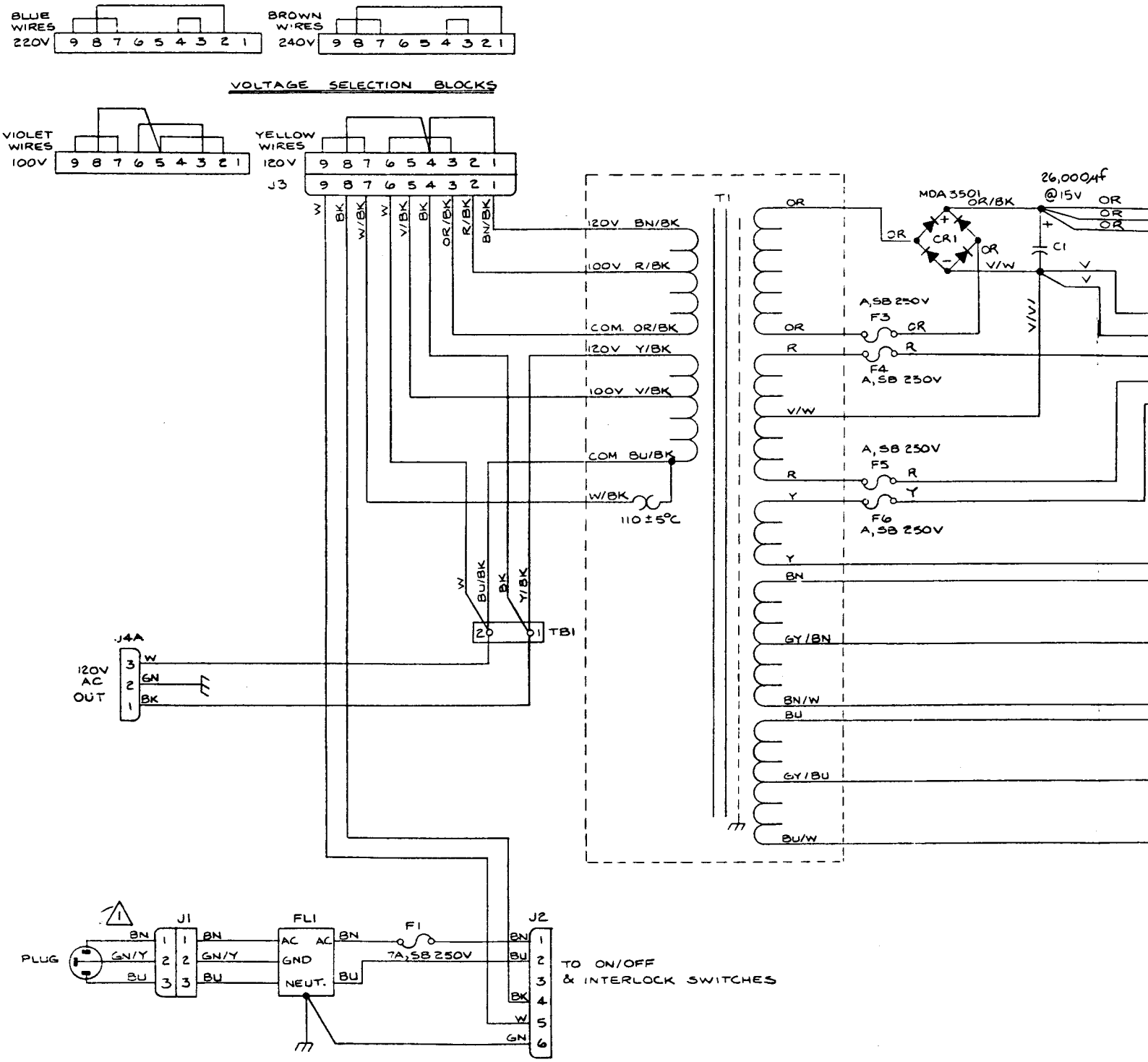


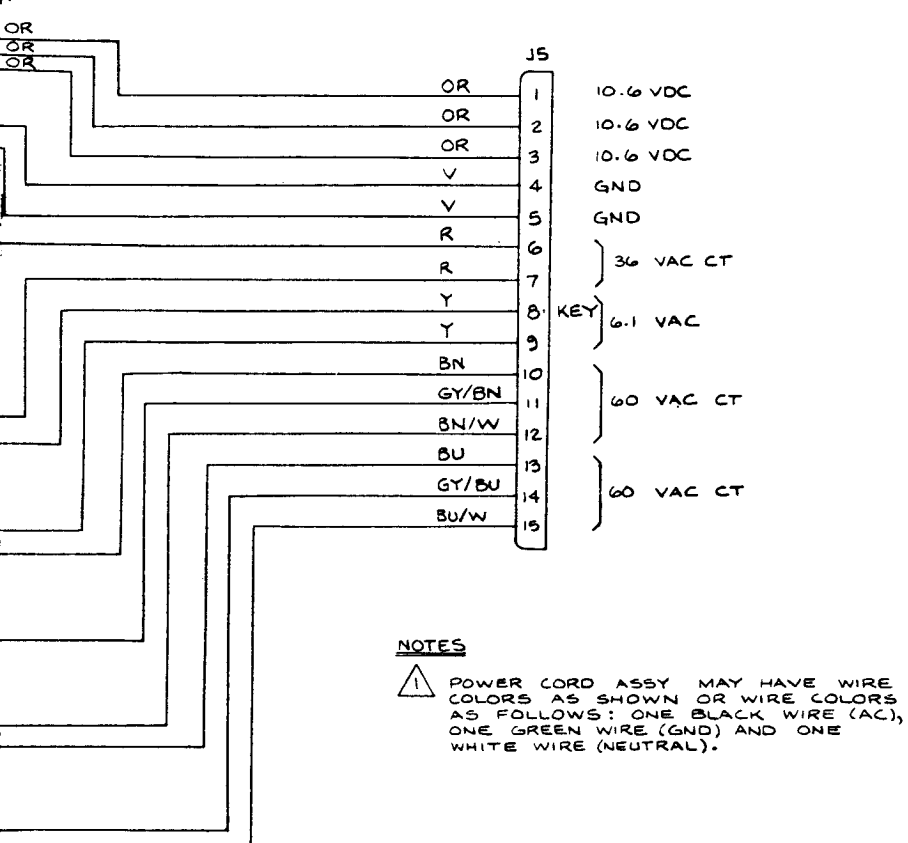


Coin Door Schematic (037050-01 A)



International Power Supply Schematic (037669-01 A)





NOTES

1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).

Regulator Audio

Regulator/Audio II PCB

The Regulator/Audio II PCB has ulating the +5 VDC logic power t plifying the audio from the game

Regulator Circuit

The regulator consists of volta pass transistor Q3 and Q3's driver tor accurately regulates the logic PCB by monitoring the voltage thr puts +SENSE and −SENSE. The the +5 VDC and ground inputs to t the regulator regulates the voltage eliminates a reduced voltage due harness between the regulator and resistor R8 is adjusted for the +5 Once adjusted, the voltage at the in remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between + of the game PCB.
2. Adjust variable resistor R8 or PCB for +5 VDC reading on t
3. Connect a voltmeter between the Regulator/Audio II PCB. V be greater than +5.5 VDC. If g connectors on both the gam tor/Audio II PCB.
4. If cleaning PCB edge connecto age difference, connect minus test point of Regulator/Audio GND test point of game PCB.

   Now connect minus lead of v point on Regulator/Audio II PC test point on game PCB. From harness circuit is dropping th the appropriate harness wire c

Audio Circuit

The audio circuit contains two i fiers. Each amplifier consists a T an effective gain of 2.2.

PCB Schematic (035435-02 D)

dual functions of reg-
e game PCB and am-

regulator Q1, power
sistor Q2. The regula-
ver input to the game
h high-impedance in-
puts are directly from
game PCB. Therefore,
the game PCB. This
IR loss in the wire
e game PCB. Variable
DC on the game PCB.
of the game PCB will

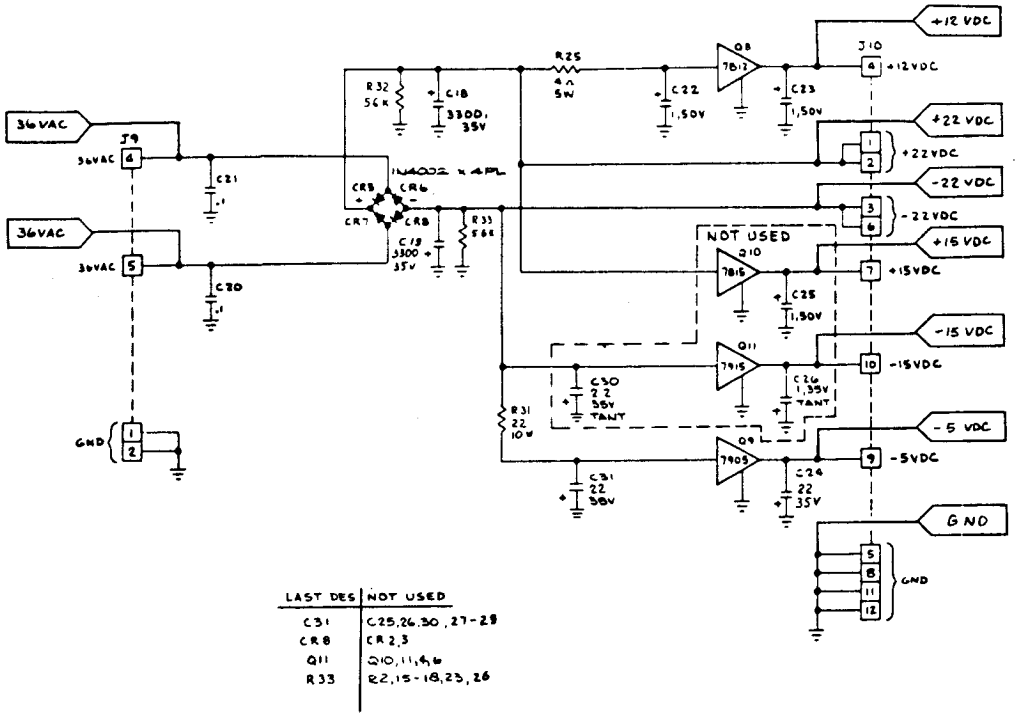
V and GND test points

ne Regulator/Audio II
voltmeter.
V REG and GND on
age reading must not
ter, try cleaning edge
PCB and the Regula-

doesn't decrease volt-
d of voltmeter to GND
PCB and plus lead to
te the voltage.
meter to +5 REG test
nd plus lead to +5 V
s you can see which
voltage. Troubleshoot
arness connector.

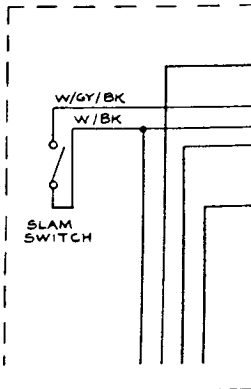
pendent audio ampli-
2002AV amplifier with

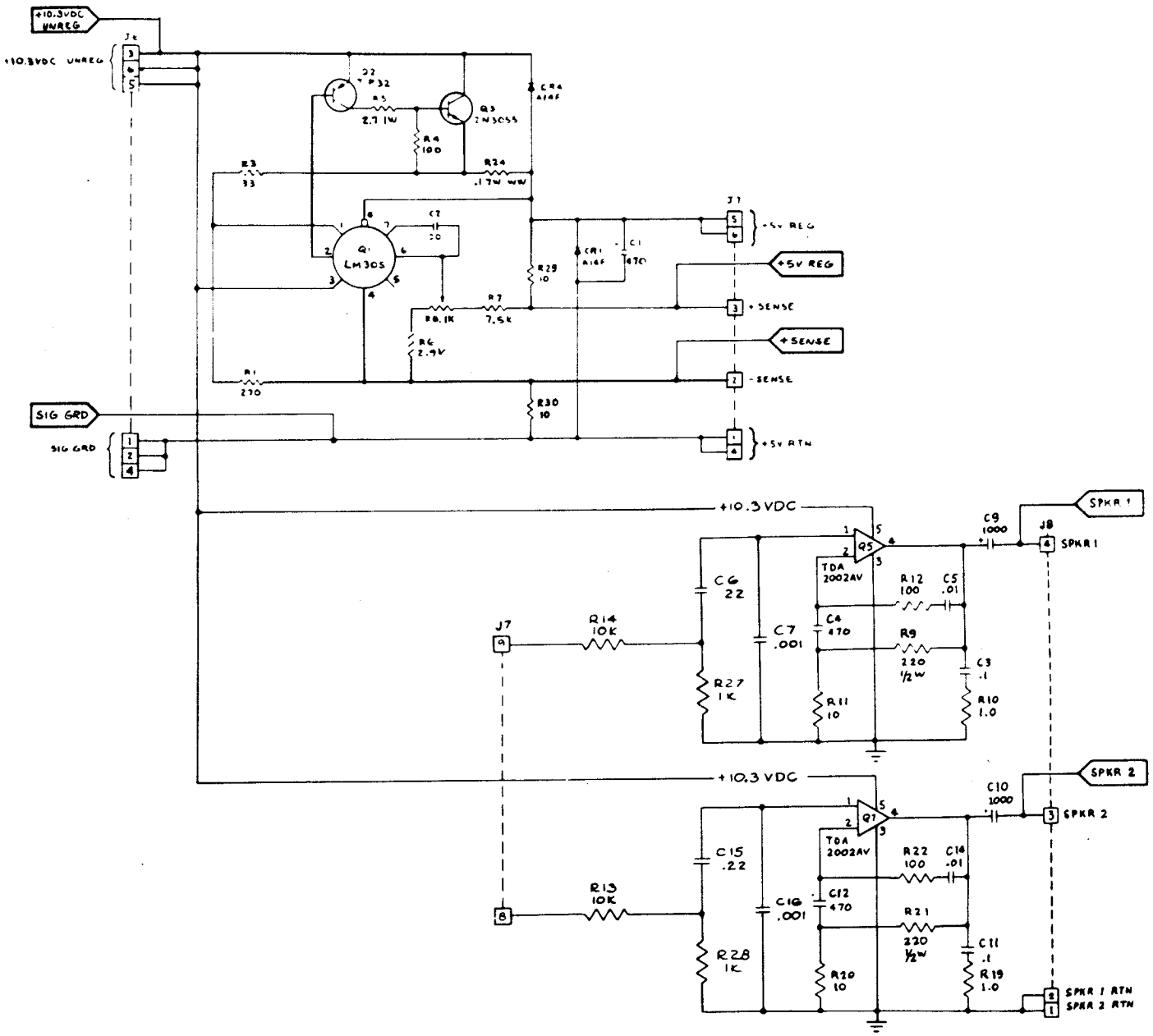
es a test point



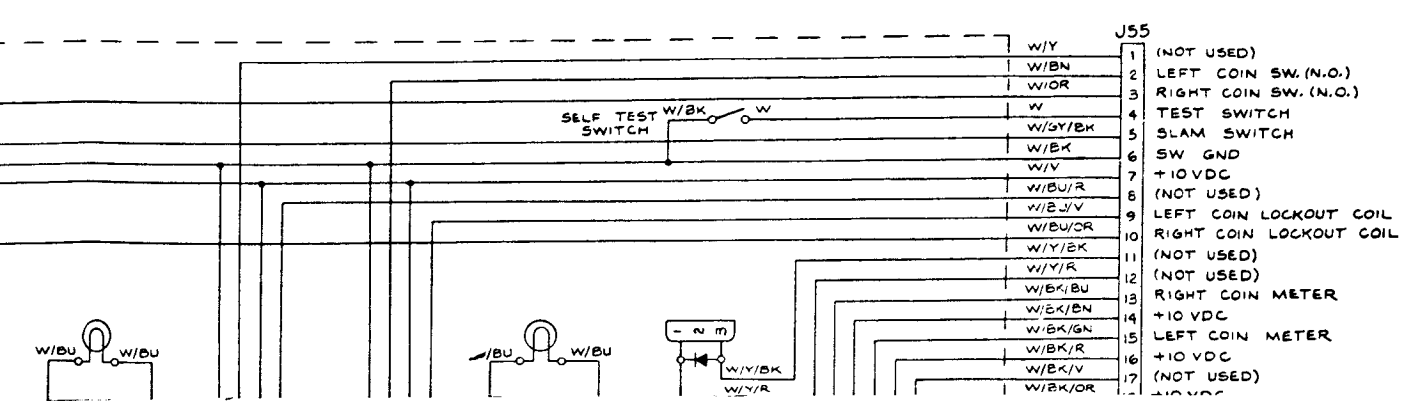
LAST DES	NOT USED
C31	C25,26,30,27-29
CR8	CR2,3
Q11	Q10,11,4,6
R33	R2,15-18,23,26

American-Made Co





Coin Door Schematic (036835-01 A)



Diagnostic Tests

Instruction	Use of Test
1. Hold the slam switch closed, while setting the self-test switch to the **on** position.	The monitor displays the color hue adjustment pattern of 16 rectangles, as follows. **Do not attempt any color hue or brightness adjustments unless you are a qualified color TV technician!** Pale Yellow-Green, Orange, White, Deep Yellow Light Green, Dark Green, Light Blue, Lime Green Deep Rose, Red, Purple, Red Navy Blue, Black, Royal Blue, Black
2. Activate any of the coin switches on the coin door.	A convergence pattern appears with a grid of white dots on a black screen. **Do not attempt any convergence adjustments unless you are a qualified color TV technician!**
3. Set self-test switch to the **off** position.	Check attract-mode display and readjust brightness if necessary.

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ATARI®

Sheet 1, Side B

Centipede™

Synchronizer
Signature Analysis Procedure
CAT Box™ Preliminary Set-Up
Power Input
Microprocessor
Address Decoder
RAM
ROM
Memory Map

Section of 037241-01 B

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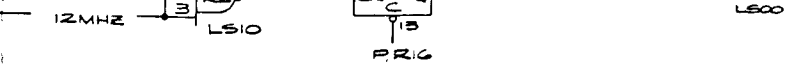
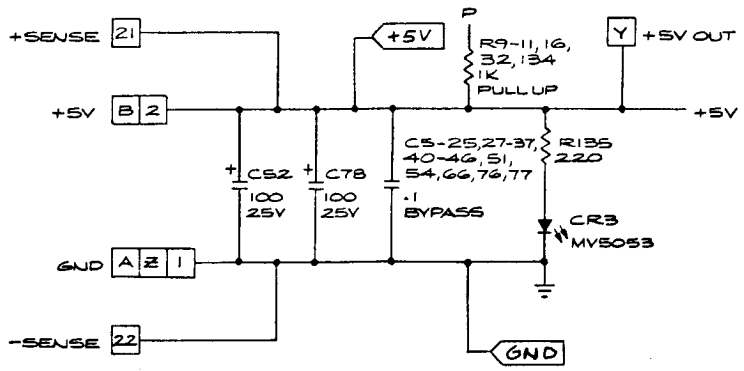
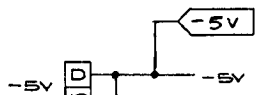
Sheet 1, Side B
DP-182-01 1st printing
Centipede

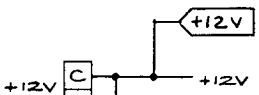


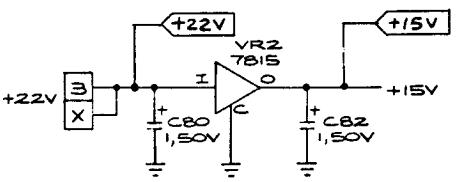
Denotes a test point

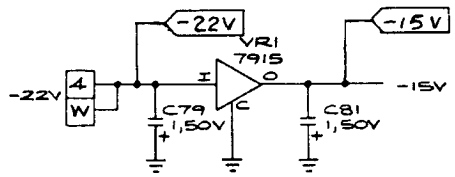
Power Input







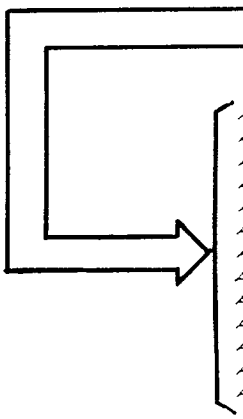




Denotes a test point

Testing the

1. Perform the CA
2. Set the CAT Bo
   a. Press TEST
   b. DBUS SOUR
   c. BYTES to 10
   d. R/W MODE
   e. R/W to WRI
   f. Key in 0000
   g. Toggle R/W
   h. R/W to REA
   i. Toggle R/W
3. If the CAT Box r
   PARE ERROR
   shows the faili
   PLAY switch is
4. If the COMPAR
   peat the test w
   ensures that th
   COMPARE ERR
   is good.



-02 VERSION
64K

Denotes a test point

AM

ox™ preliminary set-up.

witches as follows:

RESET
TO ADDR

OFF)

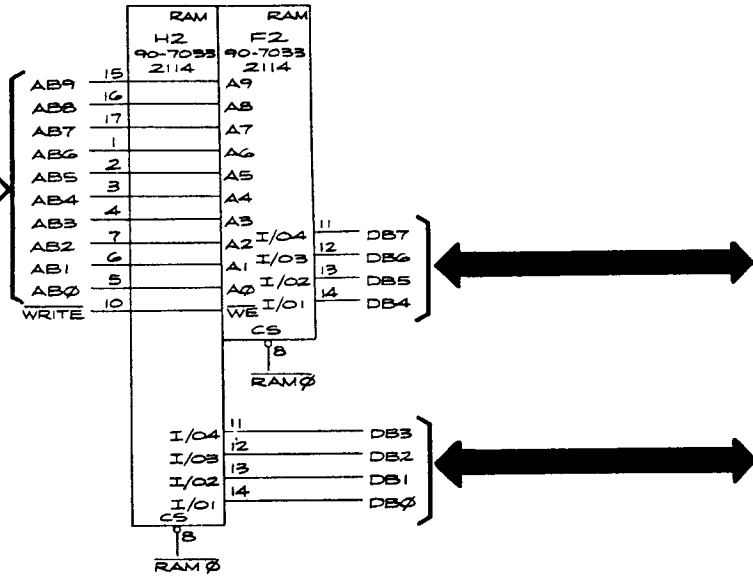
DE to SINGLE

DE to SINGLE

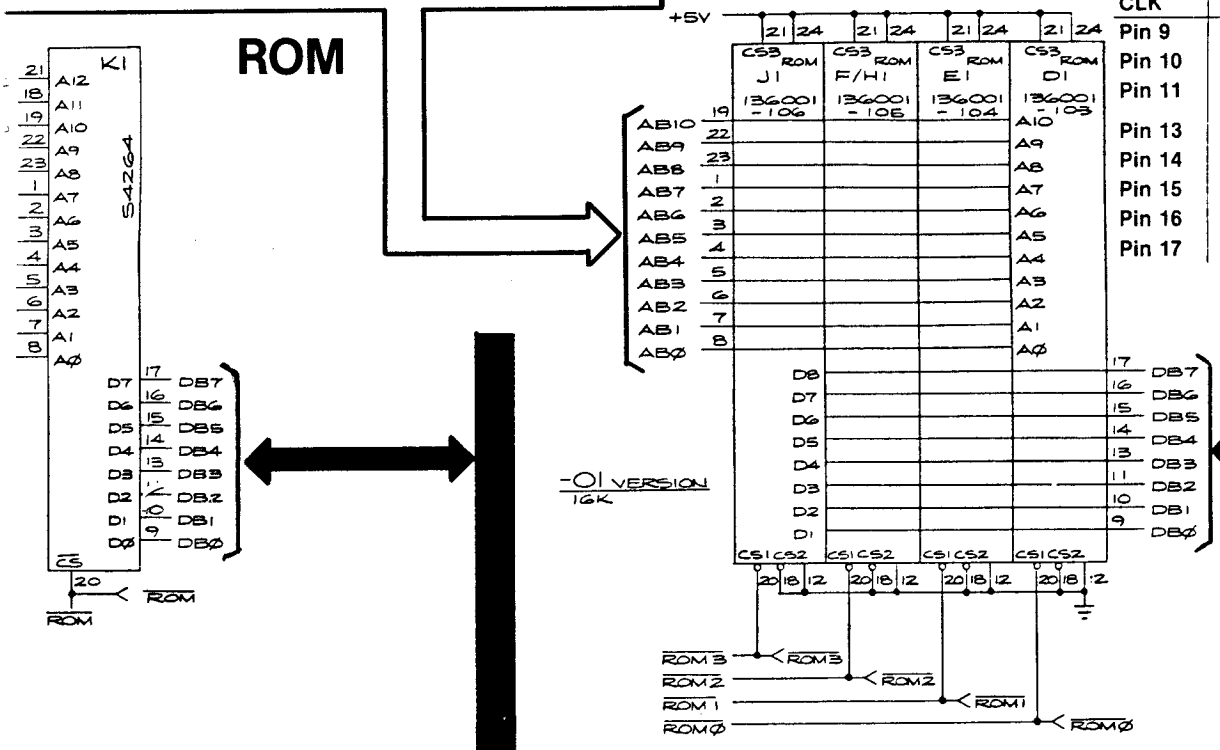
s an address that doesn't compare, the COM-
) lights, the ADDRESS/SIGNATURE display
address location, and the ERROR DATA DIS-
bled.

RROR LED does not light, rekey 0000 and re-
he DBUS SOURCE switch set to ADDR. This
ata bits at address 0000 will go high. If the
LED does not light after this step, the RAM

RAM



ROM



	D1	E1	F/H1	J1
START	Pin 20	Pin 20	Pin 20	Pin 20
STOP	Pin 20	Pin 20	Pin 20	Pin 20
CLK	Φ2	Φ2	Φ2	Φ2
Pin 9	OH81	13PH	CU62	476H
Pin 10	O8FC	C4P5	9553	2A2C
Pin 11	U9F7	11F3	7756	2337
Pin 13	P316	098P	A7CF	FP07
Pin 14	P8C4	5H24	6081	A9AF
Pin 15	H973	0548	5HAC	12HA
Pin 16	8F8F	33P7	6U43	2367
Pin 17	U638	80AA	F83H	8P82

from J2, ground J2 pin 1.

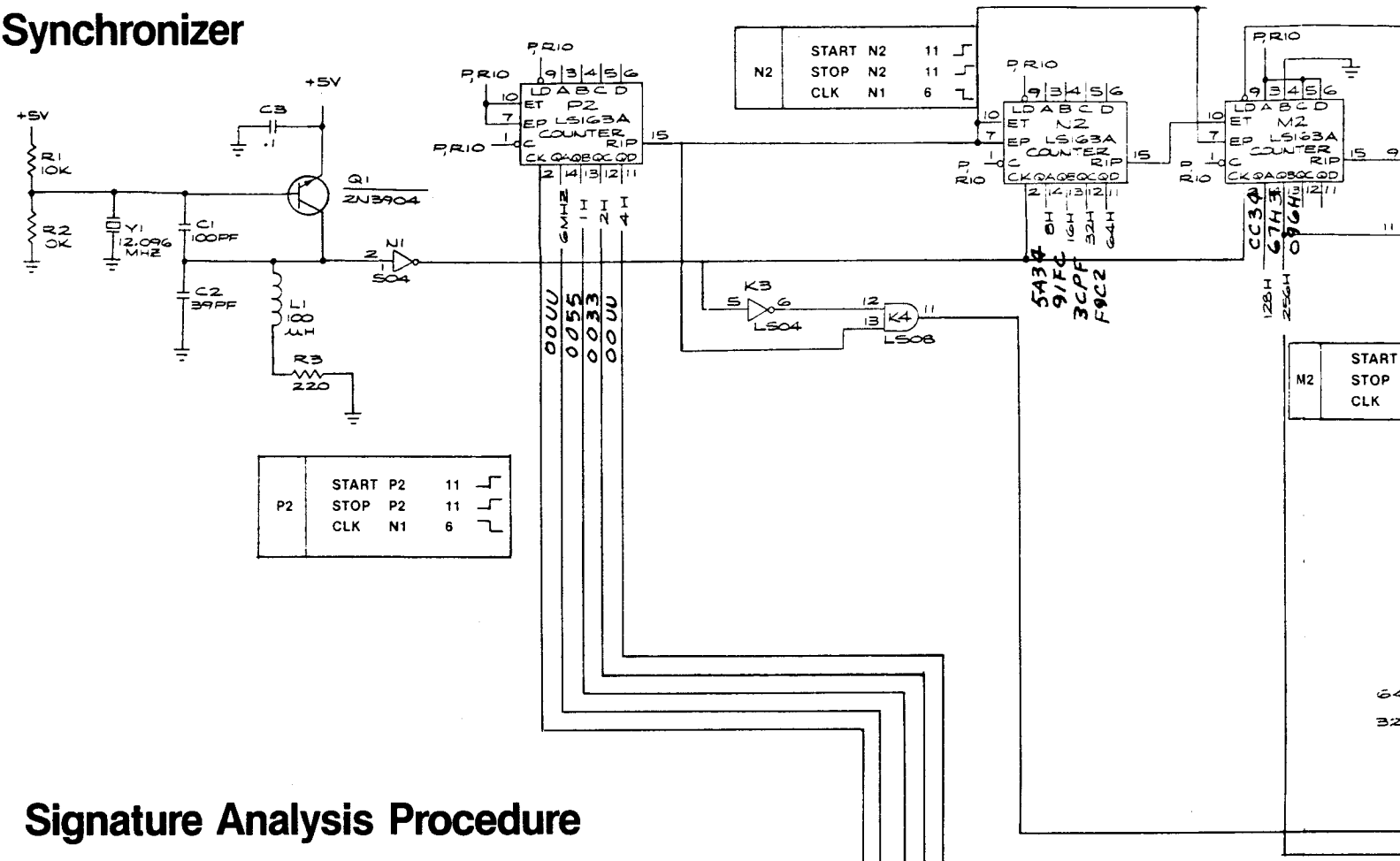
Memory Map

MEMORY MAP

HEXA-DECIMAL ADDRESS	R/W	DATA D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0000-03FF		D	D	D	D	D	D	D	D	RAM
0400-07BF		D	D	D	D	D	D	D	D	Playfield RAM
07C0-07CF		D	D	D	D	D	D	D	D	Motion Object Picture
07D0-07DF		D	D	D	D	D	D	D	D	Motion Object Vert.
07E0-07EF		D	D	D	D	D	D	D	D	Motion Object Horiz.
07F0-07FF				D	D	D	D	D	D	Motion Object Color
0800	R	D	D	D	D	D	D	D	D	Option Switch 1 (0 = On)
0801	R	D	D	D	D	D	D	D	D	Option Switch 2 (0 = On)
0C00	R	D				D	D	D	D	Horizontal Trak Ball™ Inputs
	R		D							VBLANK (1 = VBlank)
	R			D						Self-Test (0 = On)
	R				D					Cocktail Cabinet (1 = Cocktail)
0C01	R	D	D	D						R,C,L Coin Switches (0 = On)
	R				D					SLAM (0 = On)
	R					D				Player 2 Fire Switch (0 = On)
	R						D			Player 1 Fire Switch (0 = On)
	R							D		Player 2 Start Switch (0 = On)
	R								D	Player 1 Start Switch (0 = On)
0C02	R	D				D	D	D	D	Vertical Trak Ball™ Inputs
0C03	R	D	D	D	D					Player 1 Joystick (R, L, Down, Up)
	R					D	D	D	D	Player 2 Joystick (0 = On)
1000-100F	R/W	D	D	D	D	D	D	D	D	Custom Audio Chip
1404	W					D	D	D	D	Playfield Color RAM
140C	W					D	D	D	D	Motion Object Color RAM
1600	W	D	D	D	D	D	D	D	D	EA ROM Address & Data Latch
1680	W					D	D	D	D	EA ROM Control Latch
1700	R	D	D	D	D	D	D	D	D	EA ROM Read Data
1800	W									IRQ Acknowledge
1C00	W	D								Left Coin Counter (1 = On)
1C01	W	D								Center Coin Counter (1 = On)
1C02	W	D								Right Coin Counter (1 = On)
1C03	W	D								Player 1 Start LED (0 = On)
1C04	W	D								Player 2 Start LED (0 = On)
1C07	W	D								Trak Ball™ Flip Control (0 = Player 1)
2000	W									WATCHDOG
2400	W									Clear Trak Ball™ Counters
2000-3FFF	R									Program ROM

J1
Pin 20
Pin 20
Φ2
476H
2A2C
2337
FP07
A9AF
12HA
2367
8P82

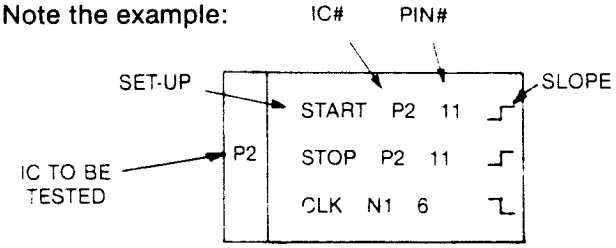
Synchronizer



Signature Analysis Procedure

1. Perform the CAT Box™ preliminary set-up.
2. Connect the three BNC to E-Z clip cables (supplied with the CAT Box) to the SIGNATURE ANALYSIS CONTROL START, STOP, AND CLOCK jacks on the CAT Box.
3. Attach the three black E-Z clips to a ground loop on the CENTIPEDE™ game PCB.
4. Attach the CAT Box data probe to the DATA jack on the CAT Box.
5. The red E-Z clips on the cables will be moved about for each group of signatures to be taken. The set-up for each group of signatures is located on the schematic sheet near the device to be checked. The signatures are located on or near the signal point on the schematic.

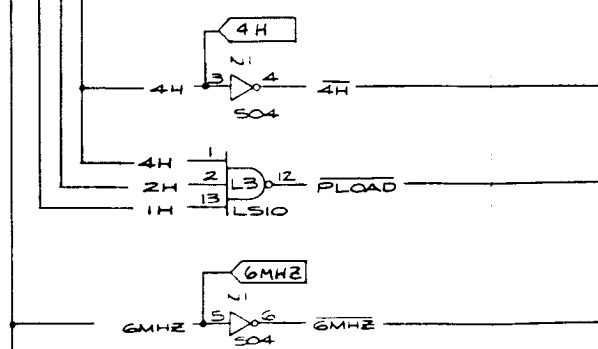
Note the example:

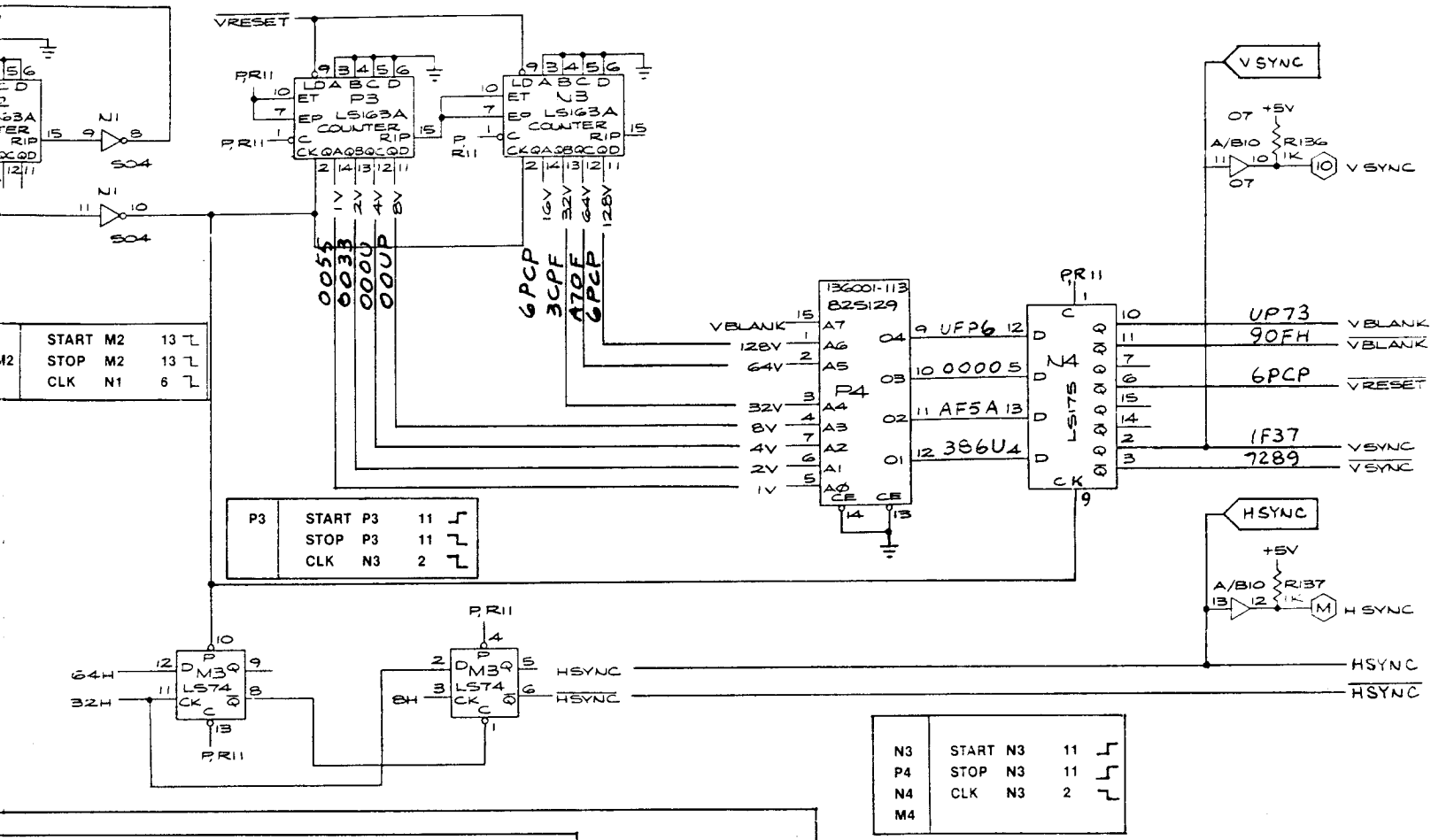


6. Set the CAT Box switches as follows:
   a. TESTER MODE: SIG
   b. TESTER SELF TEST: OFF
   c. PULSE MODE: LATCHED
   d. START:
   e. STOP:
   f. CLOCK:

CAT Box™ Prelimina

1. Remove:
   - The electrical power from
   - The wiring harness from
   - The game PCB from the
   - The MPU chip C2 from th
2. Connect:
   - The extender cables to the
   - Pins 37 to 39 on the MPU
   - The CAT Box flex cable to



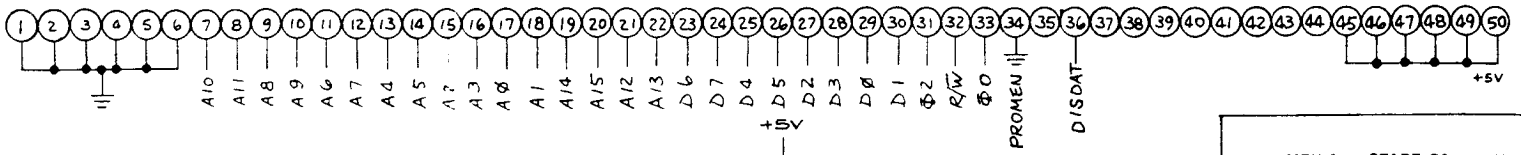


liminary Set-up

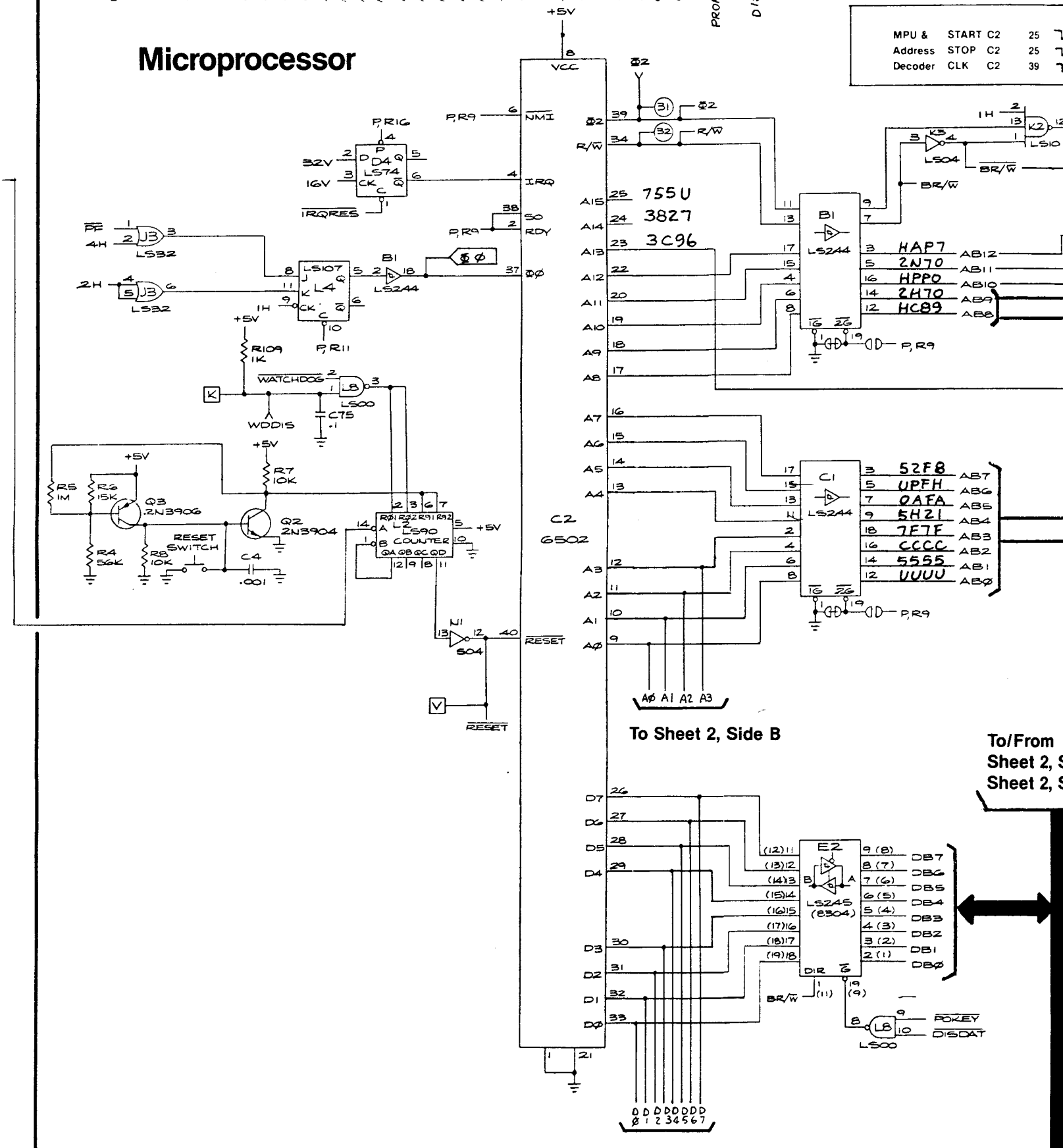
ower from the game.
ess from the game PCB.
from the cabinet.
C2 from the game PCB.

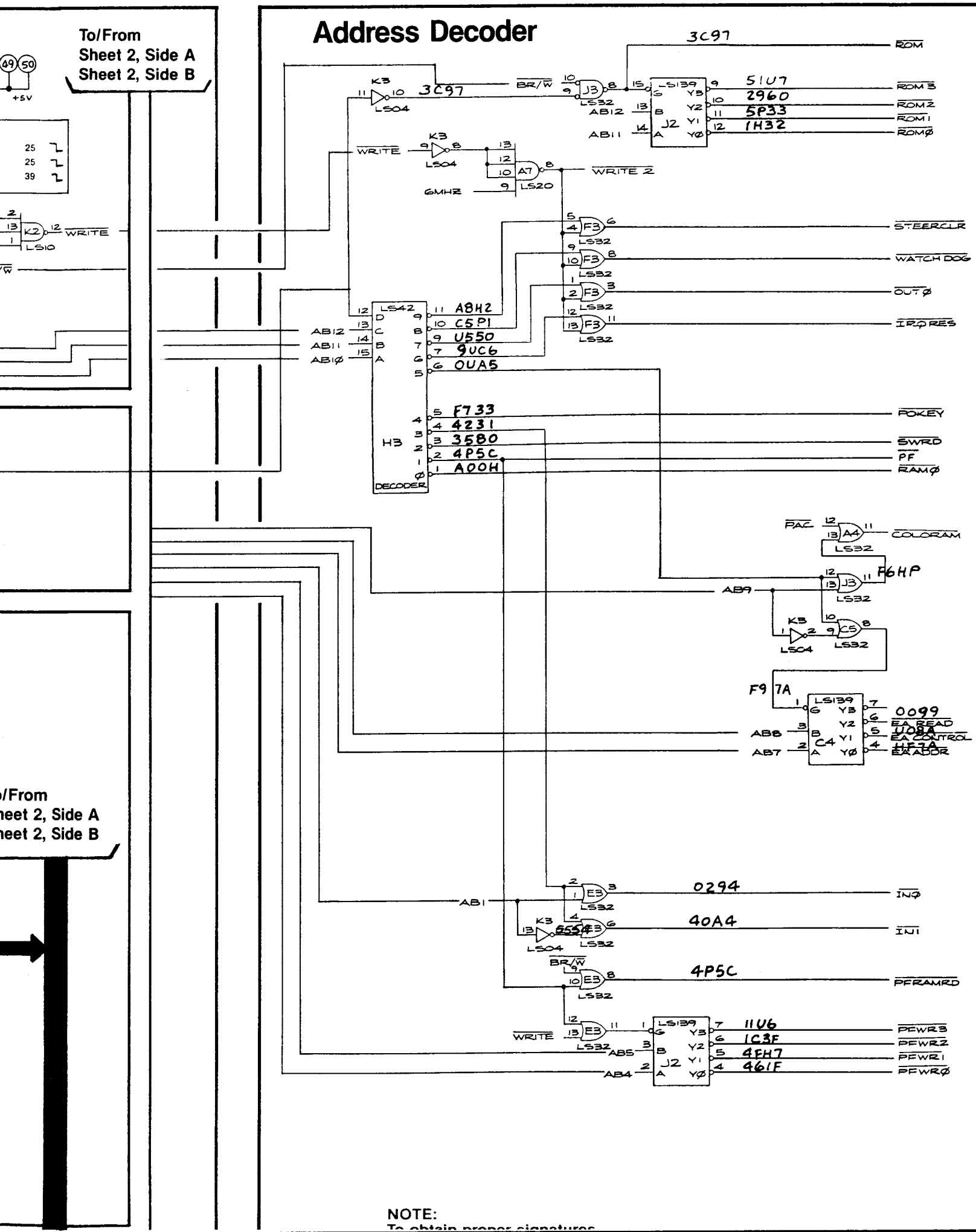
bles to the game PCB and the wiring harness.
the MPU socket with a piece of 28 AWG wire.
k cable to the game PCB test edge connector.

TEST CONNECTOR-FOR ATARI CAT BOX™



Microprocessor




Address Decoder
To/From
Sheet 2, Side A
Sheet 2, Side B
+5V
3C97
ROM
ROM3
ROM2
ROM1
ROMØ
51U7
2960
5P33
1H32
BR/W
WRITE
WRITE 2
6MHZ
STEERCLR
WATCH DOG
OUTØ
IRQ RES
A8H2
C5P1
U550
9UC6
0UA5
F733
4231
3580
4P5C
A00H
DECODER
POKEY
SWRD
PF
RAMØ
PAC
COLORAM
F6HP
AB9
F9 7A
0099
EA READ
EA CONTROL
EA ADDR
0294
INØ
40A4
IN1
4P5C
PFRAMRD
11U6
1C3F
4FH7
461F
PFWR3
PFWR2
PFWR1
PFWRØ
NOTE:

ATARI®

Sheet 2, Side A

Centipede™

Playfield Address Selector
Playfield Memory
Playfield Multiplexer
Picture Data ROM Circuitry
Motion Object Circuitry (Vertical)
Motion Object Circuitry (Horizontal)

Section of 037241-01 C+

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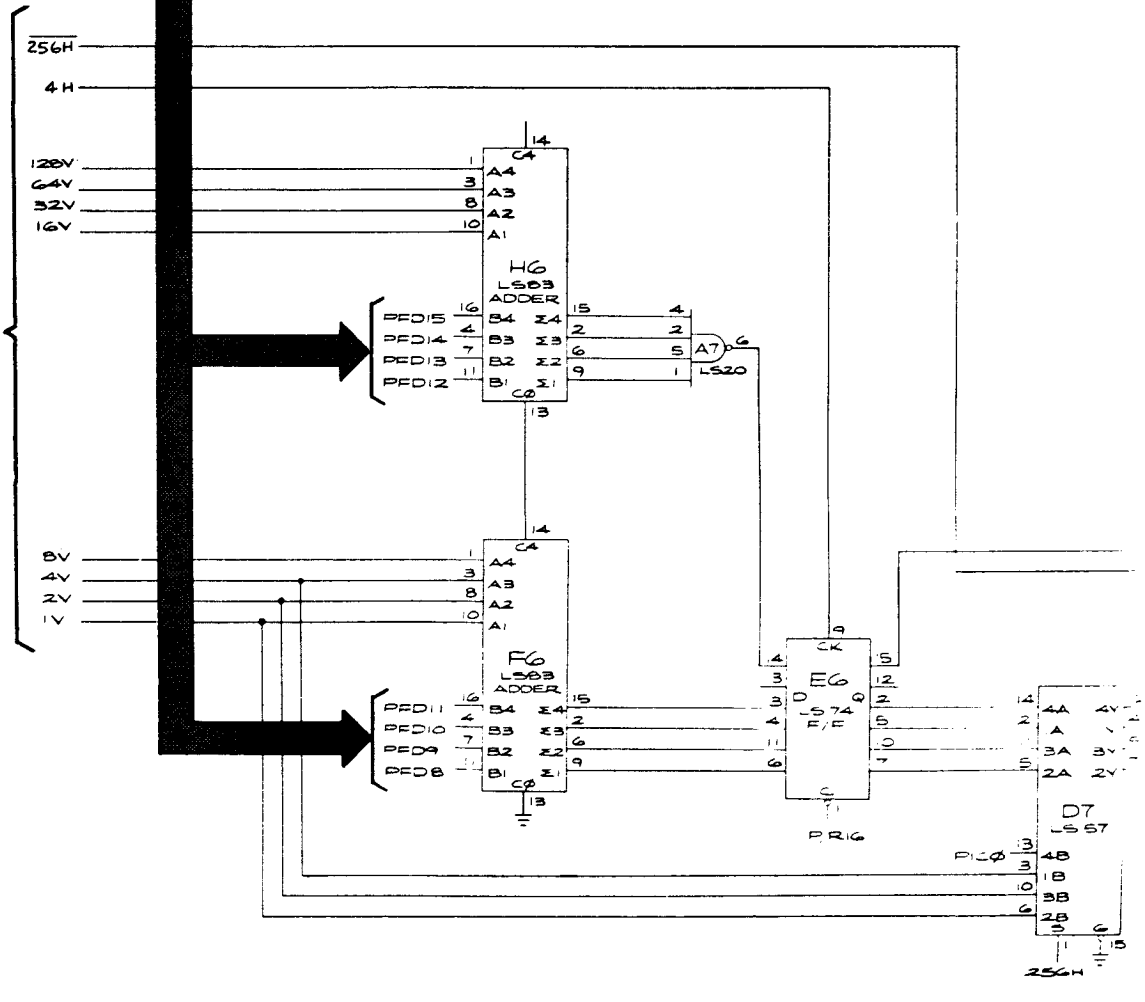
Motion Object Circuitry (Verti

The Motion Object Circuitry (vertical) receives playfield data and sync generator circuitry to generate the vertical component of the mo 15 from the playfield memory and 1V-128V from the sync generator are The output is gated by A7 when a motion object is on one of the six latched by E6 to AND gate B7. A low on B7 pin 8 indicates the preser one of the vertical lines during non-active video time. This signal (MA plexers in the picture data circuitry.

When 256H on pin 1 of D7 goes high, 1V, 2V, 4V and PIC0 are selecte the latched output of E6 is selected. The output of D7 is EXCLUSIV sent to the picture data selector circuitry as motion graphic address input to EXCLUSIVE OR gate E7 is PIC7 from the playfield code m when high causes the output of E7 to be complimented. For example PIC7 causes MGA0-MGA3 to go high. This causes the motion object to bottom.

From Sync Generator Sheet 1, Side B



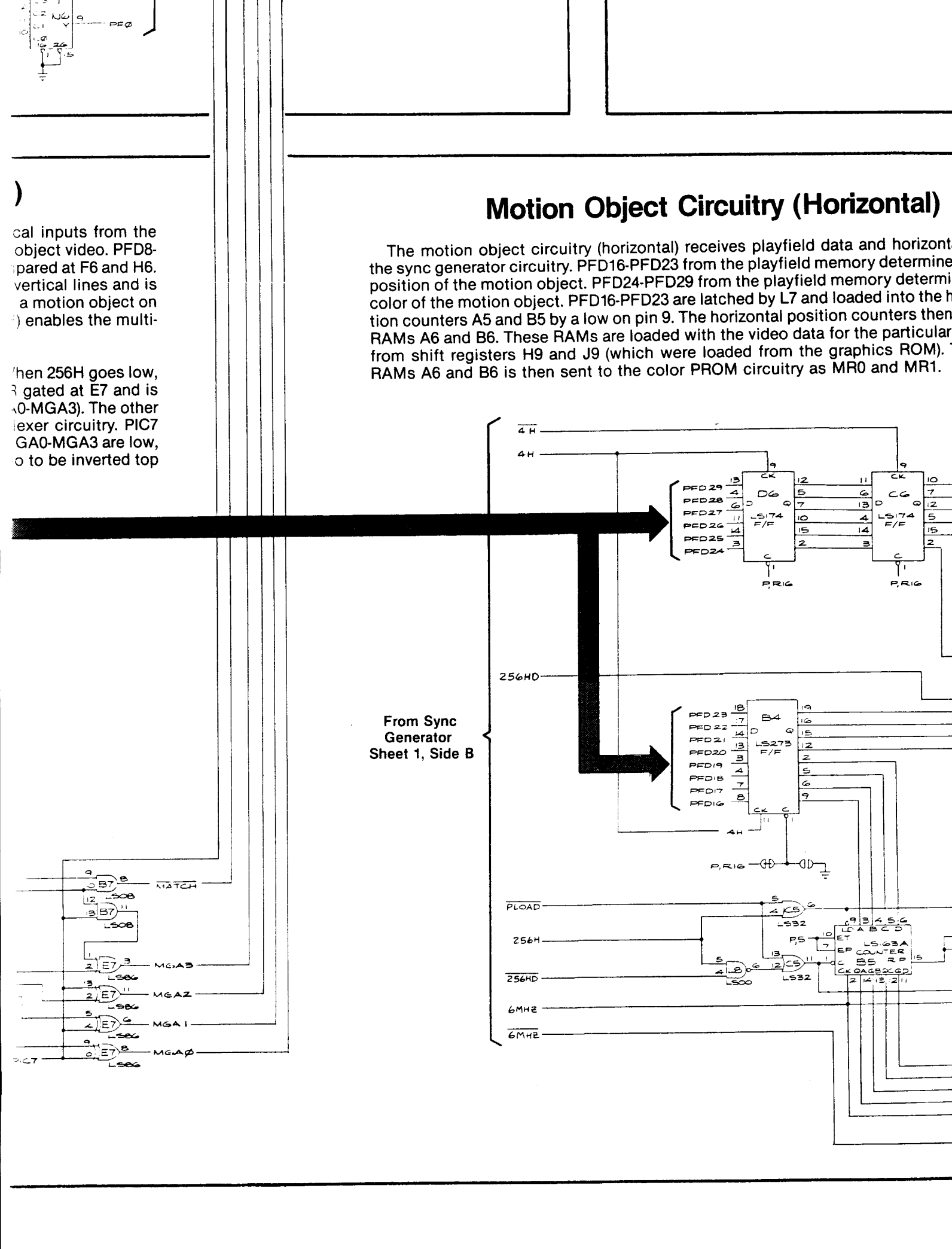
)

cal inputs from the object video. PFD8- pared at F6 and H6. vertical lines and is a motion object on) enables the multi-

hen 256H goes low, gated at E7 and is 0-MGA3). The other lexer circuitry. PIC7 GA0-MGA3 are low, o to be inverted top

Motion Object Circuitry (Horizontal)

The motion object circuitry (horizontal) receives playfield data and horizont the sync generator circuitry. PFD16-PFD23 from the playfield memory determine position of the motion object. PFD24-PFD29 from the playfield memory determi color of the motion object. PFD16-PFD23 are latched by L7 and loaded into the h tion counters A5 and B5 by a low on pin 9. The horizontal position counters then RAMs A6 and B6. These RAMs are loaded with the video data for the particular from shift registers H9 and J9 (which were loaded from the graphics ROM). RAMs A6 and B6 is then sent to the color PROM circuitry as MR0 and MR1.

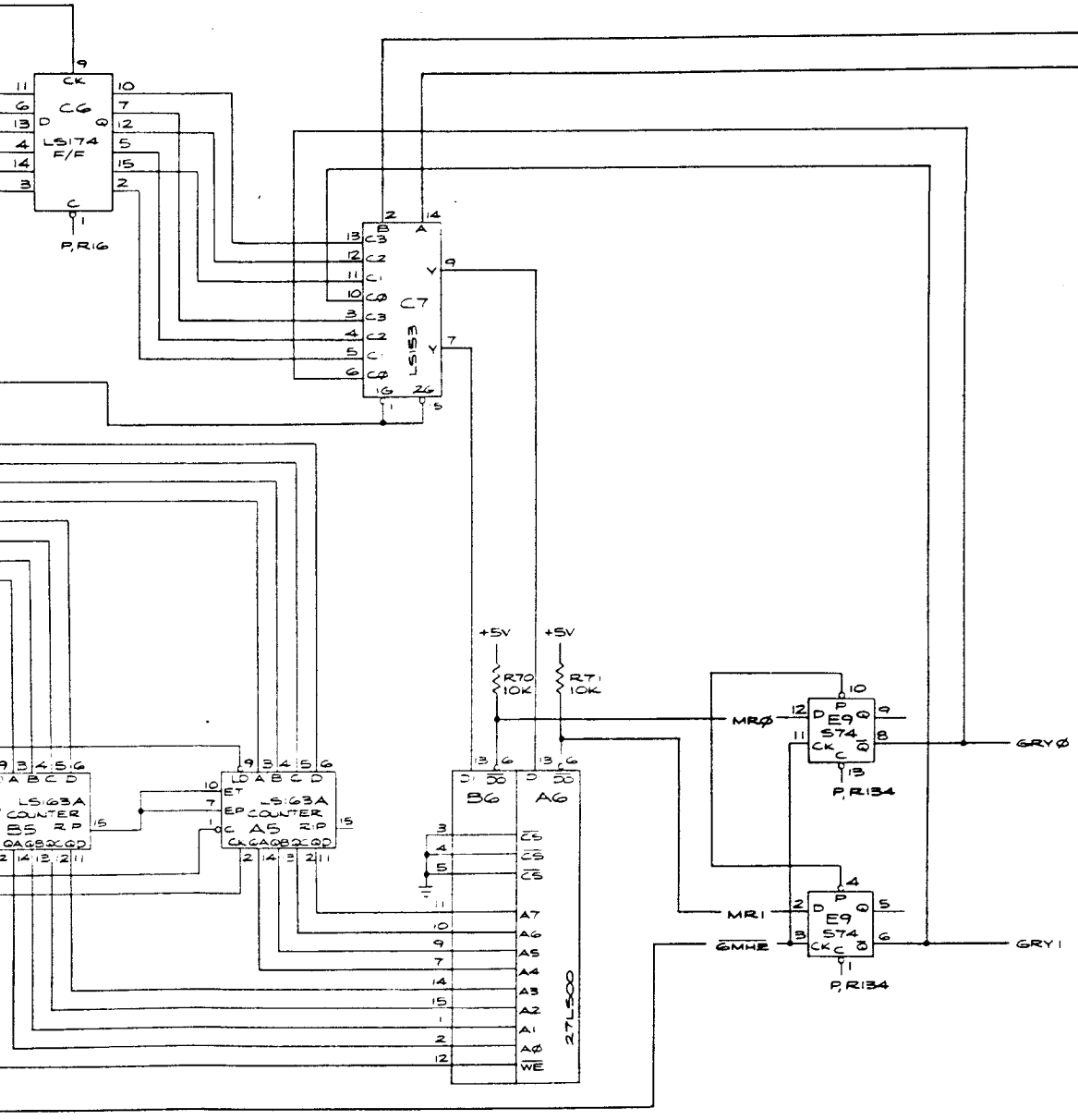


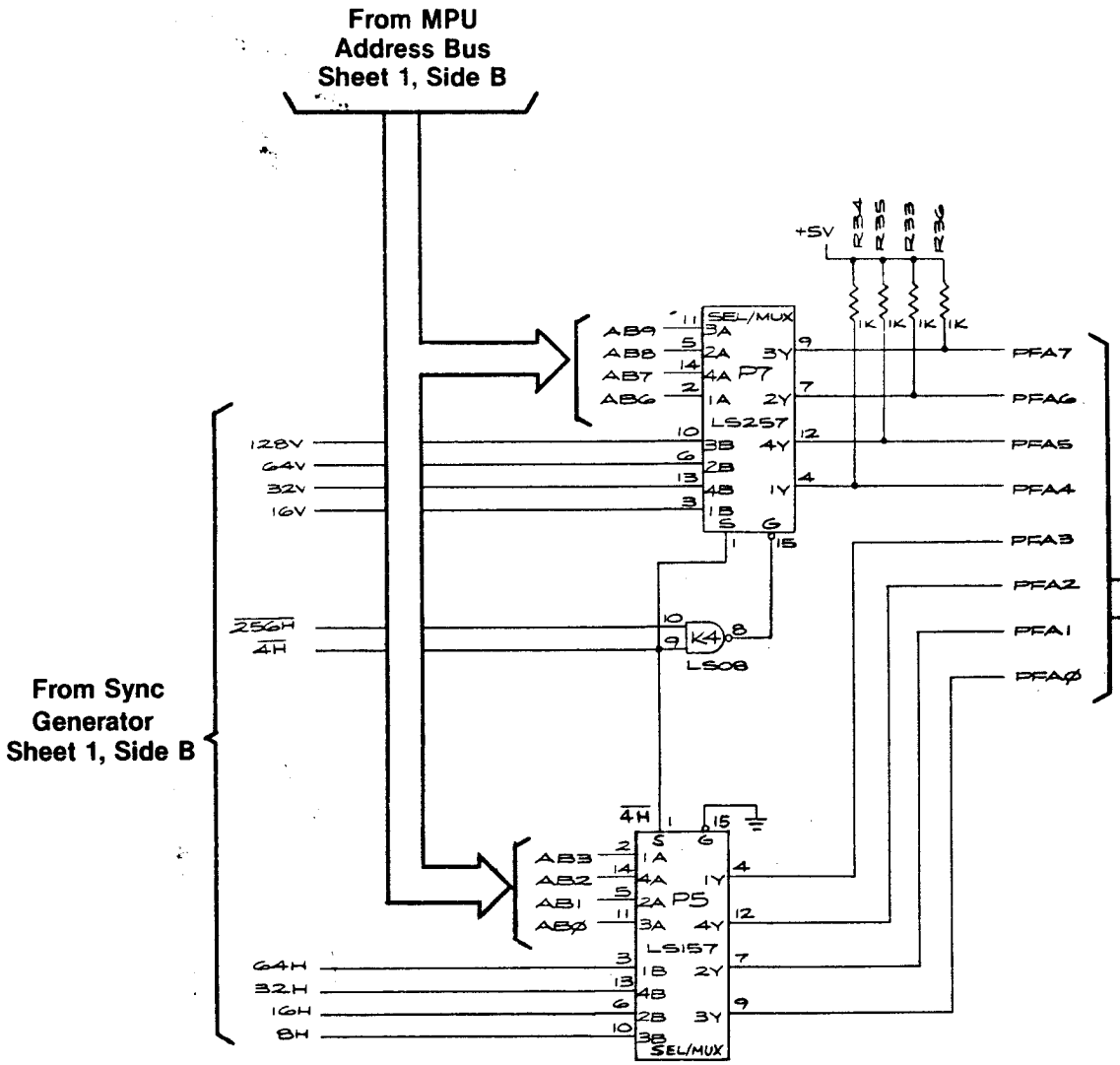
playfield code multiplexer, MGA0-MGA3 (motion graphics address) from the motion object circuitry, 256H and $\overline{256H}$ from the sync generator. PIC0-PIC5 represent the code for the object to be displayed. MGA0-MGA3 set one of eight different combinations of the 8-line by 8-bit blocks of picture video or the 16 line by 8 bit blocks of motion object video.

256H when high selects the playfield picture color codes to be addressed. 256H when low selects the motion object color codes to be addressed. The picture data ROM output D1-D8 on F7 and H/J7 are multiplexed by F8, H8, J8 and K8 and shifted out serially at H9 and J9. This serial output is latched by F9 as AREA0 and AREA1 to the motion object horizontal circuitry and the video output circuit.

izontal)

a and horizontal inputs from
nory determine the horizontal
emory determine the indirect
aded into the horizontal posi-
counters then address video
the particular motion object
aphics ROM). The output for
R0 and MR1.





Playfield Address Selector

The Playfield Address Selector controls the access to the playfield memory. It allows either the game MPU or the sync generator to scan the playfield memory. The Playfield Address Selector consists of multiplexers P5, and P7 and gate K4.

When $\overline{4H}$ on pin 1 of P5 and P7 is low and pin 15 on P7 is low, the Playfield Address Selector receives 8H, 16H, 32H, and 64H on P5 and 16V, 32V, 64V, and 128V on P7 from the sync generator. These signals enable the sync generator circuits to access the playfield memory.

When $\overline{4H}$ goes high the game MPU addresses the playfield memory (via AB0-AB9) for the positioning of the graphics. During horizontal blanking (pin 15 of P7 is high) the outputs of P7 (PFA4-PFA7) are held high enabling the motion object circuitry to access the playfield memory for the motion objects to be displayed.

Centipede Pl

Testing the P

1. Perform the CAT B
2. Set the CAT Box s
   a. Press TESTER
   b. DBUS SOURCE
   c. BYTES to 1024
   d. R/$\overline{W}$ MODE to
   e. R/$\overline{W}$ to WRITE
   f. Key in 0400
   g. Set R/$\overline{W}$ MODE
   h. R/$\overline{W}$ to READ
   i. Set R/$\overline{W}$ MODE

ede Playfield RAM

the Playfield RAM

the CAT Box preliminary set-up.

CAT Box switches as follows:

TESTER RESET
SOURCE TO ADDR
S to 1024
MODE to (OFF)
o WRITE
0400
W MODE to PULSE, then to OFF.
o READ
W MODE to PULSE, then to OFF.

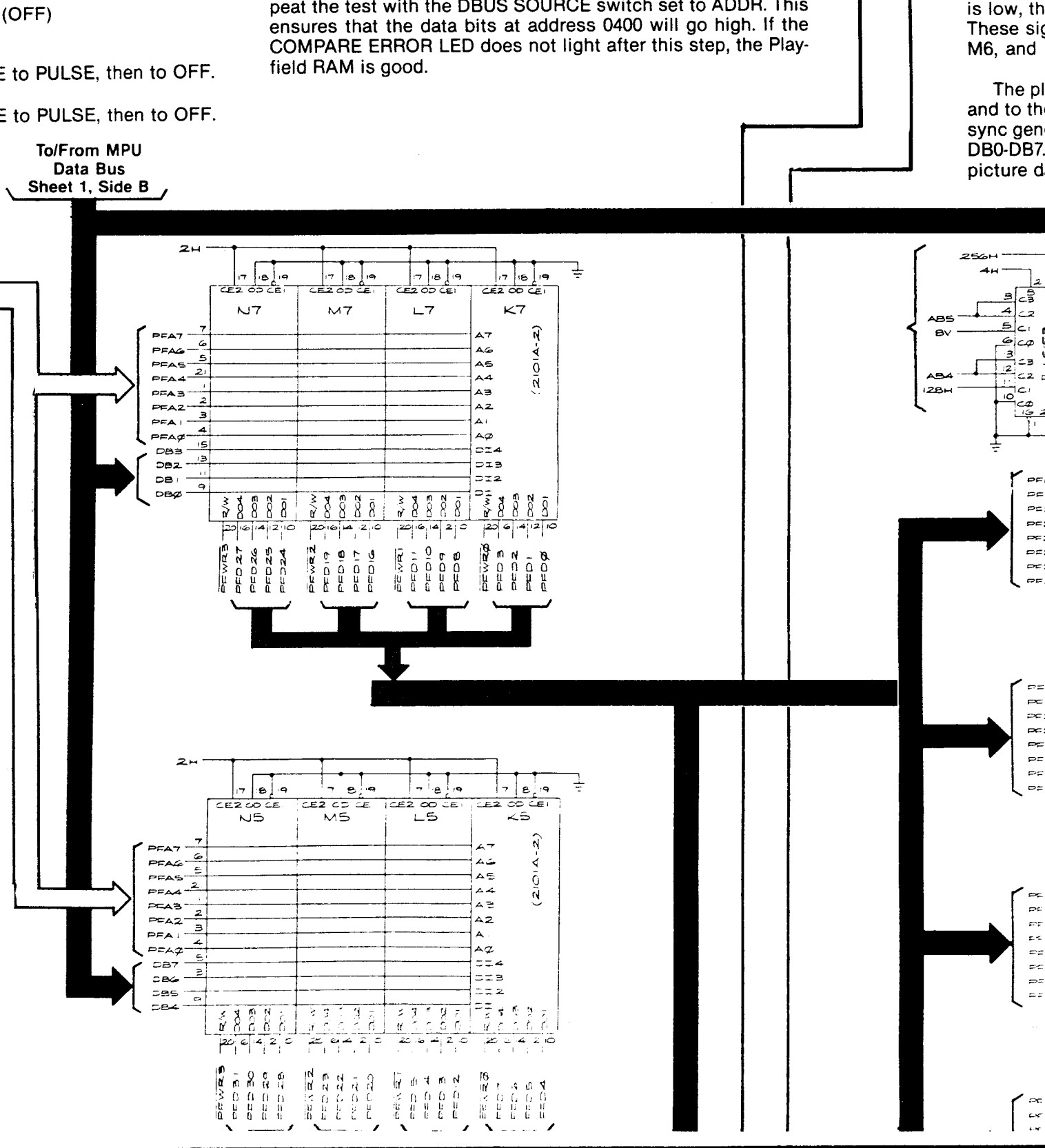
3. If the CAT Box reads an address that doesn't compare, the COMPARE ERROR LED lights, the ADDRESS/SIGNATURE display shows the failing address location, and the ERROR DATA DISPLAY switch is enabled.

4. If the COMPARE ERROR LED does not light, rekey 0400 and repeat the test with the DBUS SOURCE switch set to $\overline{\text{ADDR}}$. This ensures that the data bits at address 0400 will go high. If the COMPARE ERROR LED does not light after this step, the Playfield RAM is good.

The Pl
(PFD0-PF
played or
consists

When 2
selected
as select
playfield
is low, th
These sig
M6, and

The pl
and to th
sync gen
DB0-DB7.
picture d

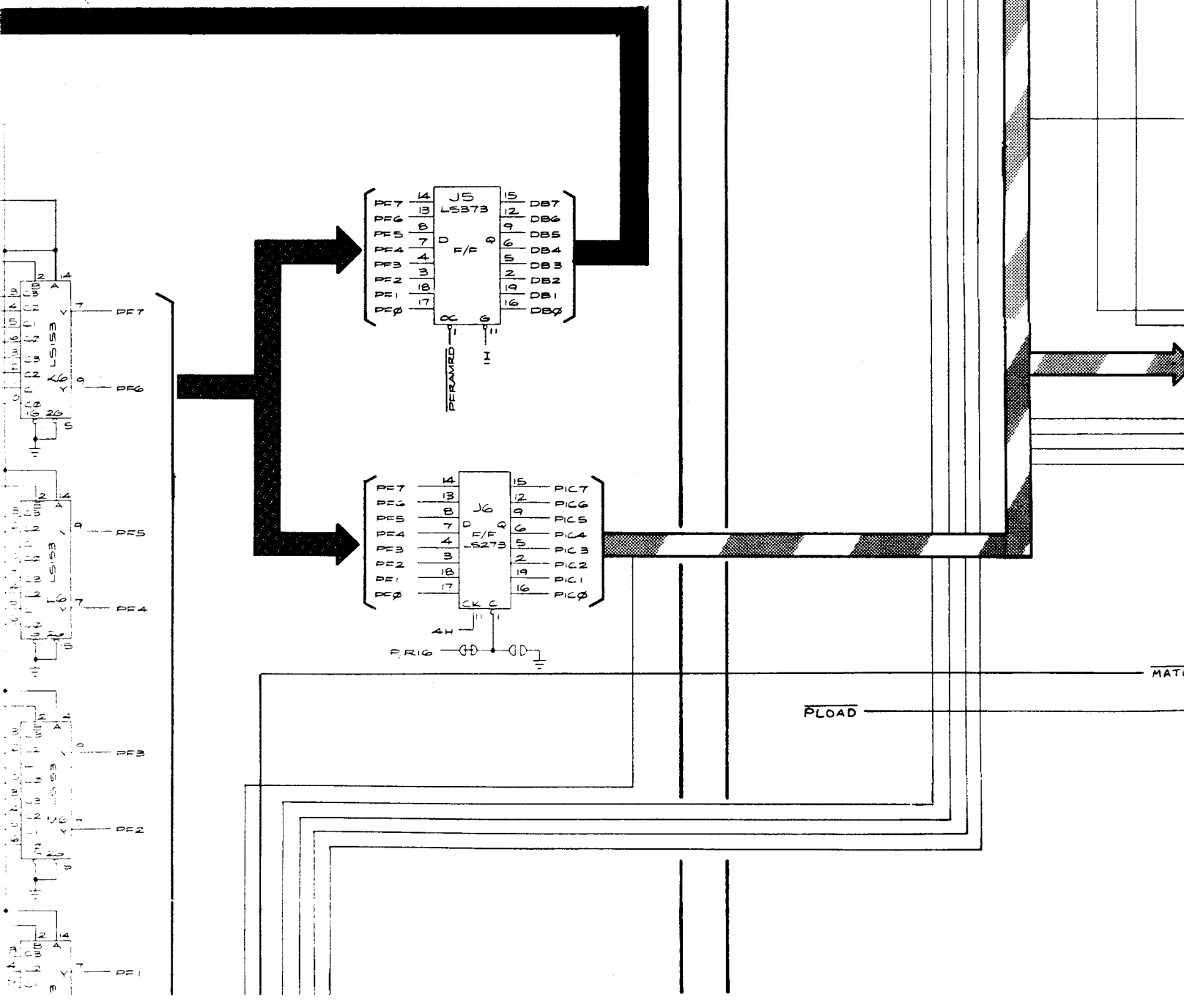


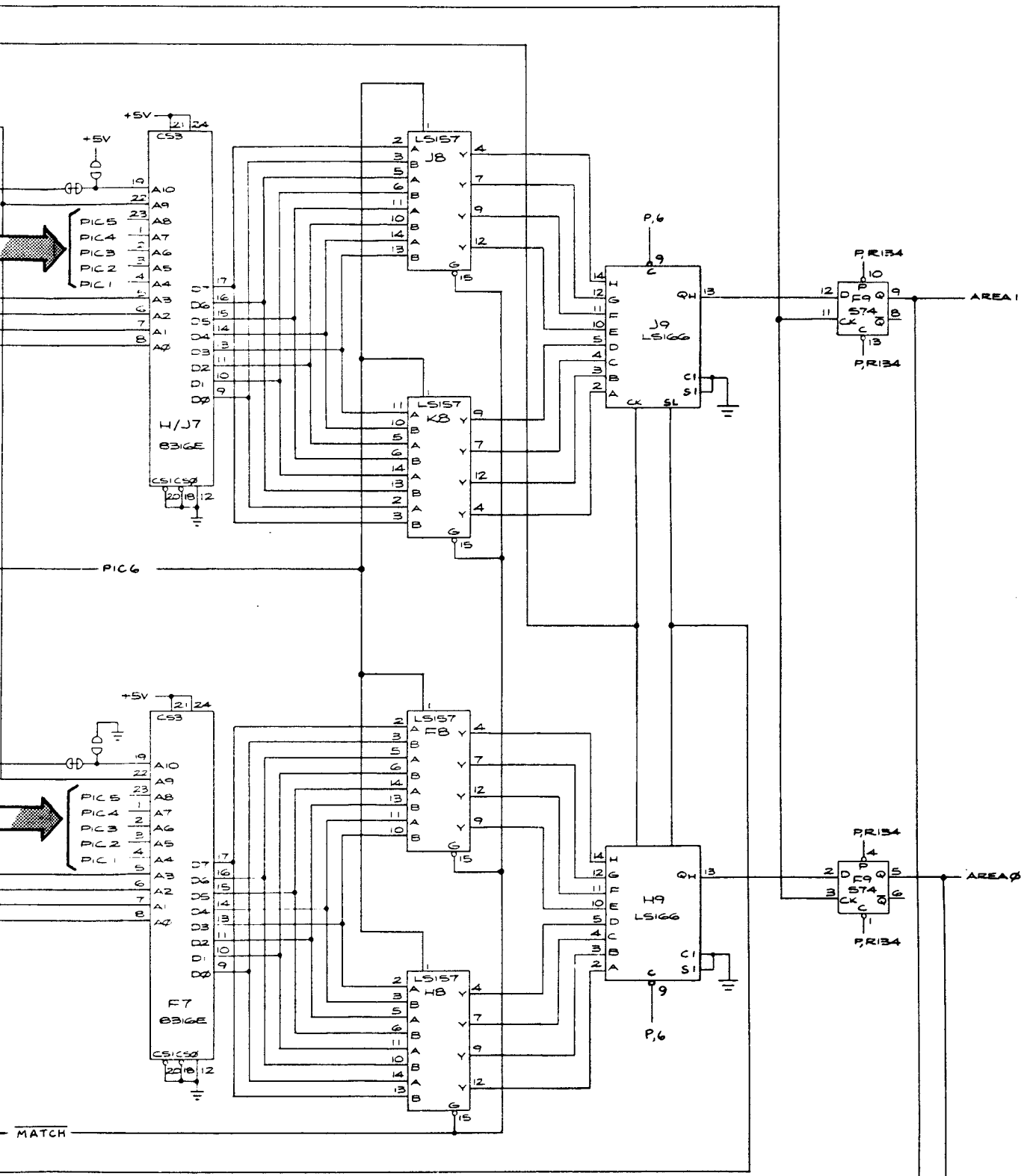
Playfield Multiplexer

: Multiplexer receives playfield data from the playfield memory nd the output (PF0-PF7) is a code that determines what is 1) dis- ıonitor, or 2) read or updated by the MPU. The Playfield Multiplexer -ct multiplexers K6, L6, M6, N6 and P6.

s low and 4H is high, AB4 and AB5 from the MPU address bus is the from P6. This output is applied to multiplexers K6, L6, M6, and N6 s. When the MPU is accessing the playfield code multiplexer, the either being read or updated by the MPU. When 256H is high and 4H ts from the sync generator (128H and 8V) are the selected outputs. hen select which bits of data PFD0-PFD31 are sent out via K6, L6, the playfield codes that eventually are displayed on the monitor.

codes (PF0-PF7) are latched by J5 and J6 to the MPU data bus (J5) re data PROM circuitry (J6). When $\overline{\text{PFRAMD}}$ is low and 1H from the goes high, the inputs on J5 (PF0-PF7) are latched out to the MPU via 4H on pin 11 of J6 goes high, the inputs (PF0-PF7) are latched to the OM circuitry.





Picture Data ROM Circuitry

The picture data ROM circuitry receives picture information, assigns a color code to the information and sends it to the color PROM circuitry. The picture data ROM circuitry consists of ROM devices F7 and H/J7, multiplexers F8, H8, J8, K8, shift registers H9 and J9, and latch F9.

Testing the Option Switches

1. Perform the CAT Box preliminary set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/$\overline{W}$ to READ
   d. Key in address 0800 (N9) or 0801 (N8)
   e. R/$\overline{W}$ MODE to STATIC

3. Activate the switch while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the switch is operating properly.

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ATARI®

Sheet 2, Side B

Centipede™

Joystick Circuitry
Mini-Trak Ball™ Circuitry
Player Input Circuitry
Video Output Circuitry
Audio Output Circuitry
Coin Counter Output Circuitry
Option Input Circuitry
High Score Memory Circuitry

Section of 037241-01 C+

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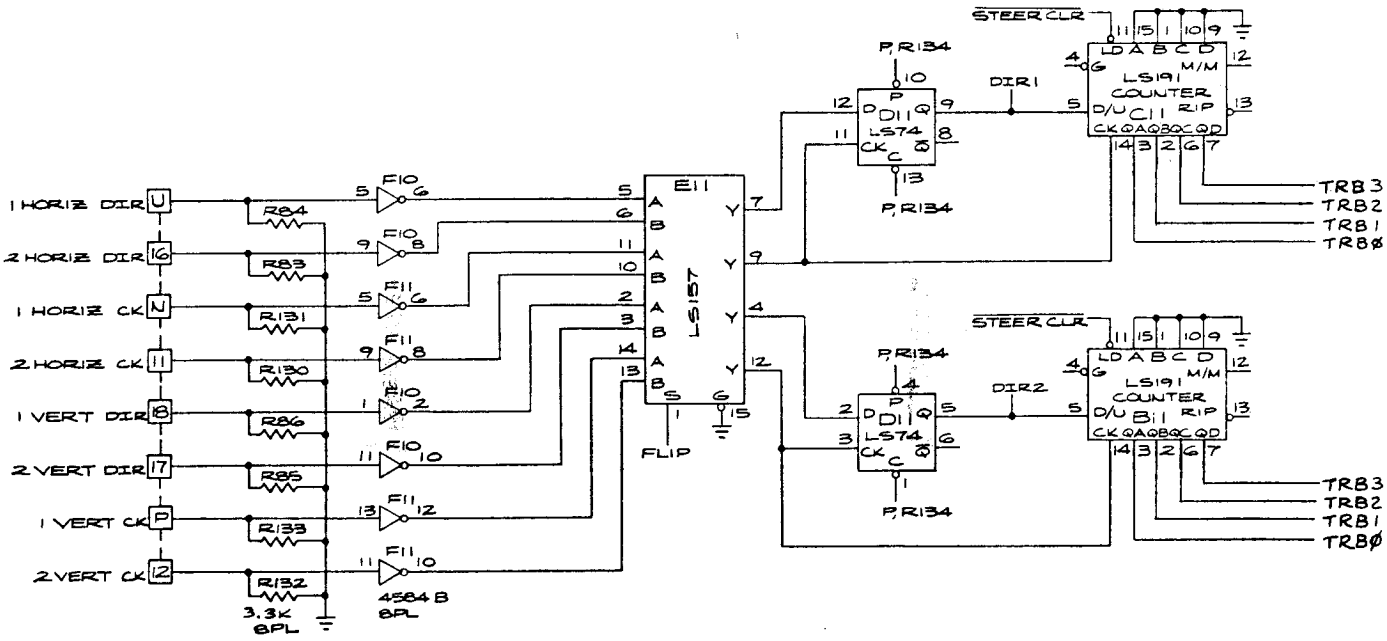
Coin Counter Output Circuit

This circuit consists of coin counter drivers Q6, Q7, and Q8 and data latch M10. The circuit is addressed by the MPU on AB0-AB2 and written by the MPU on data line DB7. When the input to a driver is clocked high, its collector goes low grounding the return of the coin counter in the coin door.

Mini-Trak Ball™ Circuitry



Testing the Mini-Trak Ball™ Inputs

1. Perform the CAT Box Preliminary Set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/$\overline{W}$ to READ
   d. Key in address 0C00 (vertical) or 0C02 (horizontal)
   e. R/$\overline{W}$ MODE to PULSE

3. Spin the Mini-Trak Ball™ while monitoring the DATA DISPLAY. The DATA DISPLAY will change if the Mini-Trak Ball input is operating properly.

ovide 6 extra colors for a total of 14.

1. If A8 pin 11 is low, transistor Q5 conducts and draws current from COLOR 3. The result is a pale blue when COLOR 1 and COLOR 2 are off.
2. If A8 pin 10 is low, transistor Q4 conducts and draws current from COLOR 2. The result is a pale green when COLOR 1 and COLOR 3 are off.

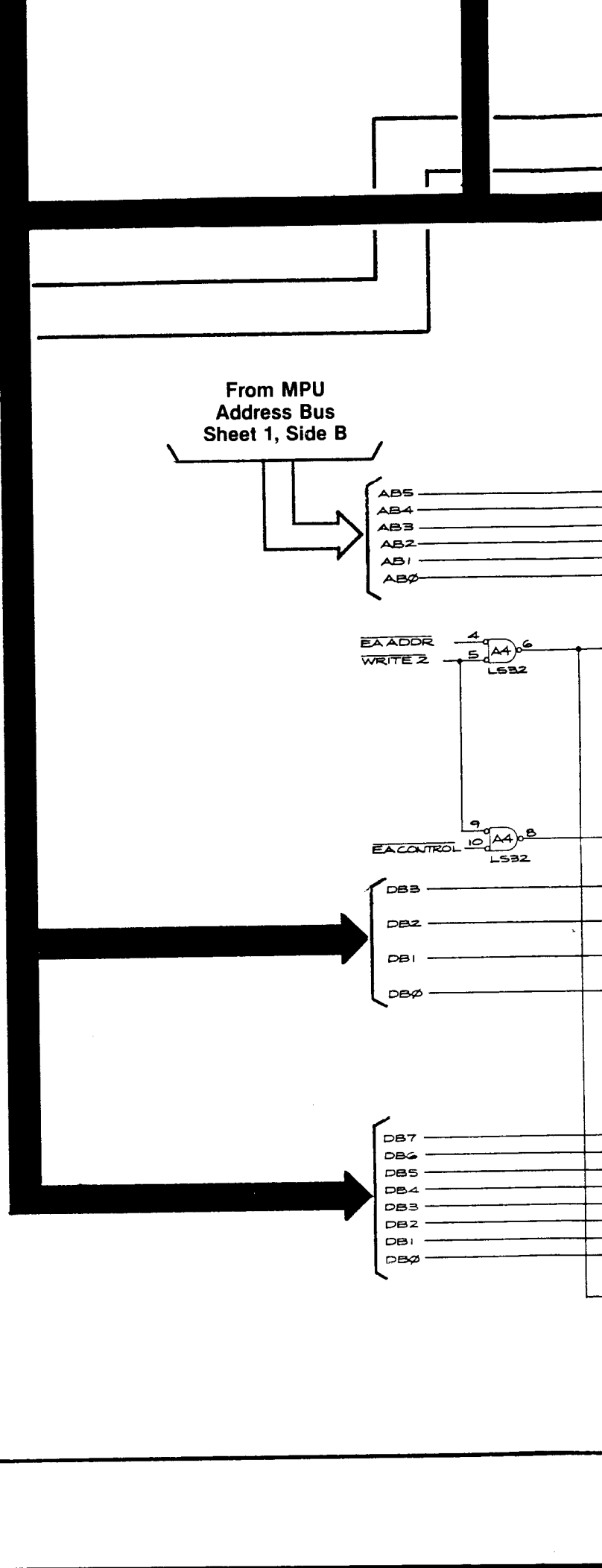
High Score Memory Circuitry

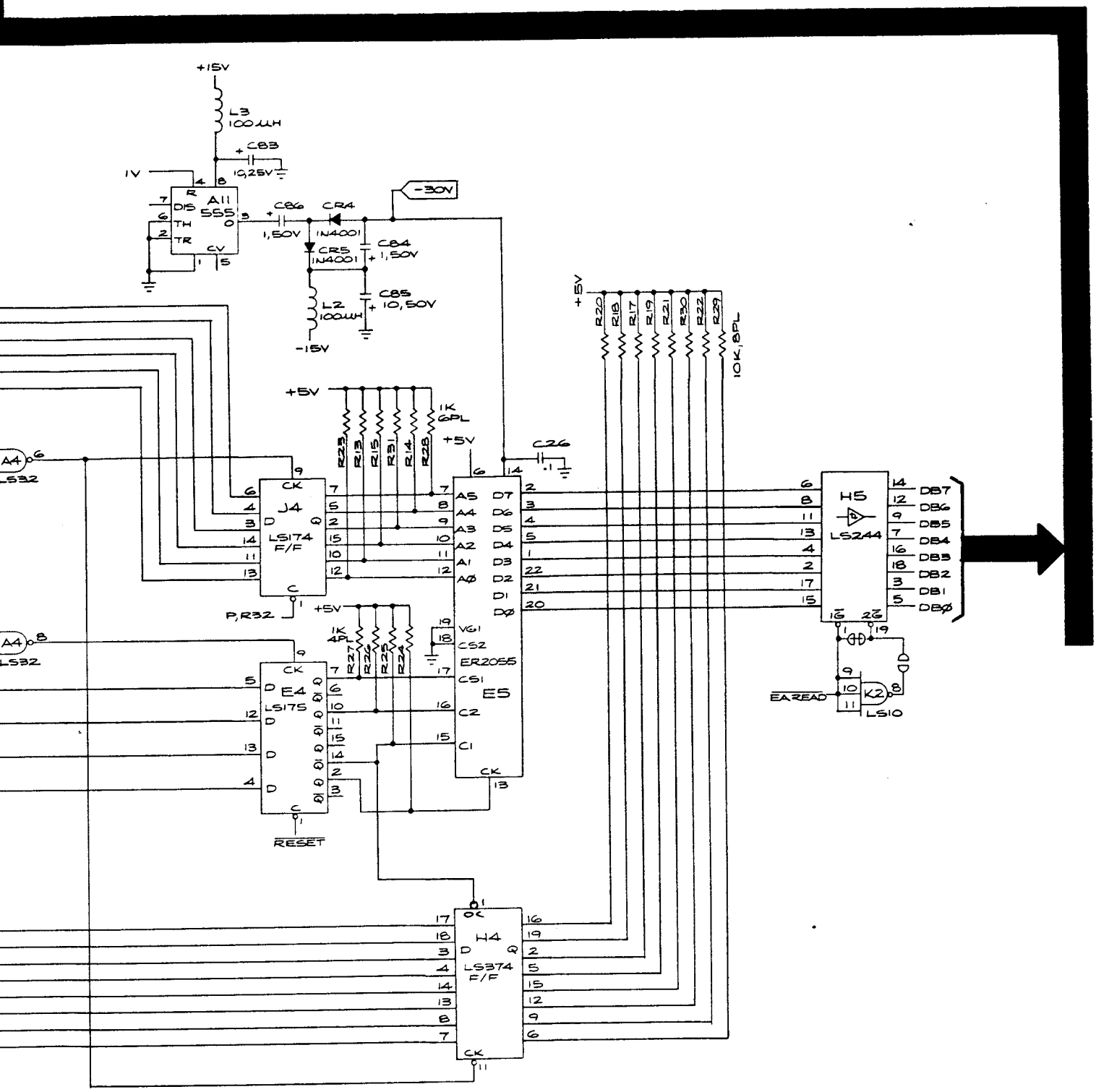
The High Score Memory circuit stores the three best scores and other pertinent information. These scores are saved even if power is removed from the game. The High Score Memory circuit consists of an erasable reprogrammable ROM E5, latches E4, H4, J4, buffer H5 and timer A11.

A11 produces a 0-15V square wave at a 1V rate. This signal, when +15V, forward biases diode CR5 and allows capacitor C86 to charge to −29V. When the signal is 0V, CR5 is cutoff and CR4 is forward-biased which causes C84 to develop a charge. C84 charges to approximately −28V. This is the potential required for EAROM C0 to operate.

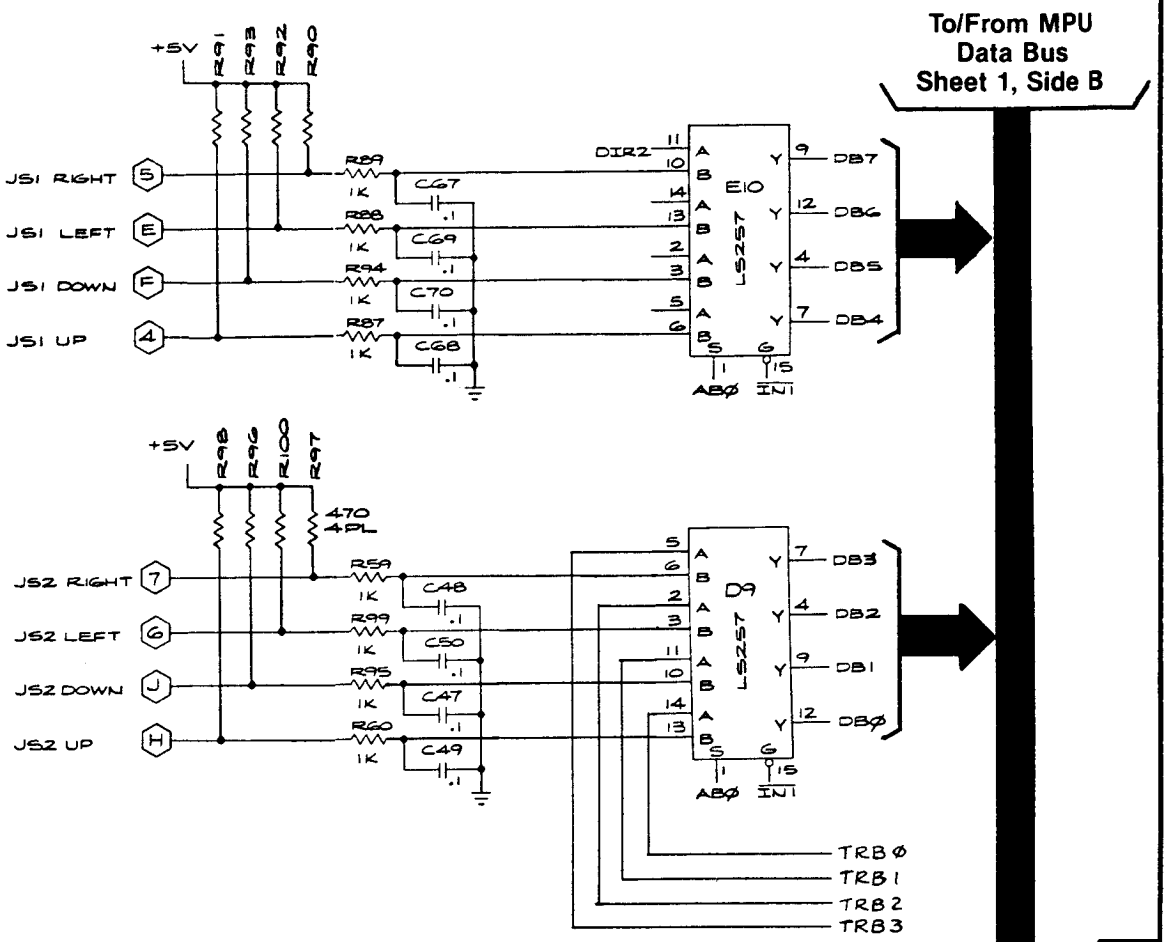
The MPU addresses the EAROM (AB0-AB5) when a low $\overline{\text{EAADDR}}$ gates $\overline{\text{WRITE2}}$ at gate A4. The trailing edge of the gated pulse latches the address information to the EAROM E5 via J4. Data is latched by H4 at the same time. The EAROM mode (read, write or erase) is determined by DB0-DB3 at latch E4. A low $\overline{\text{EACONTROL}}$ gates $\overline{\text{WRITE2}}$ at gate A4. The trailing edge of this gated pulse latches the data into the EAROM E5 via latch H4.

Data is read from the EAROM when $\overline{\text{EAREAD}}$ on pin 1 of buffer H4 goes low.

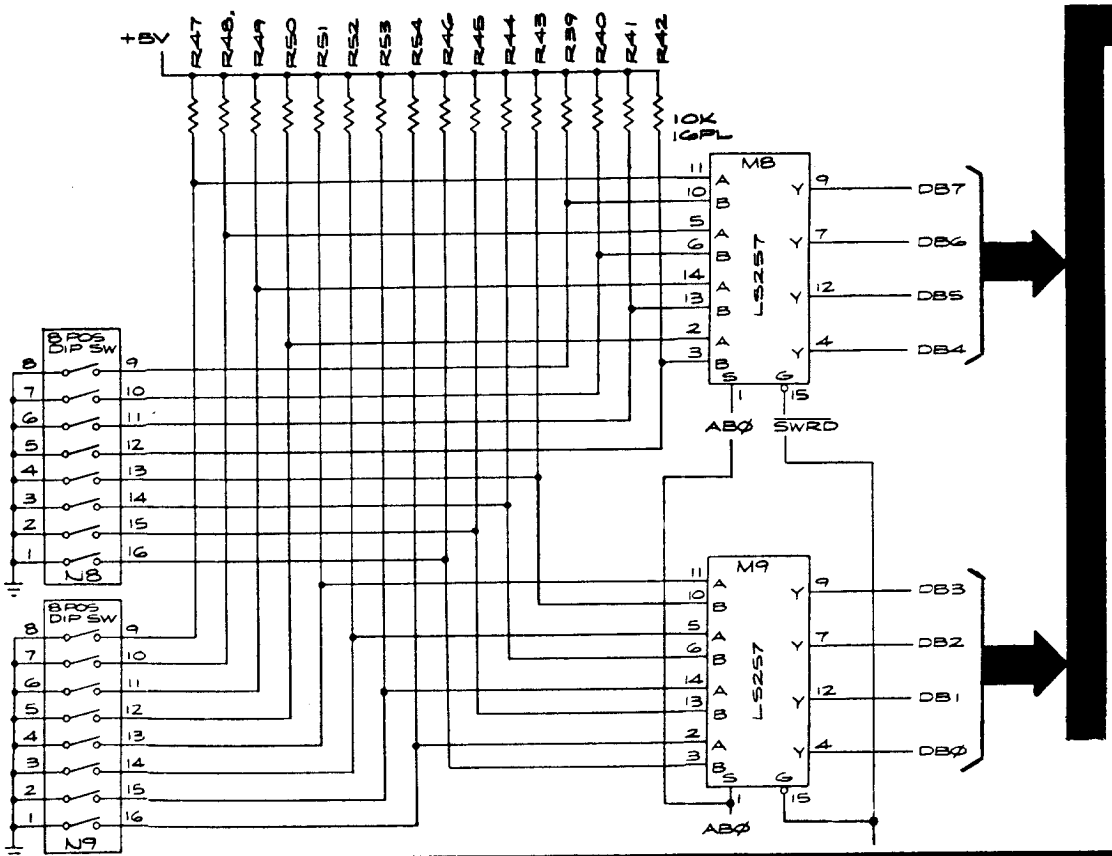



+15V
L3
100µH
C83
10,25V
1V
A11
555
C86
1,50V
CR4
1N4001
-30V
CR5
1N4001
C84
1,50V
C85
10,50V
L2
100µH
-15V
+5V
1K
6PL
R23
R13
R15
R31
R14
R28
C26
J4
LS174
F/F
P,R32
A4
LS32
E4
LS175
RESET
R27
R26
R25
R24
1K
4PL
E5
ER2055
VG1
CS2
CS1
C2
C1
H4
LS374
F/F
R20
R18
R17
R19
R21
R30
R22
R29
10K,8PL
H5
LS244
DB7
DB6
DB5
DB4
DB3
DB2
DB1
DBØ
EA READ
K2
LS10
H SYNC
V SYNC
B7
LS08
A4
07
220
COMP SYNC
R73
330
VID RET

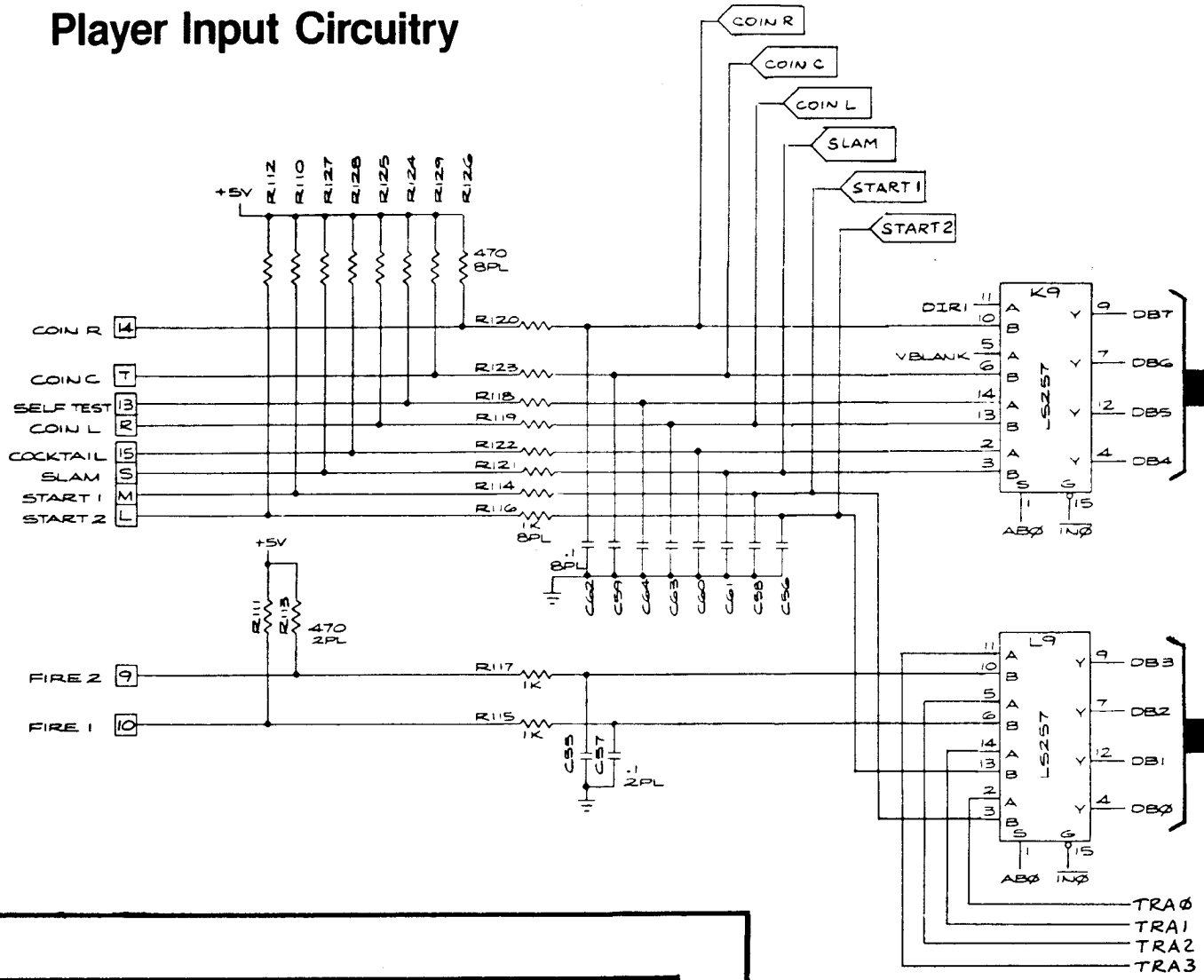
Joystick Circuitry



Option Input Circuitry

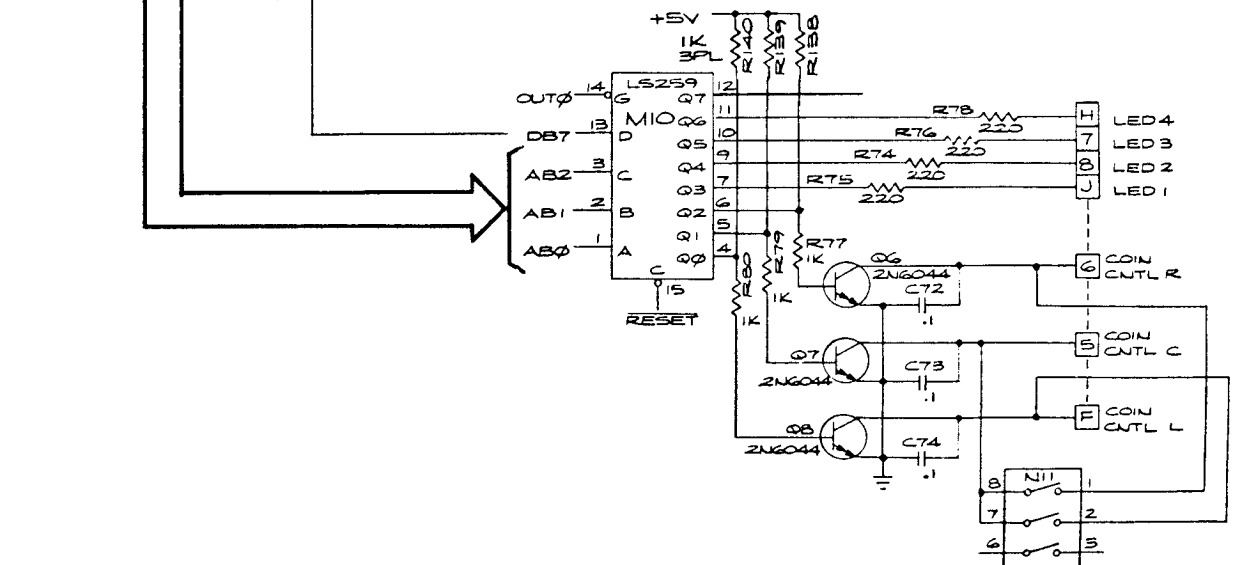


Player Input Circuitry



Coin Counter Output Circuitry

From MPU Address Bus Sheet 1, Side B



Testing the Player Inputs

1. Perform the CAT Box Preliminary Set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/$\overline{W}$ to READ
   d. Key in address 0C00 (self-test switch only) or 0C01 (all others).
   e. R/$\overline{W}$ MODE to STATIC

3. Activate the following player input switches, one at a time, while monitoring the DATA DISPLAY:
   a. Coin Right
   b. Coin Left
   c. SLAM
   d. FIRE
   e. START 1
   f. START 2

4. The DATA DISPLAY will change if the switches are operating properly.

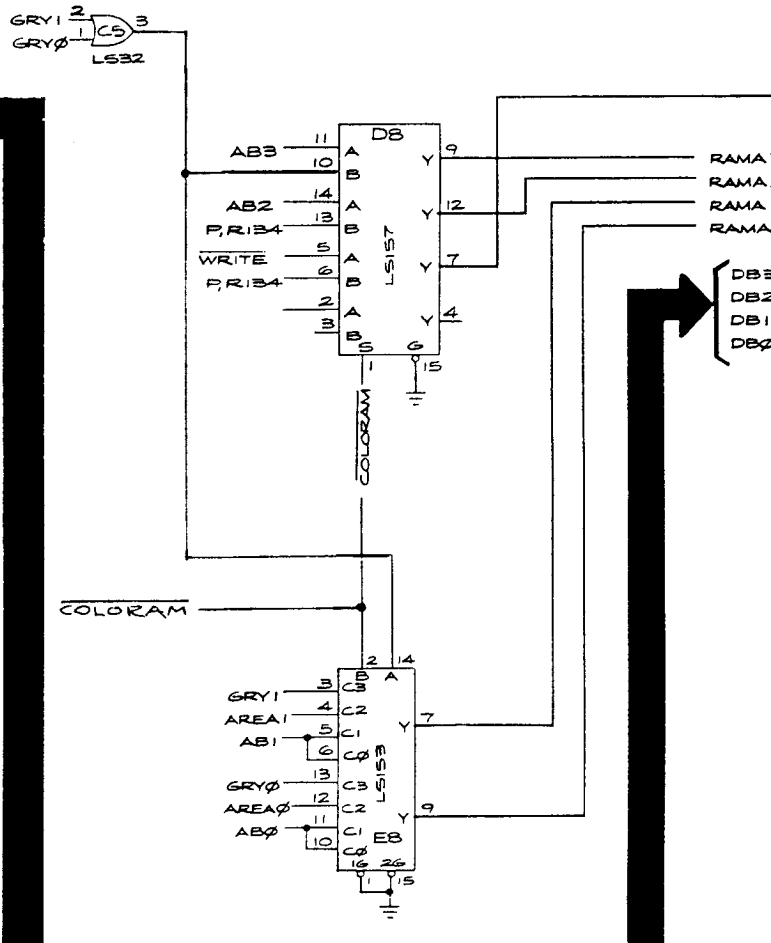
Testing the Audio Outputs

1. Perform the CAT Box preliminary set-up.

2. Set the CAT Box switches as follows:
   a. DBUS SOURCE to DATA
   b. BYTES to 1
   c. R/$\overline{W}$ to WRITE
   d. Key in address or press ADDRESS INCR
   e. Press DATA SET
   f. Key in data
   g. Set R/$\overline{W}$ MODE to PULSE, then to OFF.
   h. For each address, repeat sequence starting at Step d.

ADDRESS	DATA	RESULTS
100F	00	
100F	03	
1000	55	
1001	AF	Pure tone is heard from channel 1 ou
1001	00	Channel 1 output is turned off.
1002	55	
1003	AF	Pure tone is heard from channel 2 ou
1003	00	Channel 2 output is turned off.
1004	55	
1005	AF	Pure tone is heard from channel 3 ou
1005	00	Channel 3 output is turned off.
1006	55	
1007	AF	Pure tone is heard from channel 4 ou
1007	00	Channel 4 output is turned off.

Denotes a test point

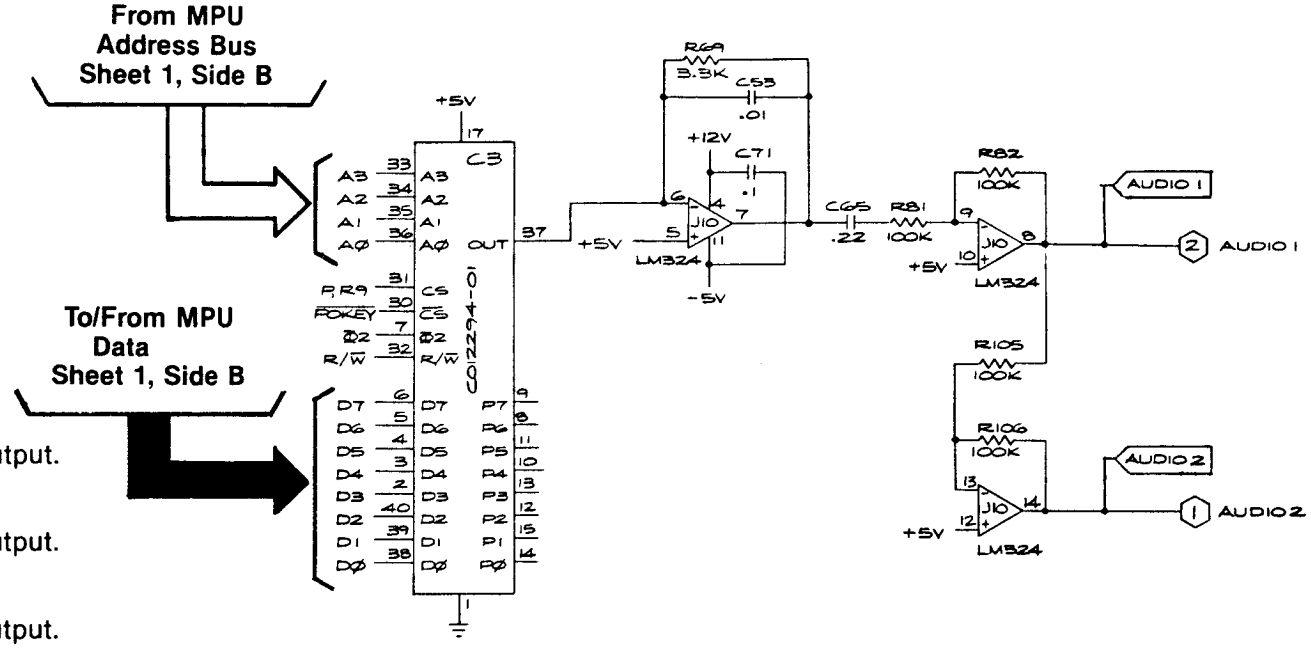


The video output circuit receives motion object, playfield, address and data inputs and produces a video output to be displayed on the game monitor. In order to read out of the color RAM, GRY0 and GRY1 from the motion object circuitry are multiplexed with AREA0 and AREA1 from the playfield circuit by E8. The output, selected by GRY0 or GRY1, is RAMA0-RAMA3 (RAM ADDRESS).

RAMA0-RAMA3 are applied to color RAM C8. The colors red, green, blue and an alternate color bit are outputs. The three color bits are latched by A8 as the game video in the three basic colors (or shades of gray in a black and white monitor). When the alternate color bit (C8 pin 11) is active, an alternate shade of blue or green is available.

The following conditions, along with the various combina-

Audio Output Circuitry



nnel 1 output.
off.

nnel 2 output.
off.

nnel 3 output.
off.

nnel 4 output.
off.

Video Output Circuitry

