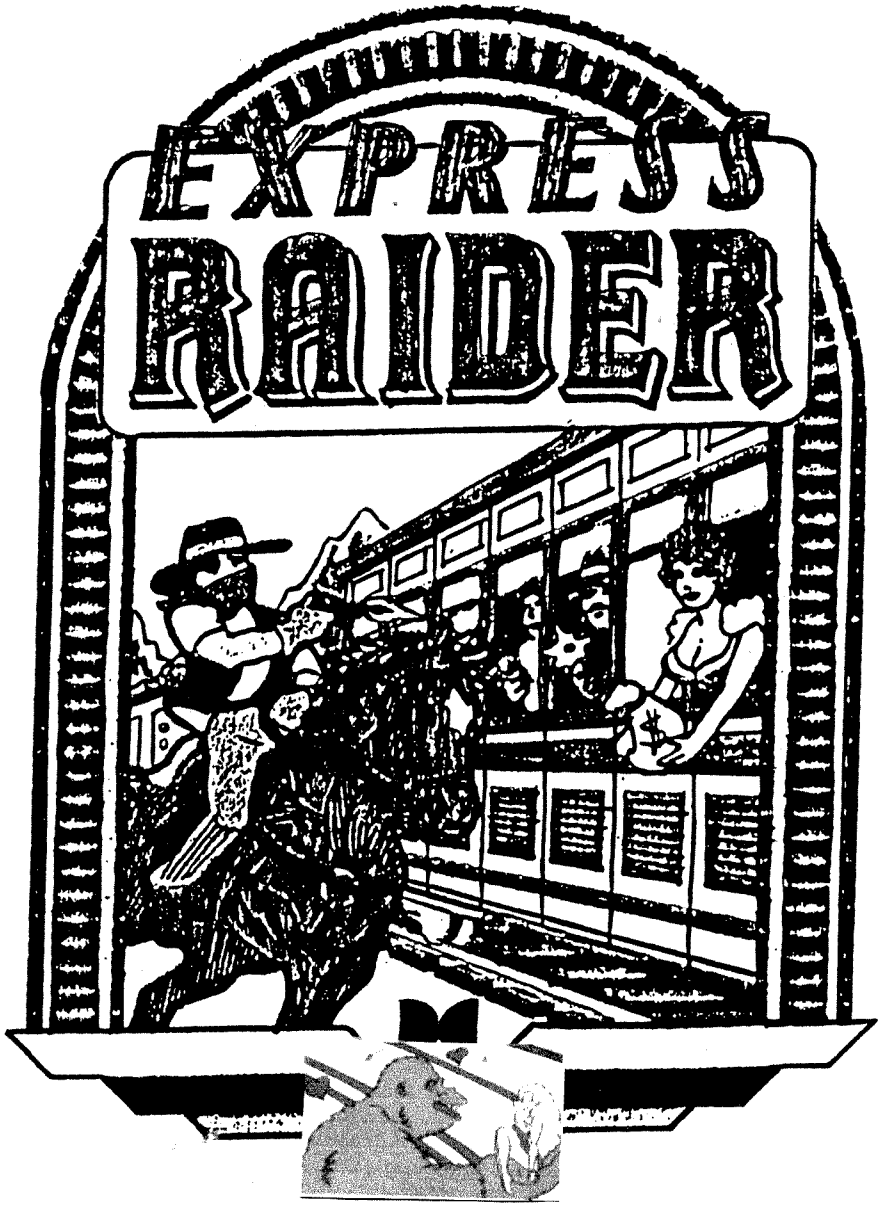
CONVERSION KIT

installation & service manual



DATA EAST USA, INC.
470 Needles Drive
San Jose, CA 95112

780-0030-00

WARNING

This equipment generates and uses radio frequency energy and if not installed and used properly, i.e., in strict accordance with the instructions manual, may cause harmful interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device persuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment.

Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Thank you for purchasing this Data East Conversion Kit. Your kit includes the following:

1	510-0056-00	PCB ASSEMBLY, EXPRESS RAIDER
1	520-0016-00	PCB ASSEMBLY, EMI FILTER DE-0209
1	450-0003-00	JOYSTICK, 8 WAY, CC.
1	545-0003-00	FLAT PLATE ADAPTOR
6	185-0001-00	PUSHBUTTON HOLDER WITH SWITCH
6	240-0001-00	PAL NUT
2	350-0001-03	PUSHBUTTON, SHORT, ORANGE
2	350-0001-06	PUSHBUTTON, SHORT, BLUE
1	350-0003-03	PUSHBUTTON, WHITE, 1 PLAYER
1	350-0003-04	PUSHBUTTON, WHITE, 2 PLAYER
1	830-0018-00	MARQUEE PLEX, EXPRESS RAIDER
1	800-0018-00	CONTROL PANEL OVERLAY, EXPRESS RAIDER
2	820-0024-00	SIDE DECAL, EXPRESS RAIDER
1	810-0011-00	UNDERLAY CARD, MONITOR, GENERIC
1	406-0019-00	LABEL, INSTRUCTIONS, EXPRESS RAIDER
1	036-0013-00	HARNESS, MAIN GENERIC KIT
1	780-0030-00	INSTALLATION & SERVICE MANUAL
1	406-0003-00	LABEL, FCC

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DATA EAST USA INC.
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1. ADJUSTMENTS & OPTIONS

A. VOLUME CONTROL. The audio volume is adjustable via a trimpot (VR1) on the CPU PCB.

B. OPERATOR SELECTABLE OPTIONS. The Operator Selectable Options can be altered by changing the settings of the Dip Switches found on the CPU PCB. Table 1 and Table 2 outline the available options.

TABLE 1		1	2	3	4	5	6	7	8
COIN VS CREDIT COIN 1	1 COIN = 1 CREDIT	OFF	OFF						
	1 COIN = 2 CREDIT	ON	OFF						
	1 COIN = 3 CREDIT	OFF	ON						
	2 COIN = 1 CREDIT	ON	ON						
COIN VS CREDIT COIN 2	1 COIN = 1 CREDIT			OFF	OFF				
	1 COIN = 2 CREDIT			ON	OFF				
	1 COIN = 3 CREDIT			OFF	ON				
	2 COIN = 1 CREDIT			ON	ON				
SWITCH 5 = ALWAYS OFF						OFF			
FLIP SCREEN	NORMAL						OFF		
	FLIP						ON		
CABINET TYPE	TABLE							OFF	
	UPRIGHT							ON	
SWITCH 8 = ALWAYS OFF									OFF

TABLE 2		1	2	3	4	5	6	7	8
NUMBER OF LIVES	THREE	OFF	OFF						
	FIVE	ON	OFF						
	ONE	OFF	ON						
	INFINITE	ON	ON						
BONUS LIVES	EVERY 50000 PTS			OFF					
	50000/80000 PTS			ON					
LEVEL OF DIFFICULTY	EASY				OFF	OFF			
	NORMAL				ON	OFF			
	HARD				OFF	ON			
	MOST DIFFICULT				ON	ON			
ATTRACT MODE SOUND	YES						OFF		
	NO						ON		
SWITCHES 7 & 8 = ALWAYS OFF								OFF	OFF

2. CONVERSION SUMMARY

One of the most important considerations determining the success of your conversion will be the condition of the machine you are converting. Obviously, if the monitor is dull in the original game, it will be no better with the conversion installed. If you have a choice, select a machine that has an instruction manual and/or good primary wiring diagrams. Try to select a machine that has previously been certified as conforming to Part 15, Subpart J, of the FCC regulations. It it important that the primary wiring contain a good noise filter in order to prevent conducted radio frequency interference.

Since it is extremely important that all visible graphics, original manufacturer's name (other than the Serial Number tag), logo's, etc., are to be removed or covered by new graphics, a proper choice of cabinet in this phase of the conversion will save you much time.

Make sure that the integrity of the cabinet is such that the converted game will not be a vandals dream. Review the control panel to identify what changes will be required so that you will be prepared. It may be necessary to drill holes in the control panel for pushbuttons, etc. before applying the new overlay. See figure 1 for suggested control layout.

The EXPRESS RAIDER game is designed to operate with a COLOR RASTER MONITOR, mounted in a HORIZONTAL position. The EXPRESS RAIDER PCB generates NEGATIVE COMPOSITE SYNC. The POWER SUPPLY requirements are: +5 volts @ 7 Amperes, and +12 volts @ 1 Ampere.

It is strongly recommended that the cabinet be wired to conform with all National and Local Electrical Code requirements before the conversion is attempted. The system must have adequate noise filtering on the AC line to prevent unwanted conducted radio frequency radiation, which could be in violation of FCC regulations.

According to the FCC and various other agencies, every video game must be clearly and permanently LABELED with the name and address of the Original Manufacturer, Date of Manufacture (or serial number), Voltage rating, Current rating, Suitability for indoor or outdoor use, and unit model number. In addition, the FCC requires that, after conversion, the unit must be labeled with a suitable warning stating that radio frequency interference may result from use in a residential area. An acceptable warning sticker is enclosed in your kit.

IT IS THE RESPONSIBILITY OF THE INDIVIDUAL PERFORMING THE CONVERSION TO INSURE THAT ALL LABELING REQUIREMENTS ARE CONFORMED WITH!

3. COSMETICS

All components that contain the Original Manufacturer's name (other than the serial number plate), graphics, logos, or game play information must be removed or covered by some means. Do not destroy the Display Plex or the Control Panel as these items may have to be used or modified for your conversion.

A cardboard underlay has been provided to be placed under a clear Display Plex. This underlay contains the game instructions. If the existing Display Plex has silkscreened artwork on it, you will need to strip it clean (lacquer thinner is usually effective) or replace it with a clear plex. If necessary, trim the cardboard underlay, with a razor blade, down to the size of the Display Plex.

The control panel overlay supplied in this kit is designed to allow the player controls to be placed in a variety of positions. First, strip off the original controls and the overlay and then thoroughly clean and deburr the control panel. If necessary, drill out any required holes in the control panel. The new overlay has a strong adhesive on one side of it, so be sure you know how you want it positioned before peeling off the paper backing and applying it to the panel. When applying the overlay, smooth it out from the center to the edges, being sure remove all trapped air bubbles. Trim any excess material, and material from mounting holes, with a razor blade or sharp knife.

A new 8 way joystick is provided with the kit. The flat plate adaptor may be used as a template for any required holes for the joystick. Appropriate color pushbuttons, button holders, and pal nuts are supplied. The pushbuttons require a 1 1/8 inch diameter mounting hole.

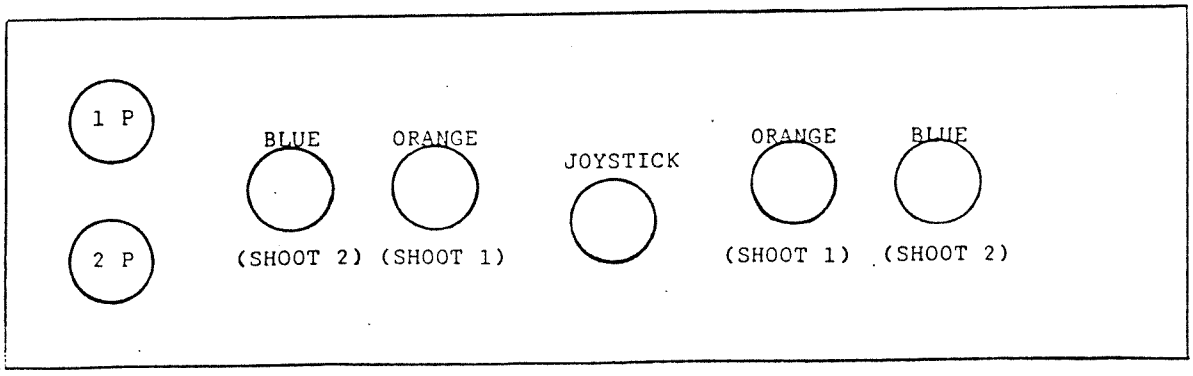


FIGURE 1

4. SPECIAL INSTRUCTIONS

Your conversion kit has been supplied with a main harness which connects the EMI Filter/Adaptor PCB to the various places in the game in which you are converting. Each wire has been labeled as to its function. If in doubt, refer to the generic main harness diagram in figure 3.

1. Follow all instructions in this manual relating to selecting a game to install this conversion into.

2. Mount the new Logic PCB set in a convenient location. An EMI cage is not necessary for this conversion, but the use of the EMI Filter/Adaptor PCB is MANDATORY!

3. Plug the EMI Filter/Adaptor PCB into the EXPRESS RAIDER as shown in figure 2.

4. Plug the Generic Main Harness onto the EMI Filter/Adaptor PCB.

5. Neatly route all of various main harnessing around the cabinet to the proper destination points and terminate as required.

6. When you are certain that you have made all the connections properly, turn on the main power and wait for the monitor to warm up. Watch for any signs of smoke or cracking noises indicating a problem. You may have to adjust your monitor to center the picture or enhance the colors. MEASURE AND ADJUST THE +5 VOLT POWER SUPPLY AT THIS TIME!

When you have finished converting your game, be sure to attach the FCC WARNING label to the rear of the cabinet. Failure to do so is a violation of the FCC regulations.

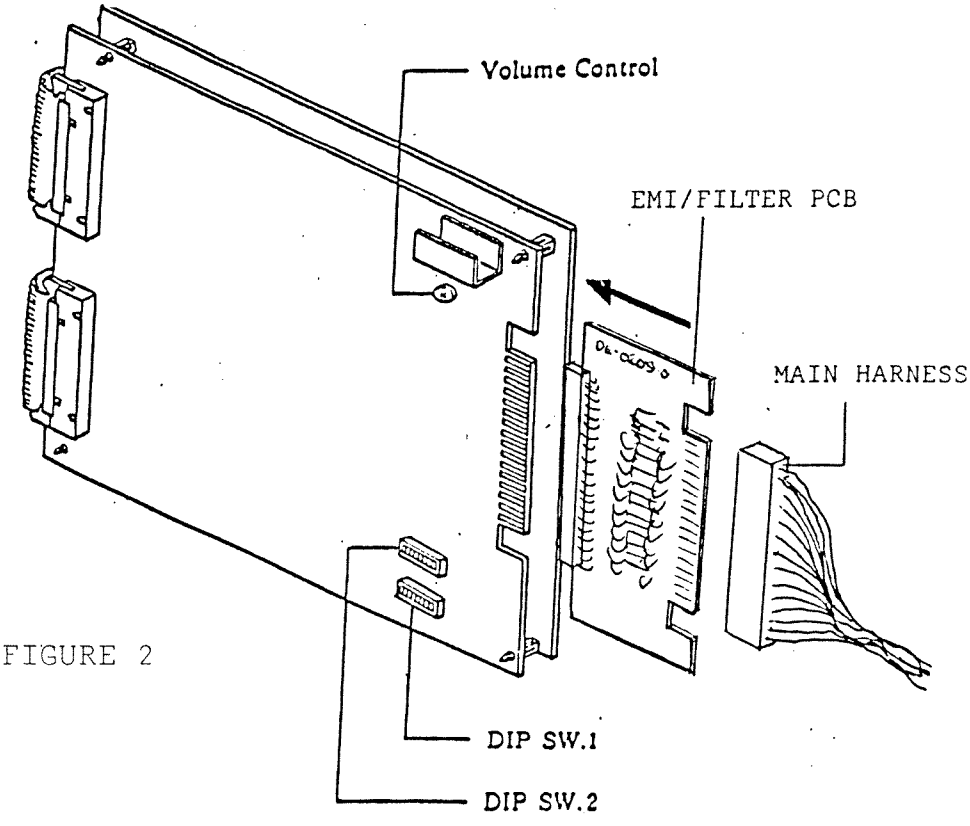


FIGURE 2

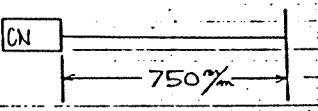
仕様，名称

1	A	GN(ミド)	DOWN
2	B	YL(キ)	UP
3	C	OR(ダイ)	LEFT
4	D	RD(アカ)	RIGHT
5	E		
6	F		
7	H		
8	J	SB(ソラ)	SERVICE
9	K	BL(アオ)	SHOOT 1 (ORANGE BUTTON)
10	L	VI(ムラ)	SHOOT 2 (BLUE BUTTON)
11	M	BN(チャ)	1P
		RD/WH(アカ/シロ)	2P
12	N	GN(ミド)	COIN1
		RD(アカ)	COIN2
13	P	VI(ムラ)	COUNTER 1
		SL(ハイ)	COUNTER2
14	R	BL/WH(アオ/シロ)	TV B
		GN/WH(ミド/シロ)	TV G
15	S	WH/BK(シロ/クロ)	SYNC
		RD/WH(アカ/シロ)	TV R
16	T		
17	U	WH(シロ)	SPEAKER(+)
		BK/WH(クロ/シロ)	SPEAKER(−)
18	V	★OR(ダイ)	+12V
		★BL(アオ)	−5V
19	W	★RD(アカ)	+5V
		RD(アカ)	
20	X	★RD(アカ)	+5V
		RD(アカ)	
21	Y	BK/WH(クロ/シロ)	TV GND
		★BK(クロ)	GND
22	Z	★BK(クロ)	GND
		★BK(クロ)	GND

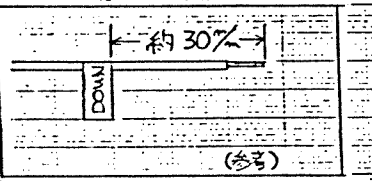
○コネクター　HRS CR7E-44DA-3.S6E

○線材　★印は AWG 20 STYLE 1007
その他 指定なきものは
AWG 22 STYLE 1007

○線長



○先端処理　5m/m ムキ 5m/m 半田加工のこと
行先指示名札 貼り付け加工のこと



※コネクター半田部分は熱収縮チューブ加工のこと

NOTE: PINS 1〜22 = COMPONENT SIDE
PINS A〜Z = SOLDER SIDE

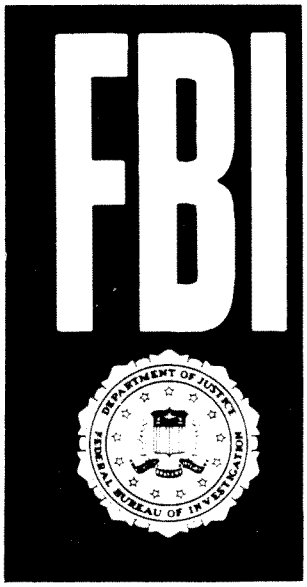
FIGURE 3

出図
60.9.05
データ・イースト(株)
生技部

記号	担当	年月日	改訂個所	符号	部品，図面番号	名称	仕様，材質	日/月

材質	処理	公差	名称
			GENERIC HARNESS Assy

承認	検図	検図	担当	単位 mm	図番 036-0013-00	1
				尺度 /		1

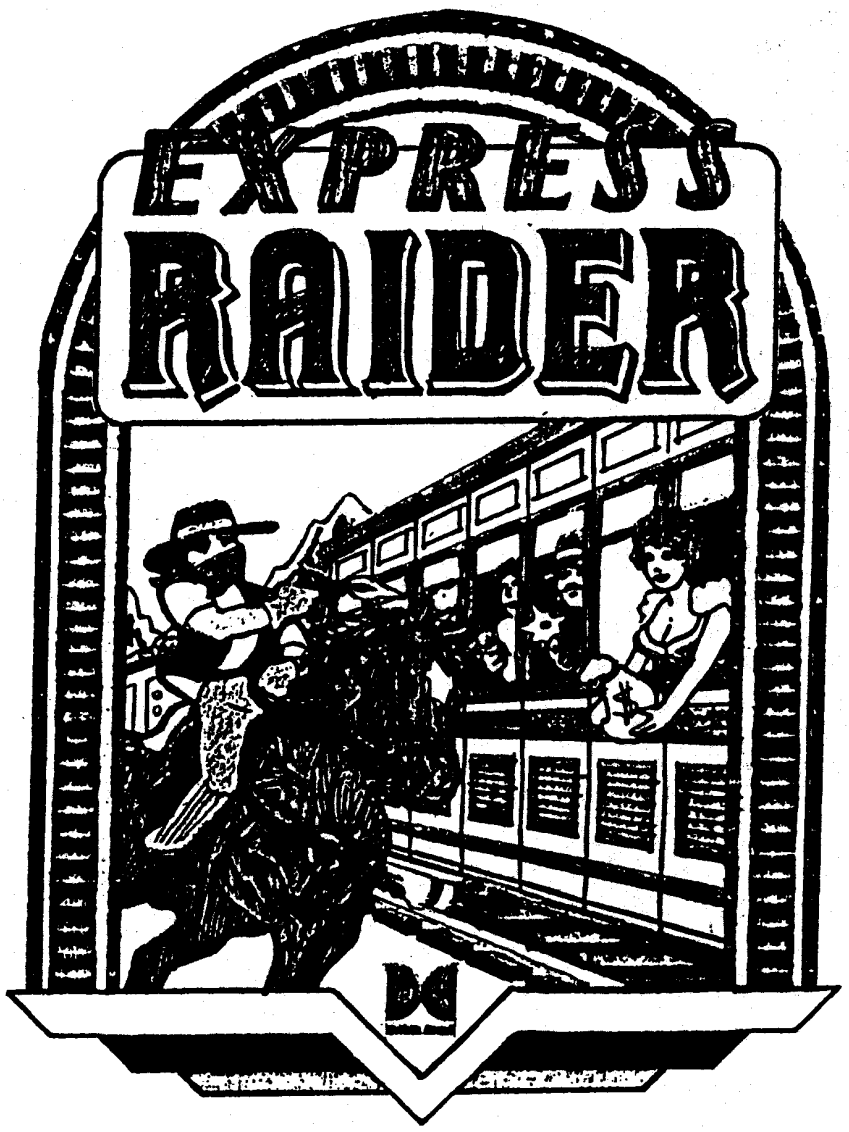


WARNING

Federal law provides severe civil and criminal penalties for the unauthorized reproduction, distribution, or exhibition of copyrighted audiovisual works and video games.

The Federal Bureau of Investigation investigates allegations of criminal copyright infringement.

PCB SCHEMATICS



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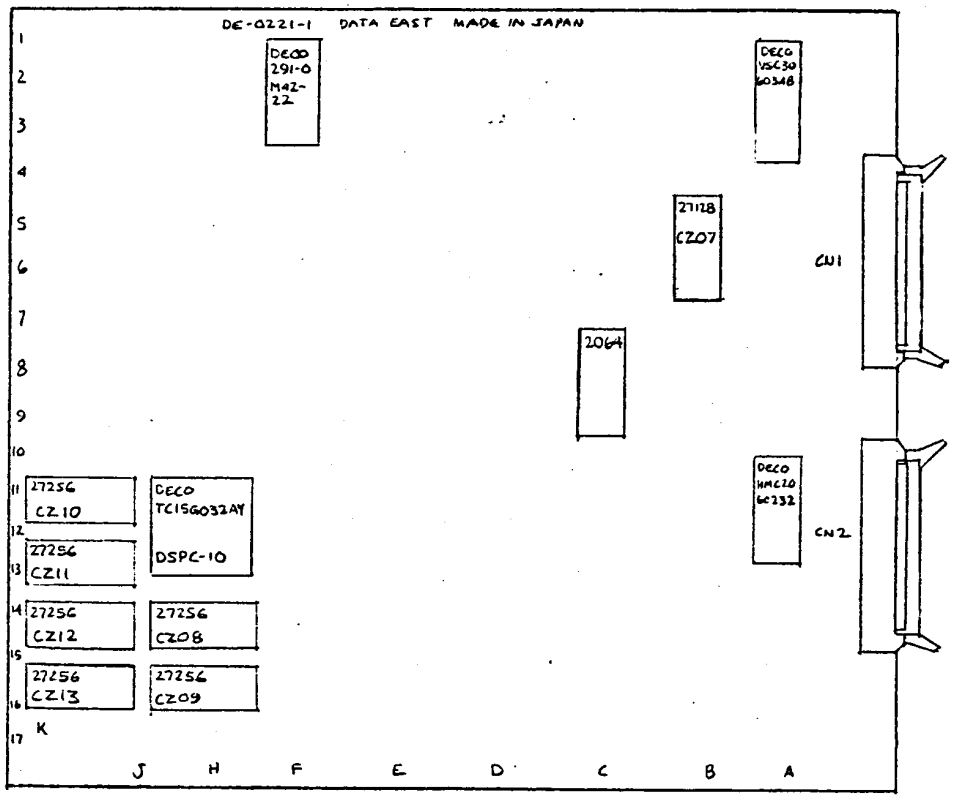
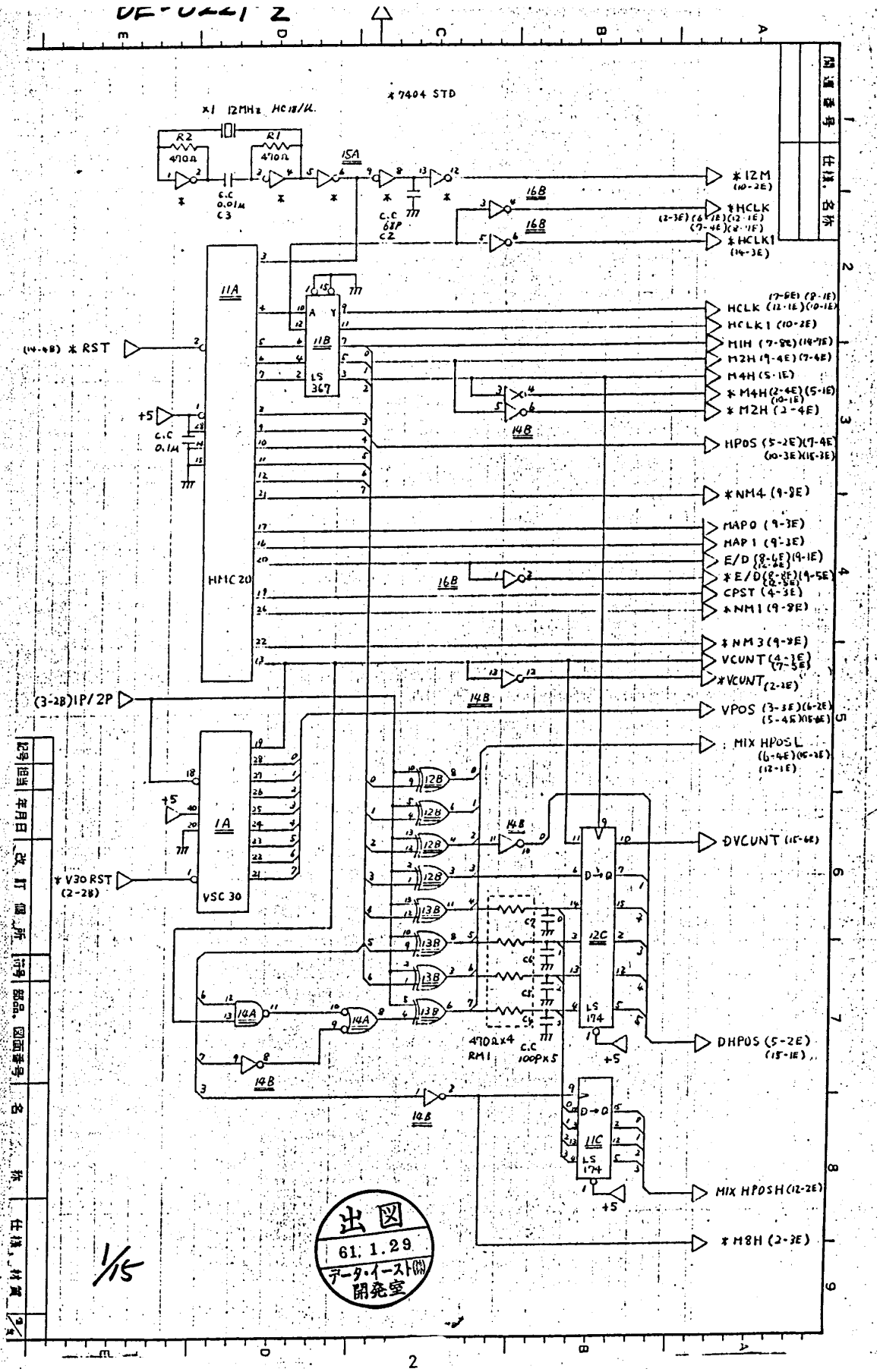
470 Needles Drive
San Jose, CA 95112

780-0034-00

1. EXPRESS RAIDER BOTTOM PCB, DE-0221-1 (520-0069-00)




VE-0421 2
*7404 STD
X1 12MHz HC18/U.
R2 470Ω
R1 470Ω
C3 C.C 0.01M
C2 C.C 68P
ISA
*12M (10-2E)
*HCLK (2-3E)(6-1E)(12-1E)(7-4E)(8-1E)
*HCLK1 (14-3E)
16B
14B
11A
11B
LS 367
HMC 20
1A
VSC 30
12B
13B
14A
12C
11C
LS 174
(14-4B) *RST
+5
C.C 0.1M
(3-2B) IP/2P
*V30 RST (2-2B)
HCLK (12-1E)(10-1E)
HCLK1 (10-2E)
MIH (7-9E)(14-7E)
M2H (9-4E)(7-4E)
M4H (5-1E)
*M4H (2-4E)(5-1E)(10-1E)
*M2H (2-4E)
HPOS (5-2E)(7-4E)(10-3E)(15-3E)
*NM4 (9-3E)
MAP0 (9-3E)
MAP1 (9-3E)
E/D (8-4E)(9-1E)(12-3E)
*E/D (8-2E)(9-5E)(12-3E)
CPST (4-3E)
*NM1 (9-8E)
*NM3 (9-3E)
VCUNT (4-1E)(7-5E)
*VCUNT (2-1E)
VPOS (3-3E)(6-2E)(5-4E)(15-4E)
MIX HPOSL (6-4E)(16-3E)(12-1E)
DVCUNT (15-6E)
DHPOS (5-2E)(15-1E)
470Ω×4 RM1
C.C 100P×5
MIX HPOSH (12-2E)
*M8H (2-3E)
出図
61. 1. 29
データ・イースト㈱
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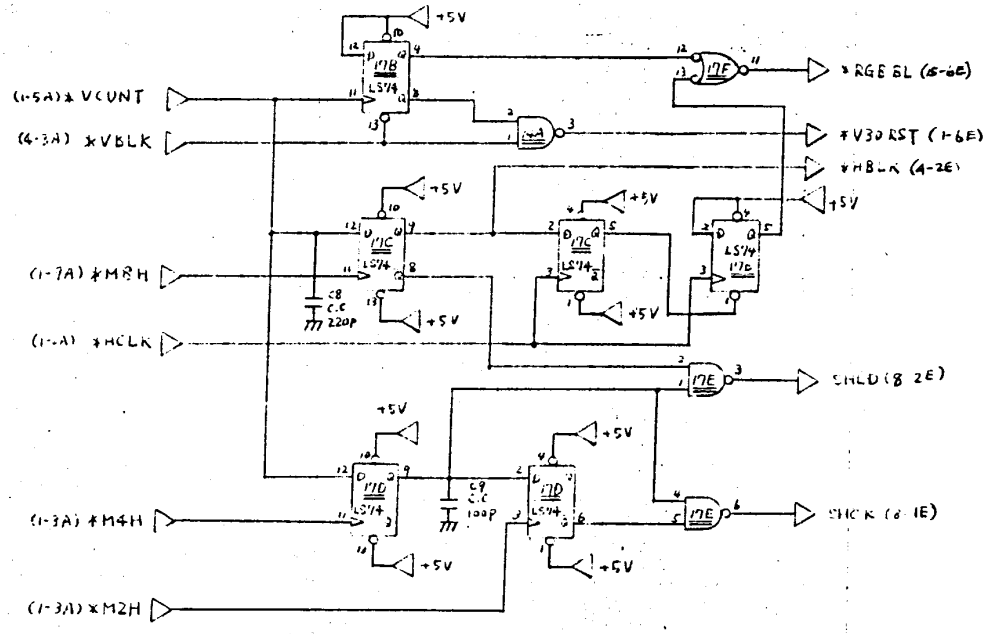
1/15



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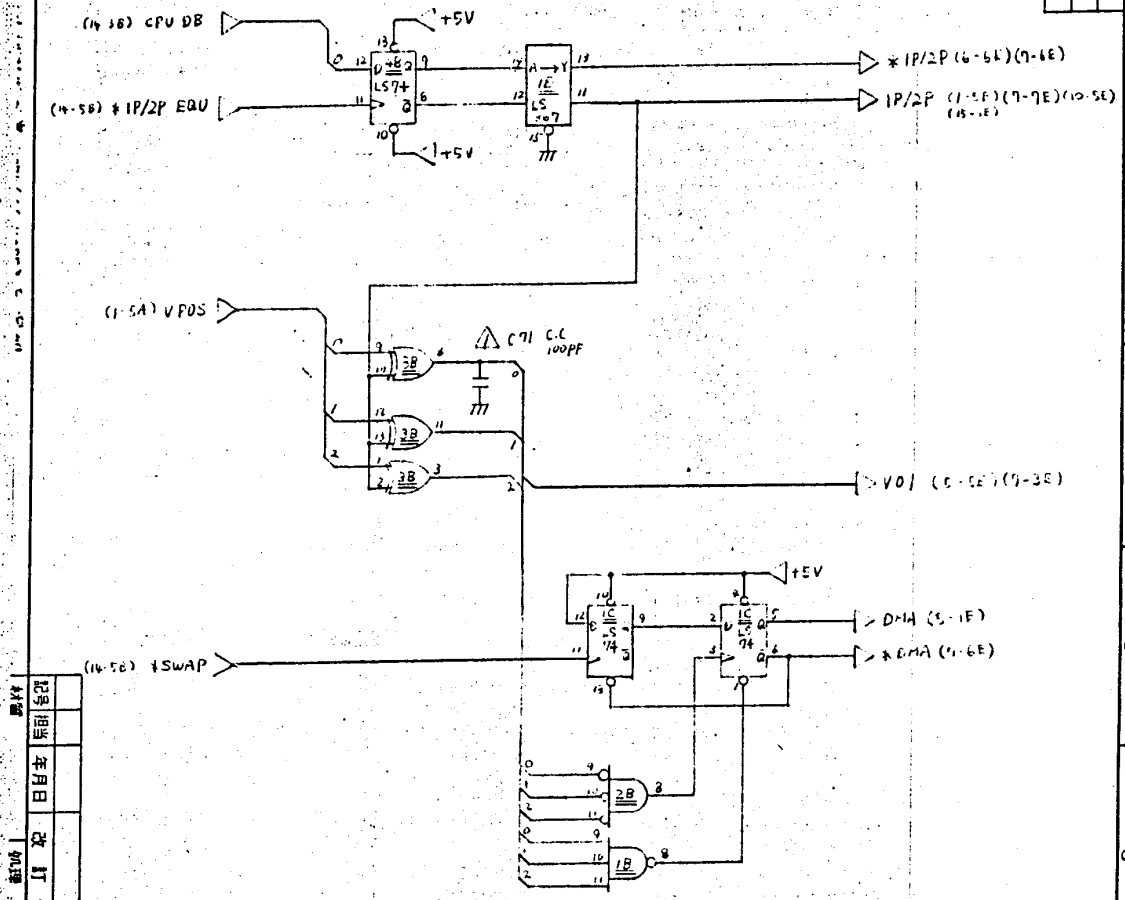

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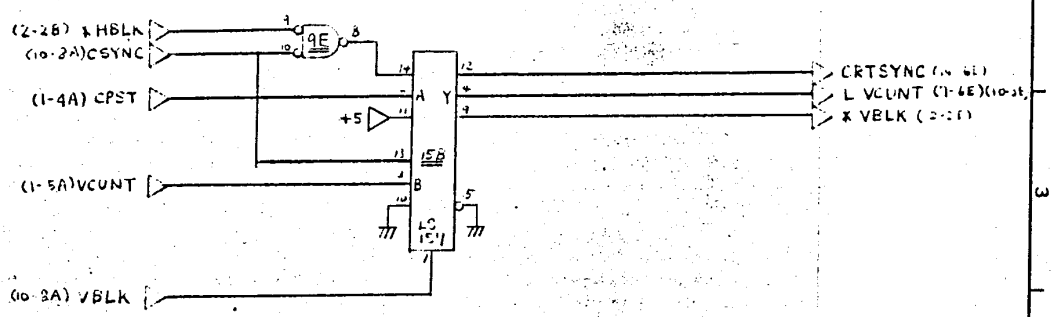

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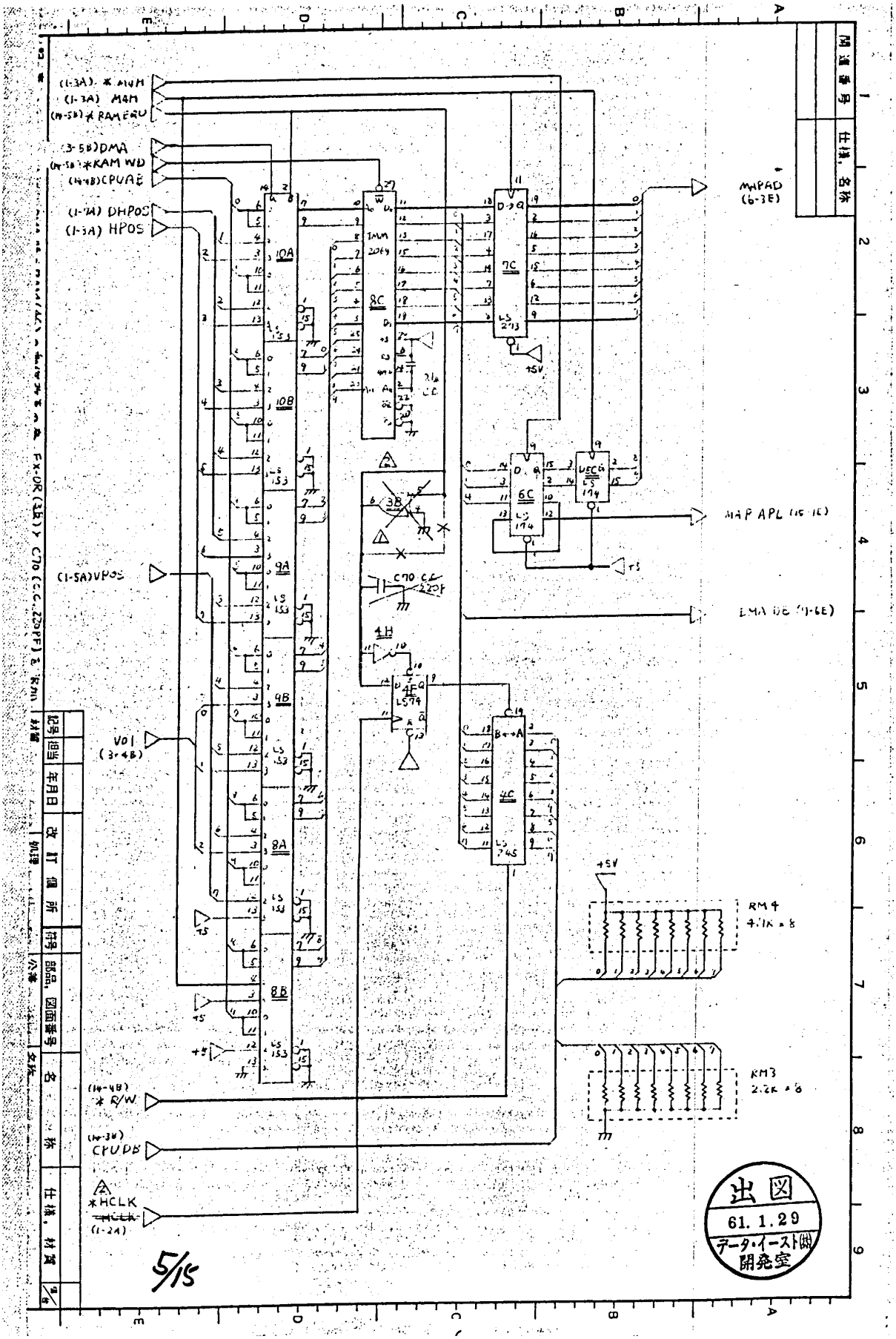
(1-3A) *MWM
(1-3A) MWM
(1-5B) *RAMERU
(3-5B) DMA
(1-5B) *RAM WD
(1-4B) CPUAB
(1-3A) DHPOS
(1-3A) HPOS
(1-5A) VPOS
VD1
(3-4B)
(1-4B) *R/W
(1-3B) CPUDB
*HCLK
(1-2A)
MAPAD (6-3E)
MAP APL (6-1E)
DMA DB (1-6E)
C70 CC 220P
RM4 4.7K × 8
RM3 2.2K × 8
+5V
出図
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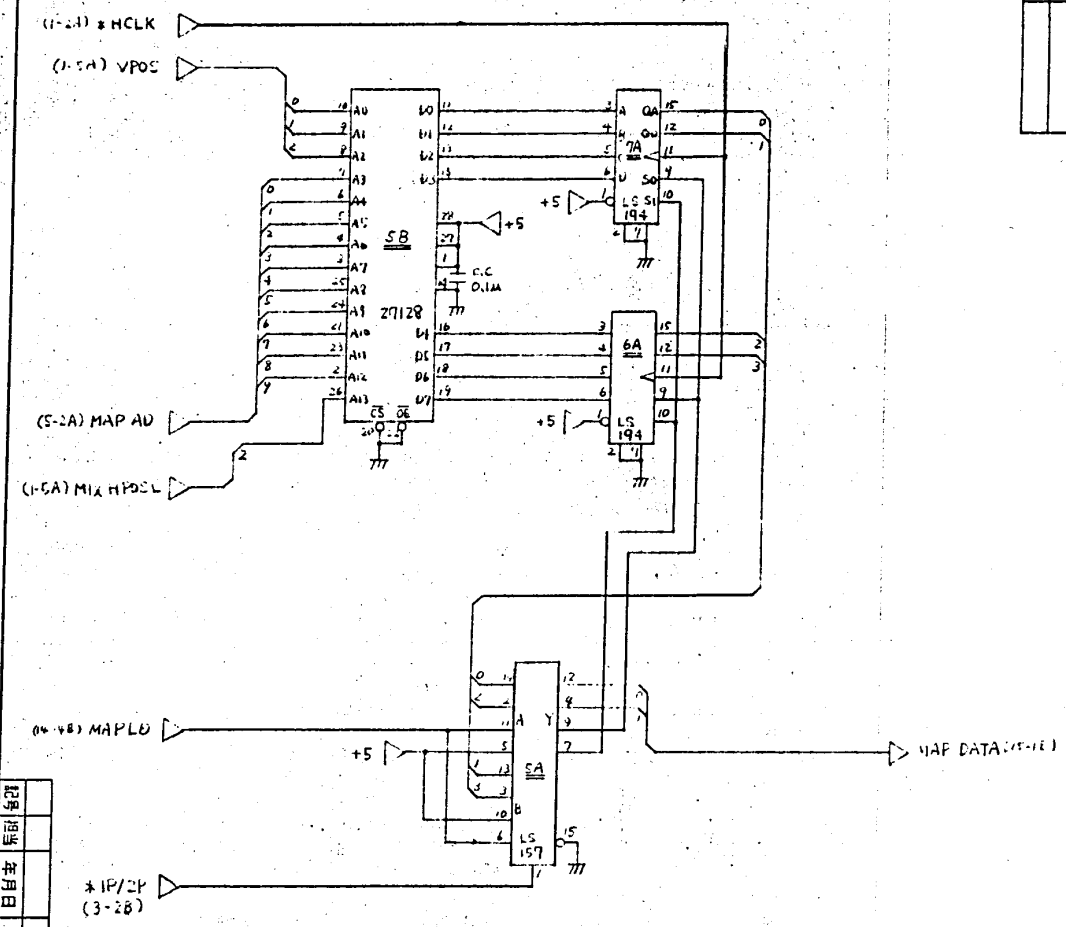

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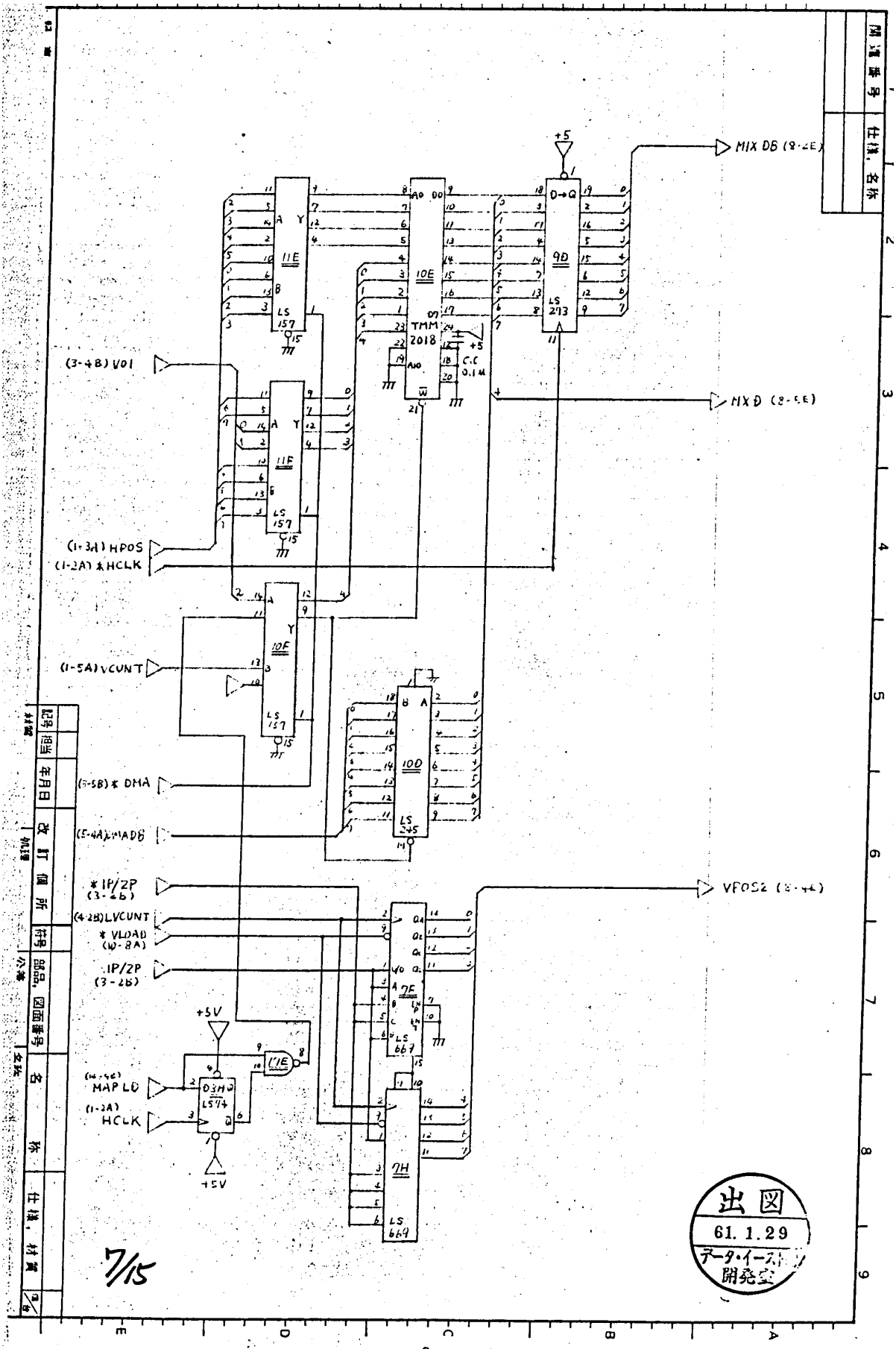
MIX DB (8-4E)
MIX D (8-5E)
VPOS2 (8-4E)
(3-4B) V01
(1-3A) HPOS
(1-2A) *HCLK
(1-5A) VCUNT
(5-5B) * DMA
(5-4A) *MADB
*IP/ZP (3-2B)
(4-2B) LVCUNT
* VLOAD (W-8A)
IP/ZP (3-2B)
(4-4E) MAP LD
(1-2A) HCLK
+5V
11E
10E
9D
11F
10F
10D
7E
7H
TMM 2018
LS 157
LS 273
LS 245
LS 667
LS 669
LS 174
C.C 0.1M
出図
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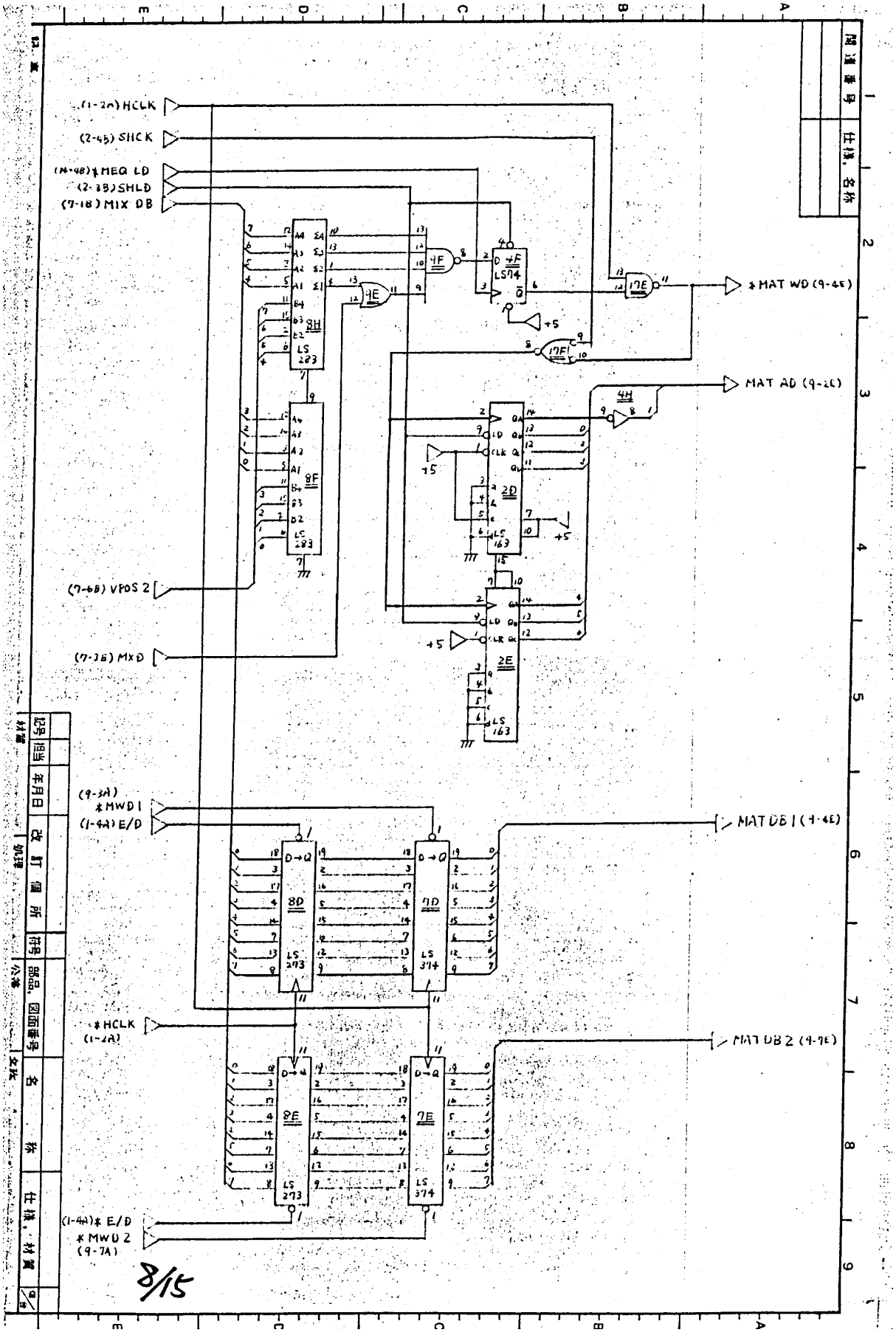
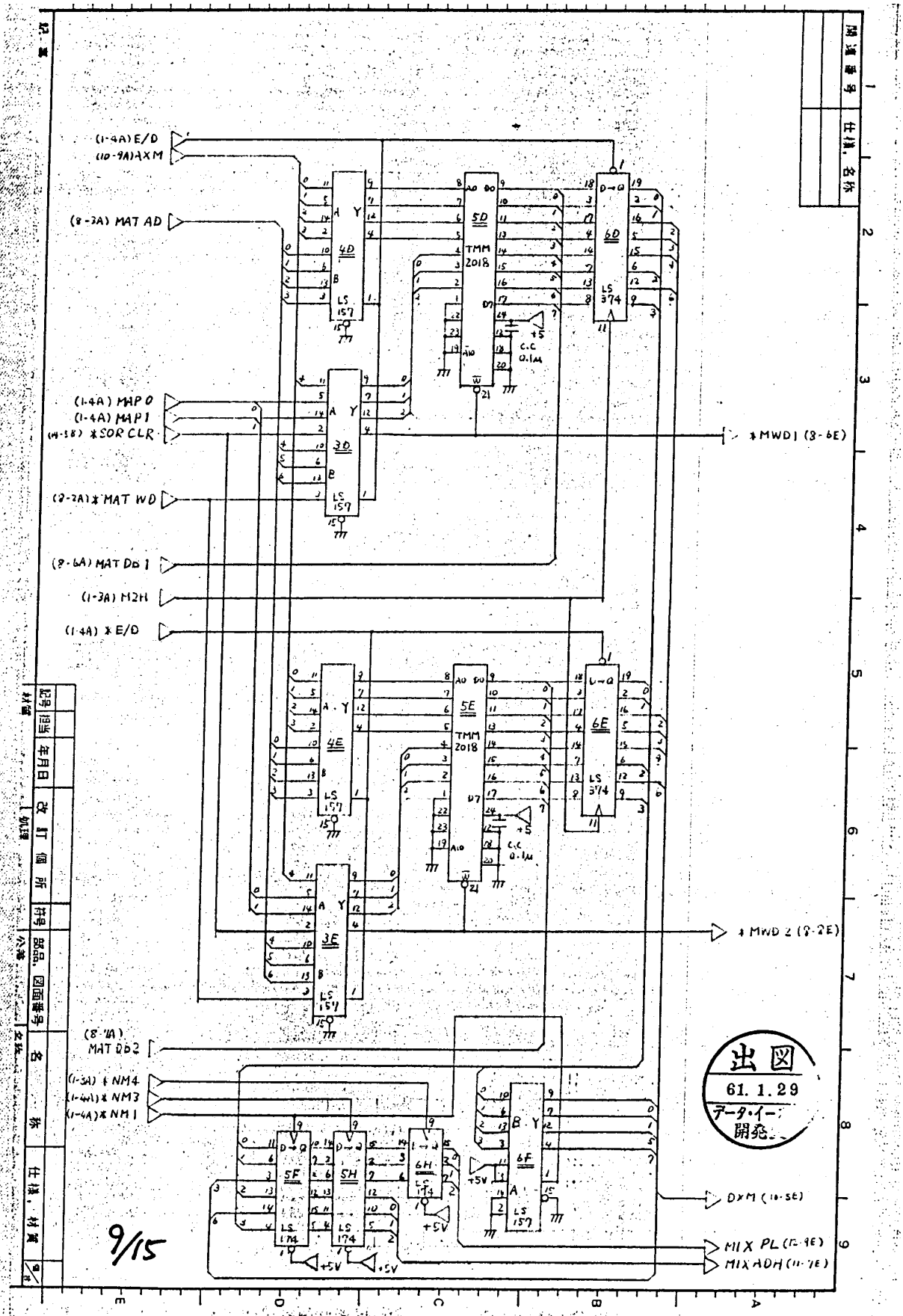


(1-2A) HCLK
(2-4B) SHCK
(14-4B) *MEQ LD
(2-3B) SHLD
(7-1B) MIX DB
*MAT WD (9-4E)
MAT AD (9-2E)
(7-6B) VPOS 2
(7-3B) MXD
(9-3A) *MWD1
(1-4A) E/D
MAT DB1 (9-4E)
*HCLK (1-2A)
MAT DB2 (9-7E)
(1-4A) *E/D
*MWD2 (9-7A)
8H
8F
4F
2D
2E
8D
7D
8E
7E
LS 283
LS 74
LS 163
LS 273
LS 374
+5
8/15


(1-4A) E/D
(10-9A) AXM
(8-3A) MAT AD
(1-4A) MAP 0
(1-4A) MAP 1
(14-5B) *SOR CLR
(8-2A) *MAT WD
(8-6A) MAT DB 1
(1-3A) M2H
(1-4A) *E/D
(8-1A) MAT DB 2
(1-3A) * NM4
(1-4A) * NM3
(1-4A) * NM 1
*MWD1 (8-6E)
*MWD 2 (8-2E)
DXM (10-5E)
MIX PL (12-9E)
MIX ADH (11-7E)
TMM 2018
LS 157
LS 374
LS 174
C.C 0.1M
+5V
出図
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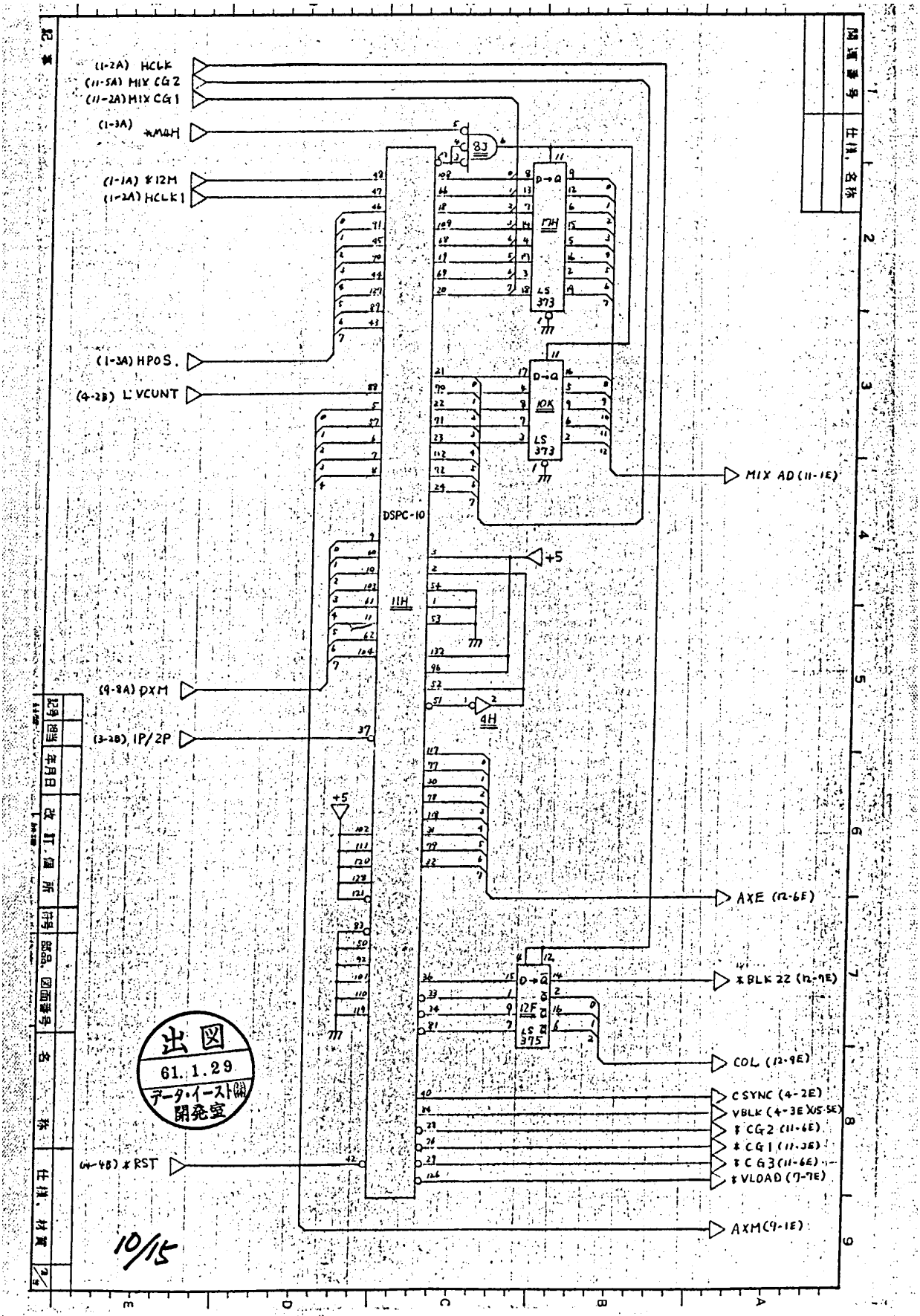
(1-2A) HCLK
(11-5A) MIX CG2
(11-2A) MIX CG1
(1-3A) *MWH
(1-1A) *12M
(1-2A) HCLK1
(1-3A) HPOS.
(4-2B) LVCUNT
DSPC-10
(9-8A) DXM
(3-2B) IP/2P
(4-4B) *RST
+5
MIX AD (11-1E)
AXE (12-6E)
*BLK 2Z (12-9E)
COL (12-9E)
CSYNC (4-2E)
VBLK (4-3E)(5-5E)
*CG2 (11-6E)
*CG1 (11-3E)
*CG3 (11-6E)
*VLOAD (9-7E)
AXM (9-1E)
出図
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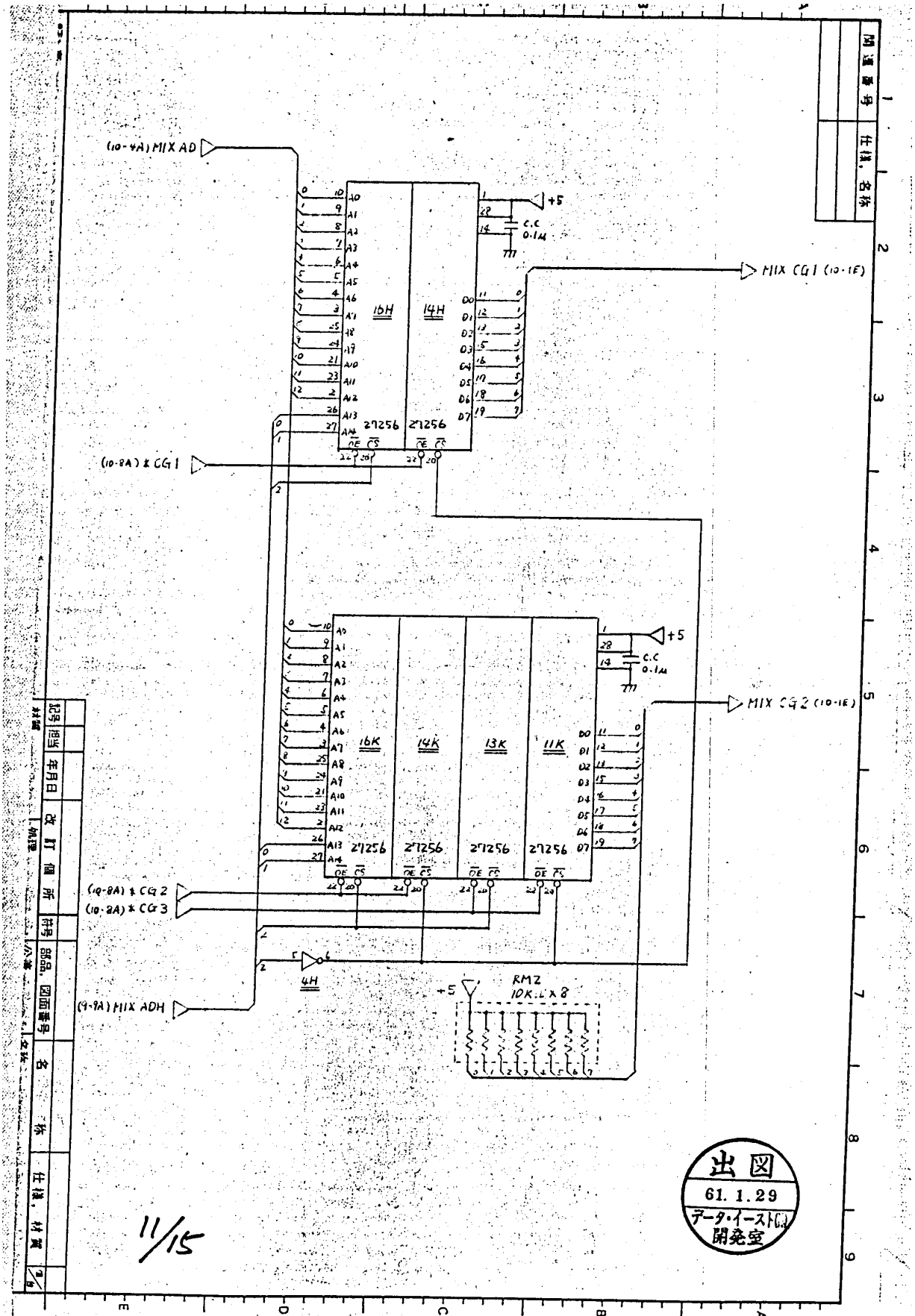
(10-4A) MIX AD
16H
14H
27256
+5
C.C
0.1μ
MIX CG1 (10-1E)
(10-8A) & CG1
16K
14K
13K
11K
MIX CG2 (10-1E)
(10-8A) & CG2
(10-2A) & CG3
4H
(9-9A) MIX ADH
RM2
10K.Ω×8
出図
61. 1. 29
データ・イースト㈱
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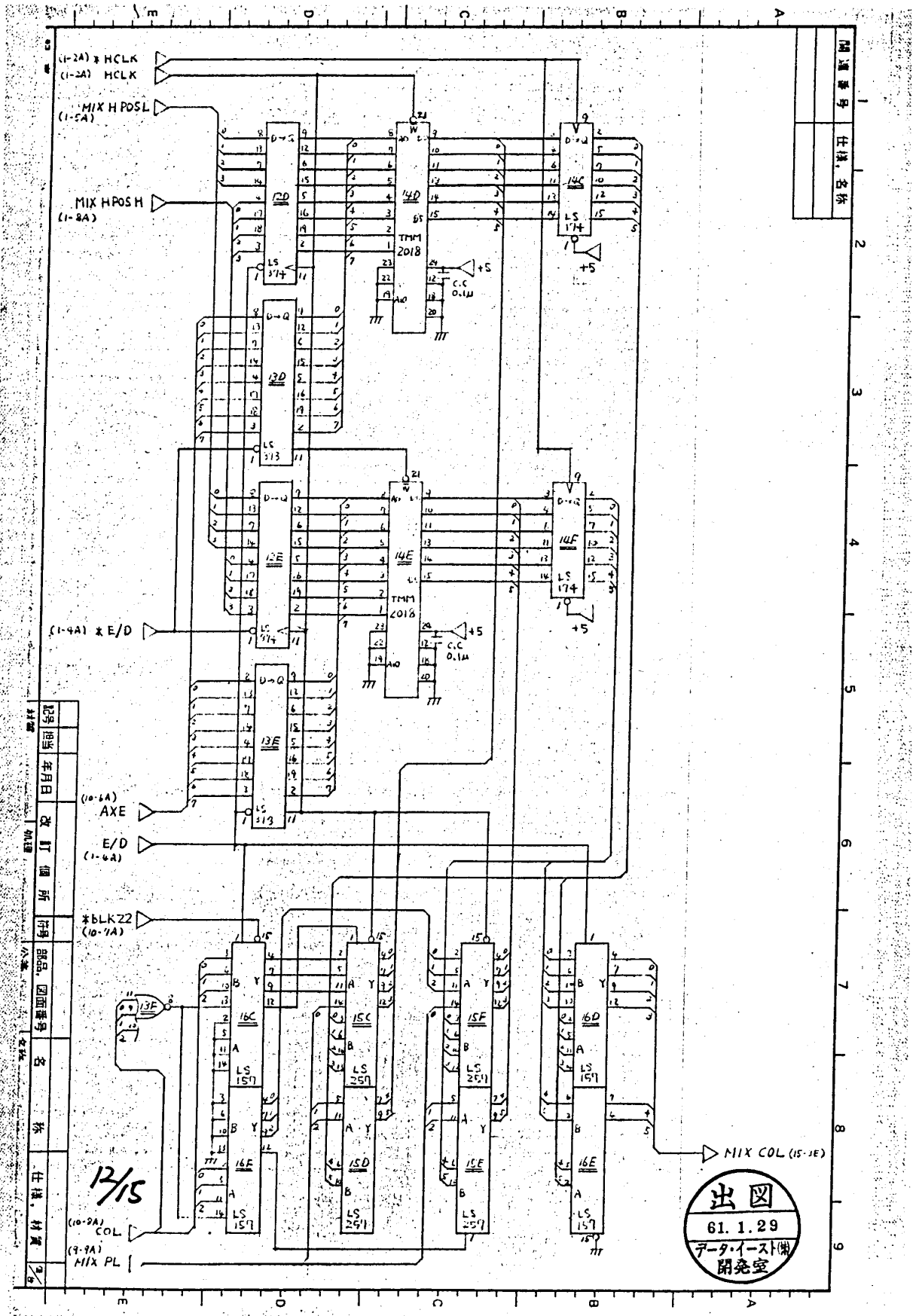
11/15


(1-2A) * HCLK
(1-2A) HCLK
MIX H POSL
(1-5A)
MIX H POS H
(1-8A)
(1-9A) * E/D
(10-6A)
AXE
E/D
(1-6A)
*BLKZ2
(10-7A)
(10-9A)
COL
(9-9A)
MIX PL
MIX COL (15-1E)
TMM 2018
LS 374
LS 373
LS 157
LS 251
C.C 0.1μ
+5
出図
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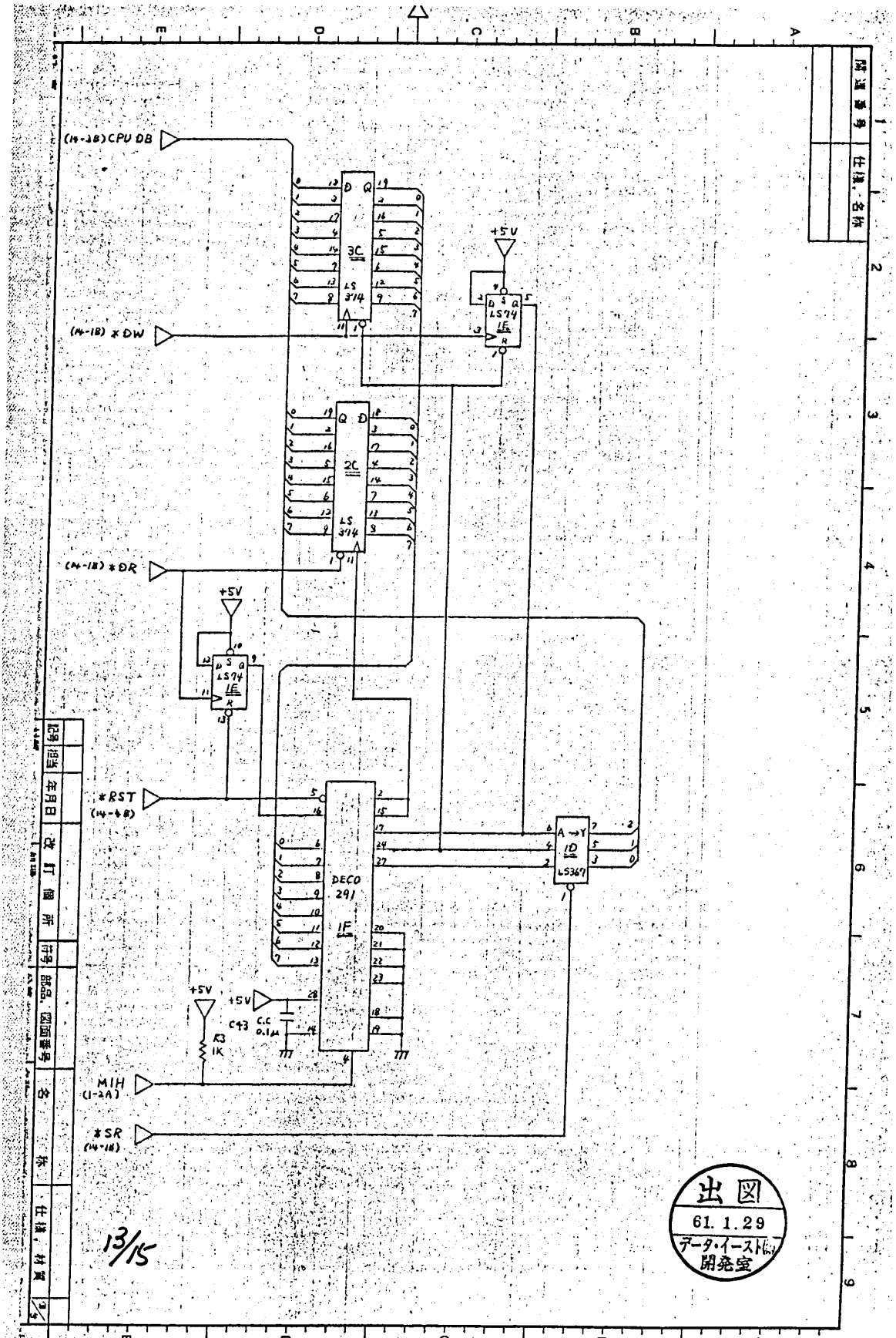
(14-28) CPU DB
(14-18) *DW
(14-18) *DR
*RST
(14-6 8)
MIH
(1-2A)
*SR
(14-18)
+5V
LS374
LS74
LS367
DECO 291
C43 C.C 0.1μM
R3 1K
出図
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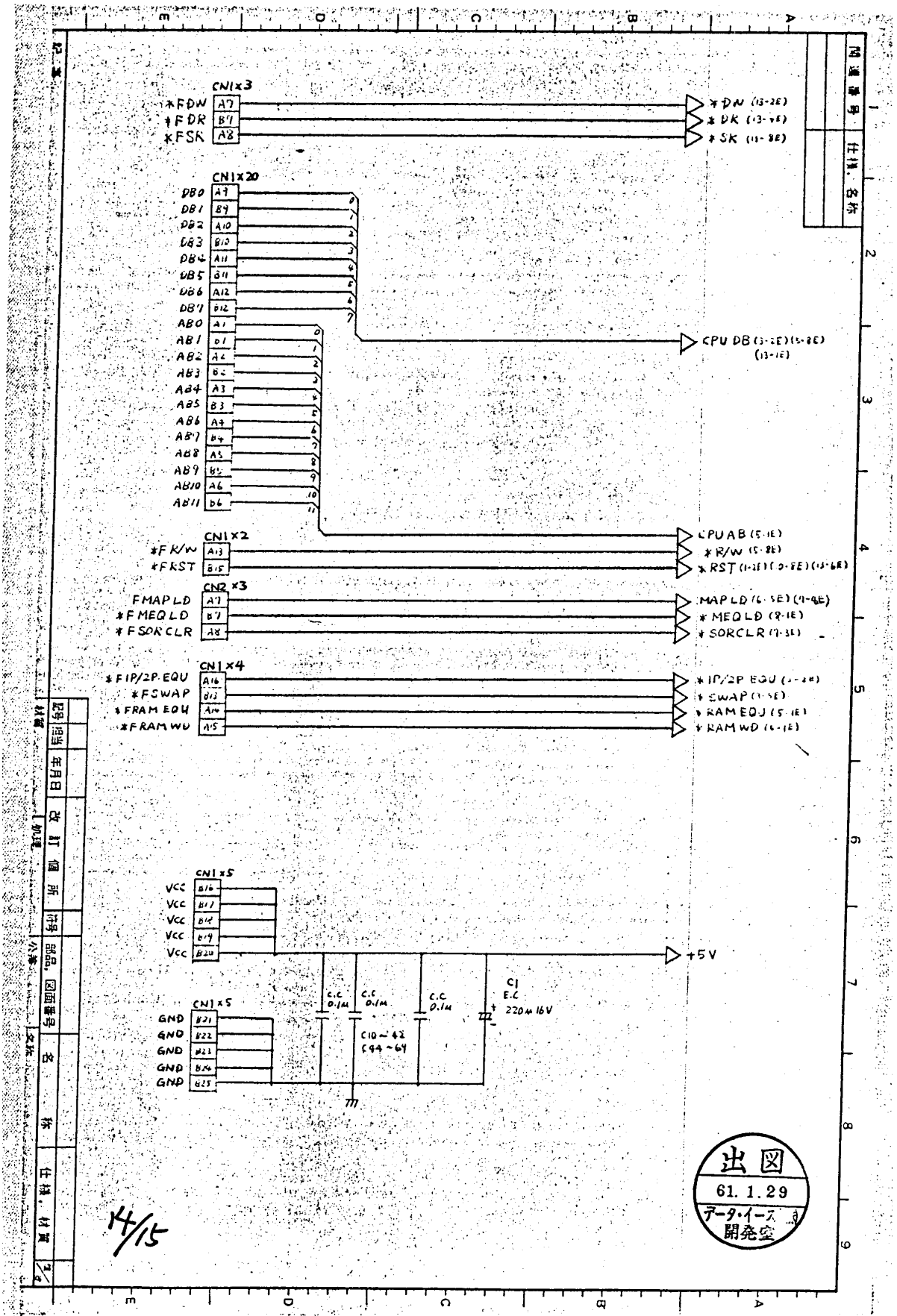
CN1×3
*FDW A7
*FDR B7
*FSK A8
*DW (13-2E)
*DR (13-4E)
*SK (11-8E)
CN1×20
DB0 A9
DB1 B9
DB2 A10
DB3 B10
DB4 A11
DB5 B11
DB6 A12
DB7 B12
ABO A1
AB1 B1
AB2 A2
AB3 B2
AB4 A3
AB5 B3
AB6 A4
AB7 B4
AB8 A5
AB9 B5
AB10 A6
AB11 B6
CPU DB (3-2E)(5-8E)
(13-1E)
CPU AB (5-1E)
CN1×2
*FR/W A13
*FRST B15
*R/W (5-8E)
*RST (1-2E)(3-5E)(13-6E)
CN2×3
FMAPLD A7
*FMEQLD B7
*FSORCLR A8
MAPLD (6-5E)(9-4E)
*MEQLD (8-1E)
*SORCLR (9-3E)
CN1×4
*FIP/2P-EQU A16
*FSWAP B13
*FRAM EQU A14
*FRAM WD A15
*IP/2P EQU (1-4E)
*SWAP (1-5E)
*RAM EQU (5-1E)
*RAM WD (6-1E)
CN1×5
VCC B16
VCC B17
VCC B18
VCC B19
VCC B20
+5V
CN1×5
GND B21
GND B22
GND B23
GND B24
GND B25
C.C 0.1M
C.C 0.1M
C10~62
C94~64
C.C 0.1M
C1
E.C
220M 16V
出図
61. 1. 29
データ・イース
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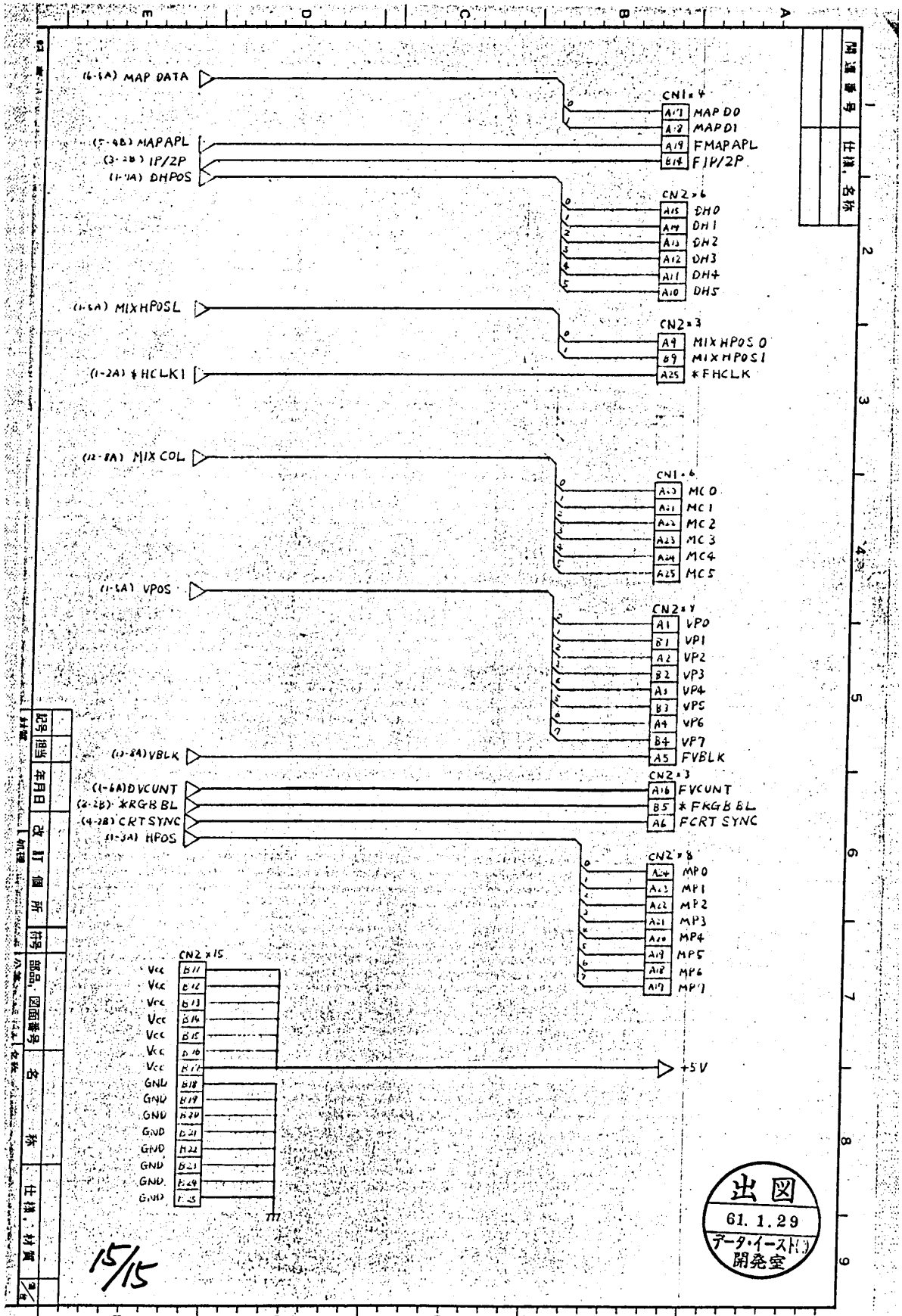
(6-5A) MAP DATA
CN1×4
A17 MAP D0
A18 MAP D1
(5-4B) MAPAPL
A19 FMAPAPL
(3-2B) IP/2P
B14 FIP/2P
(1-1A) DHPOS
CN2×6
A15 DH0
A14 DH1
A13 DH2
A12 DH3
A11 DH4
A10 DH5
(1-6A) MIXHPOSL
CN2×3
A9 MIXHPOS 0
B9 MIXHPOS 1
(1-2A) *HCLK1
A25 *FHCLK
(12-8A) MIX COL
CN1×6
A20 MC 0
A21 MC 1
A22 MC 2
A23 MC 3
A24 MC 4
A25 MC 5
(1-5A) VPOS
CN2×8
A1 VP0
B1 VP1
A2 VP2
B2 VP3
A3 VP4
B3 VP5
A4 VP6
B4 VP7
(13-8A) VBLK
A5 FVBLK
(1-6A) DVCUNT
(2-2B) *RGBBL
(4-2B) CRTSYNC
(1-3A) HPOS
CN2×3
A16 FVCUNT
B5 *FRGBBL
A6 FCRTSYNC
CN2×8
A24 MP0
A23 MP1
A22 MP2
A21 MP3
A20 MP4
A19 MP5
A18 MP6
A17 MP7
CN2×15
Vcc B11
Vcc B12
Vcc B13
Vcc B14
Vcc B15
Vcc B16
Vcc A11
GND B18
GND B19
GND A20
GND B21
GND A22
GND B23
GND B24
GND A25
+5V
出図
61. 1. 29
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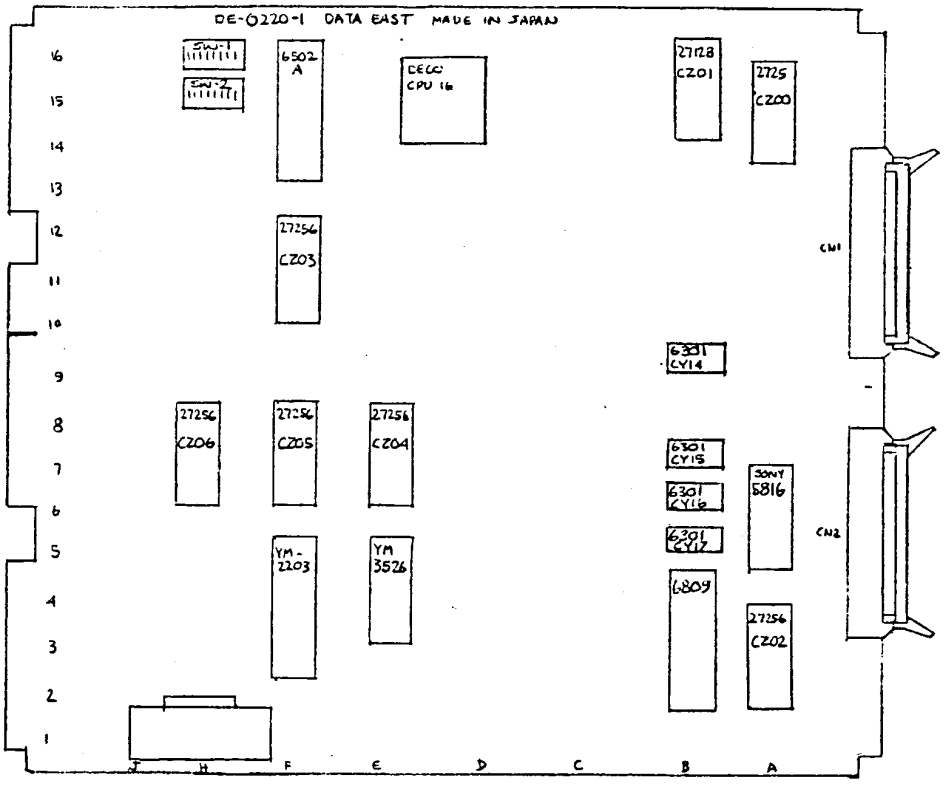
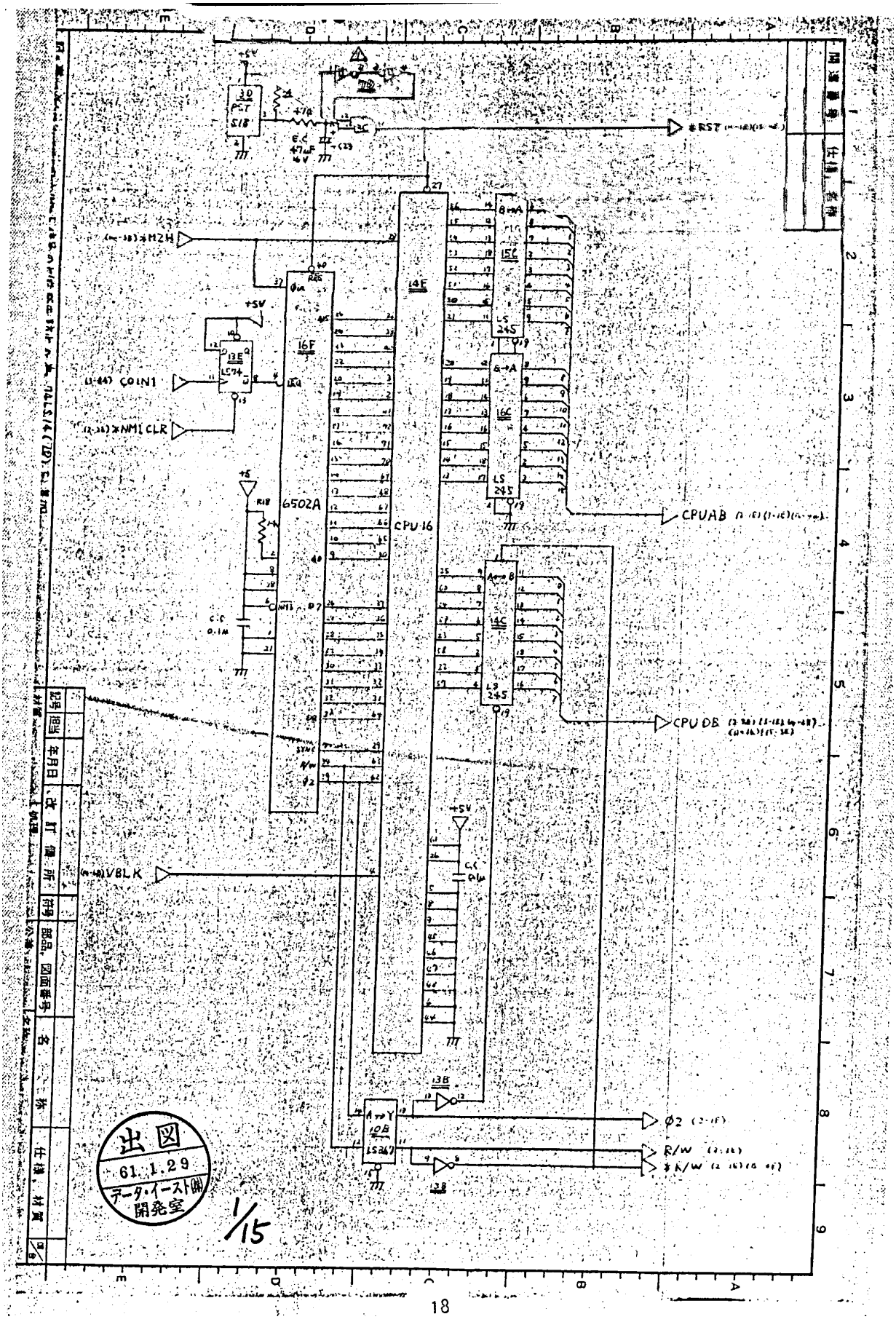
2. EXPRESS RAIDER TOP PCB, DE-0221-1 (520-0068-~)





6502A
CPU-16
14E
16F
15C
16C
14C
13E
LS74
LS 245
LS367
10B
13B
30
PST
S18
+5V
*RST
*M2H
COIN1
*NMI CLR
CPUAB
CPU DB
VBLK
Ø2
R/W
*R/W
出図
61.1.29
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開発室
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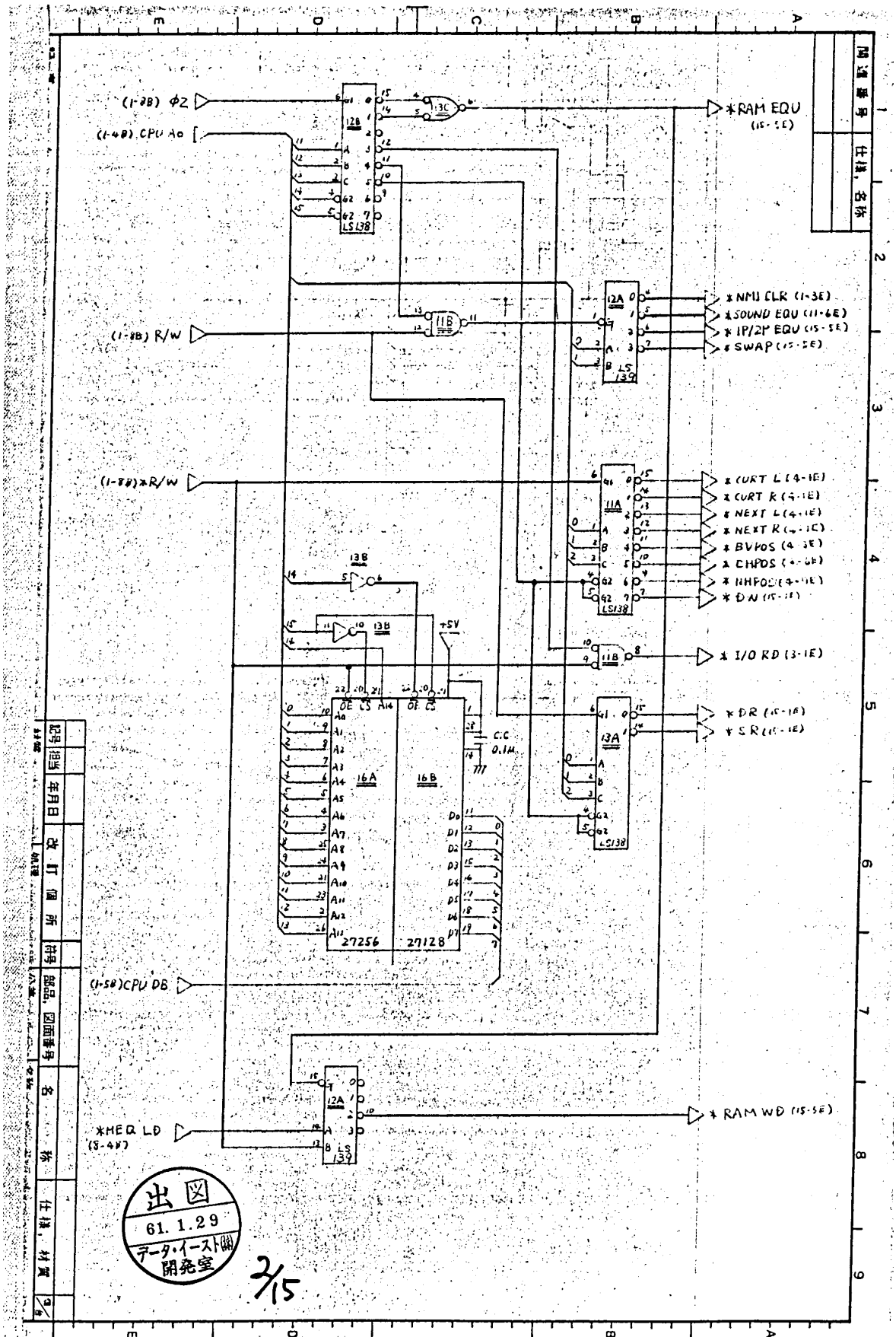

出図
61. 1. 29
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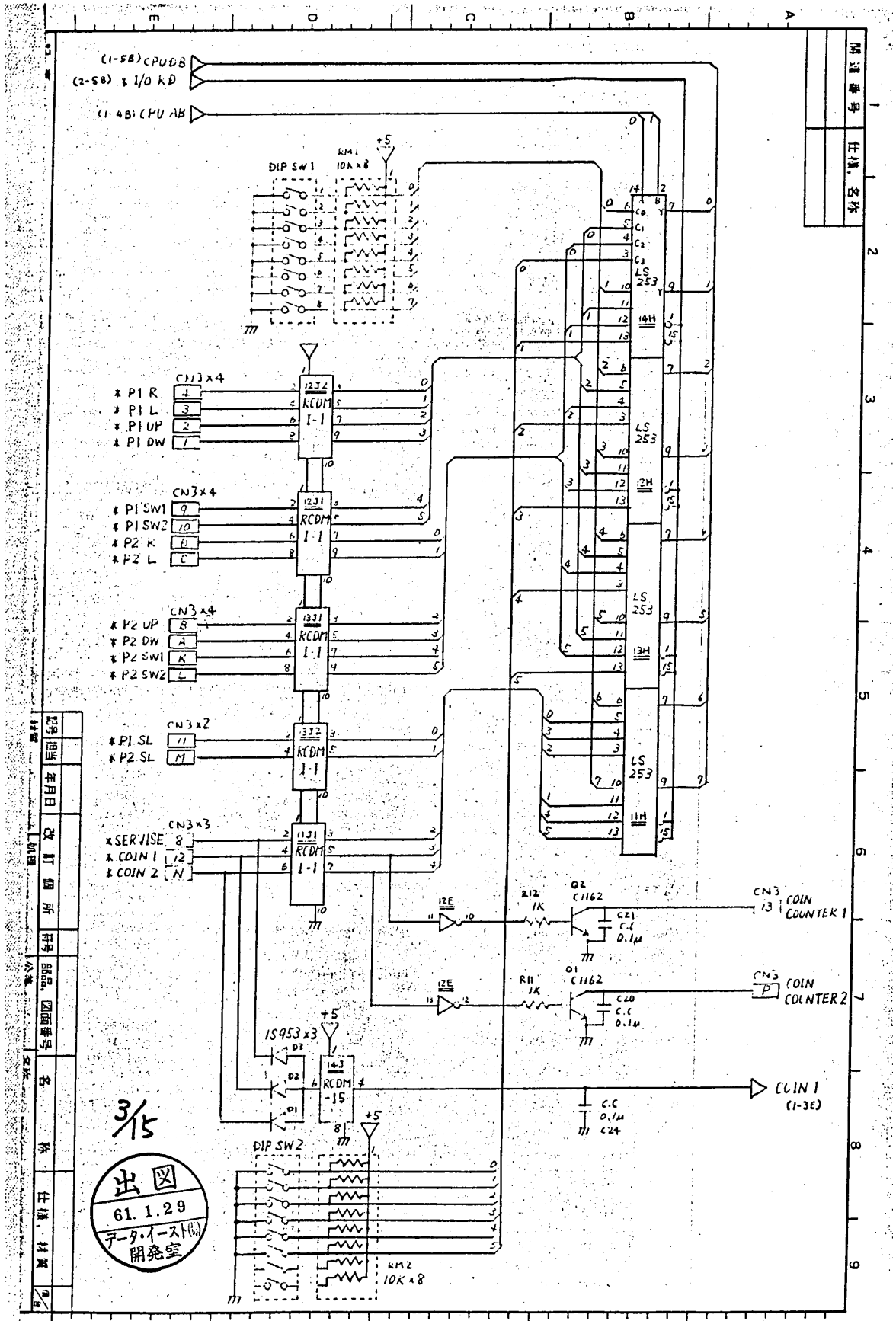
(1-58) CPU DB
(2-58) ※ I/O RD
(1-48) CPU AB
DIP SW1
RM1 10K×8
+5
CN3×4
※ P1 R
※ P1 L
※ P1 UP
※ P1 DW
※ P1 SW1
※ P1 SW2
※ P2 R
※ P2 L
※ P2 UP
※ P2 DW
※ P2 SW1
※ P2 SW2
CN3×2
※ P1 SL
※ P2 SL
CN3×3
※ SERVISE
※ COIN 1
※ COIN 2
KCDM 1-1
KCDM -15
LS 253
IS953×3
Q2 C1162
Q1 C1162
R12 1K
R11 1K
C21 C.C 0.1μ
C20 C.C 0.1μ
C24 C.C 0.1μ
CN3 13 COIN COUNTER 1
CN3 P COIN COUNTER 2
COIN 1 (1-3E)
DIP SW2
RM2 10K×8
3/15
出図
61. 1. 29
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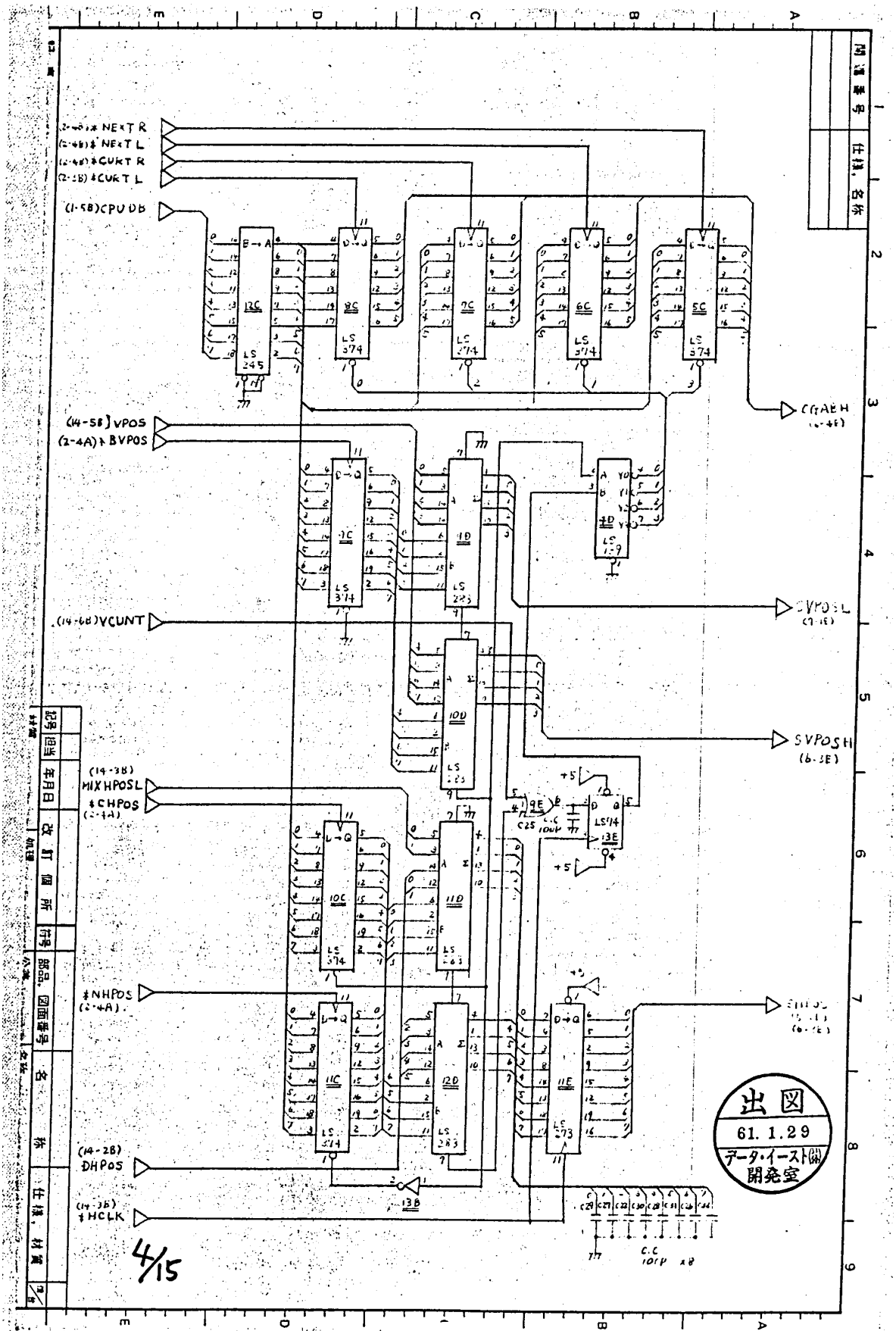
開発室



(2-4B)*NEXT R
(2-4B)*NEXT L
(2-4B)*CURT R
(2-3B)*CURT L
(1-5B)CPU DB
(14-5B)VPOS
(2-4A)*BVPOS
(14-6B)VCUNT
(14-3B)
MIXHPOSL
*CHPOS
(2-4A)
*NHPOS
(2-4A)
(14-2B)
DHPOS
(14-3B)
*HCLK
CGABH
SVPOSL
SVPOSH
(6-3E)
出図
61. 1.29
データ・イースト(株)
開発室
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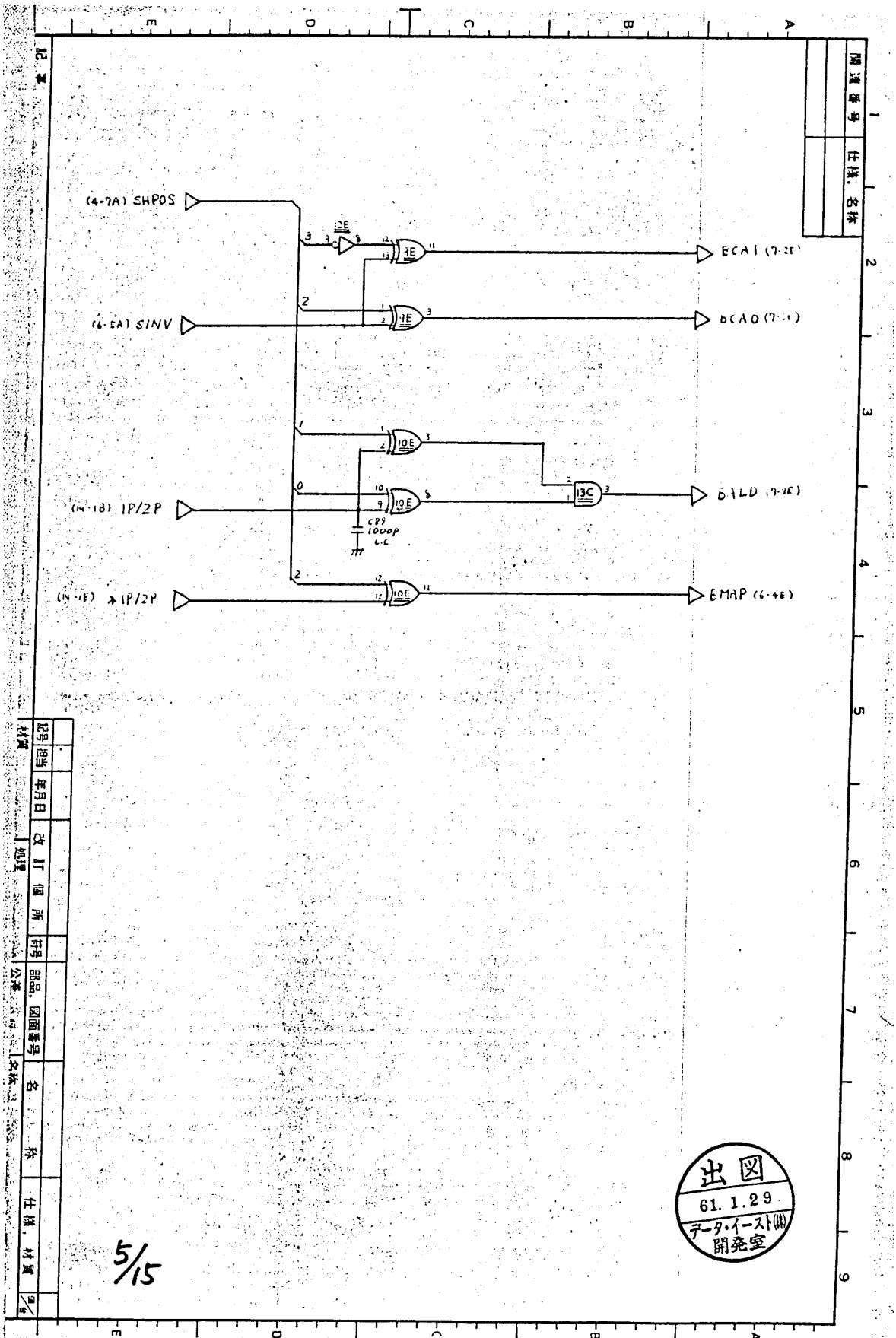

出図
61. 1. 29
データ・イースト㈱
開発室

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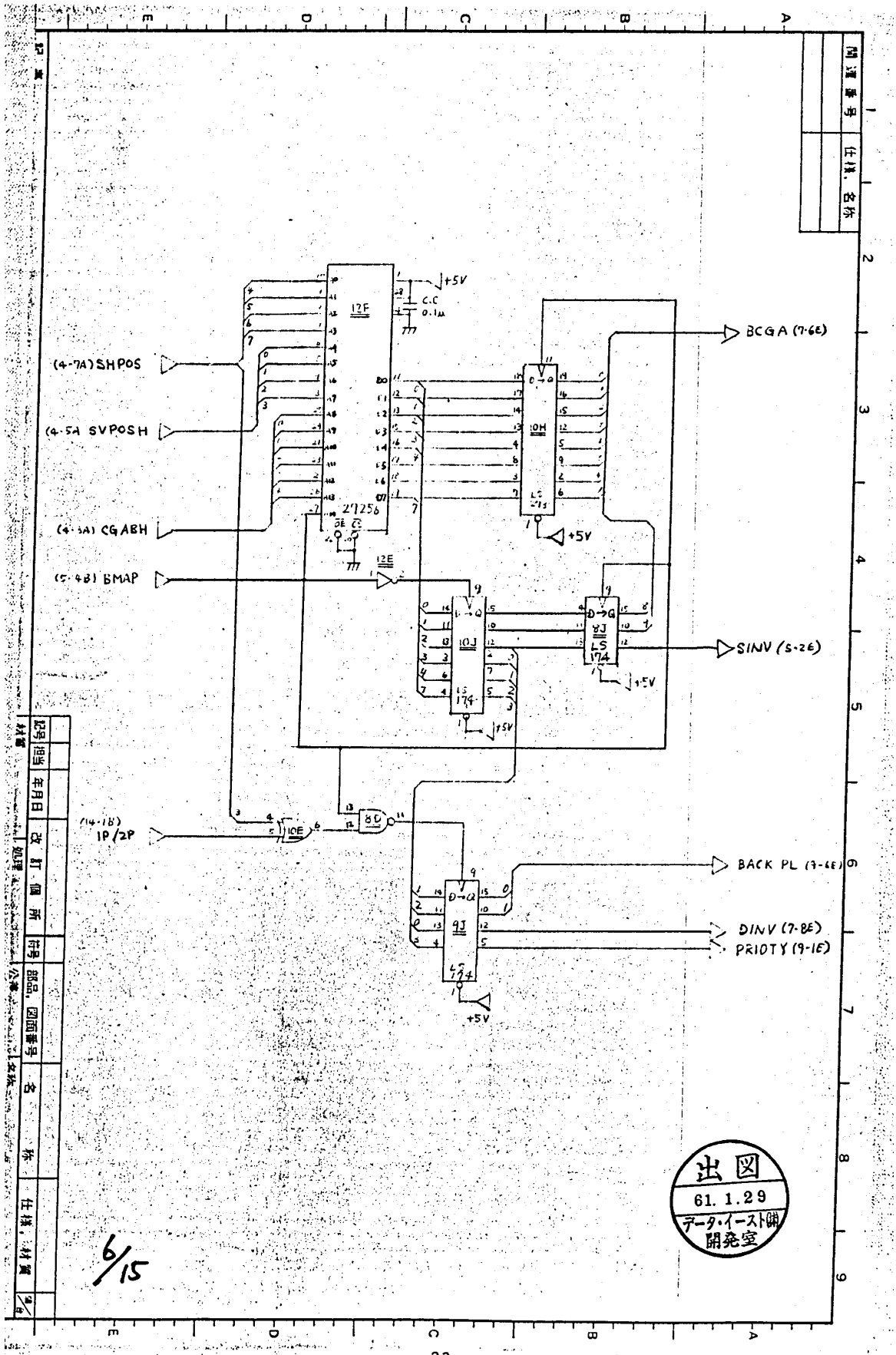

(4-7A) SHPOS
(4-5A SVPOSH
(4-3A) CGABH
(5-4B) BMAP
(14-1B) 1P/2P
12F
27256
12E
10H
10J
8J
9J
10E
8D
+5V
C.C 0.1μ
BCGA (7-6E)
SINV (5-2E)
BACK PL (7-6E)
DINV (7-8E)
PRIOTY (9-1E)
出図
61. 1.29
データ・イースト㈱
開発室
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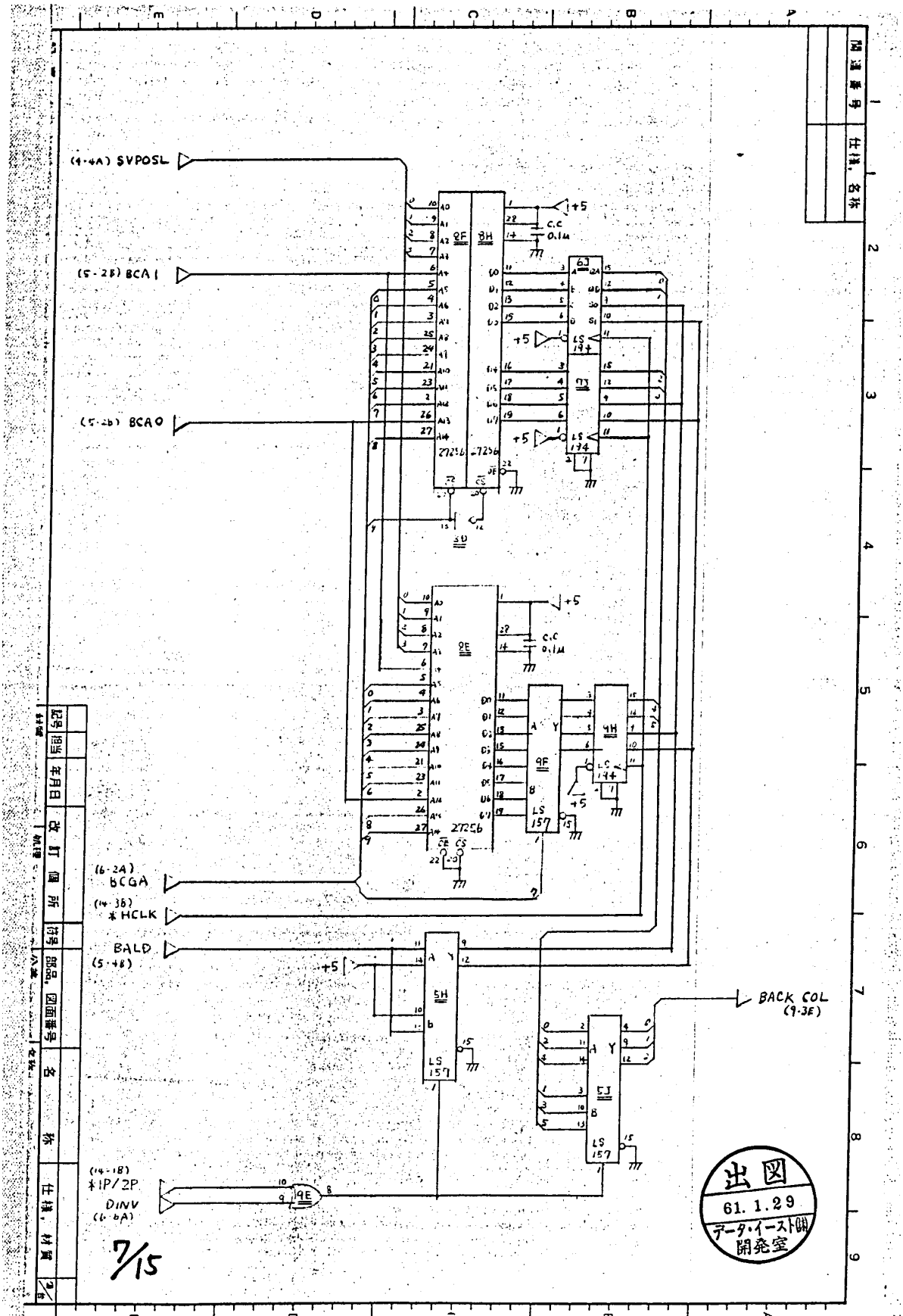
(4-4A) SVPOSL
(5-2B) BCA1
(5-2B) BCA0
(6-2A) BCGA
(14-3B) *HCLK
BALD (5-4B)
(14-1B) *1P/2P
DINV (6-6A)
BACK COL (9-3E)
+5
C.C 0.1μ
27256
LS 157
LS 194
出図
61. 1. 29
データ・イースト(株)
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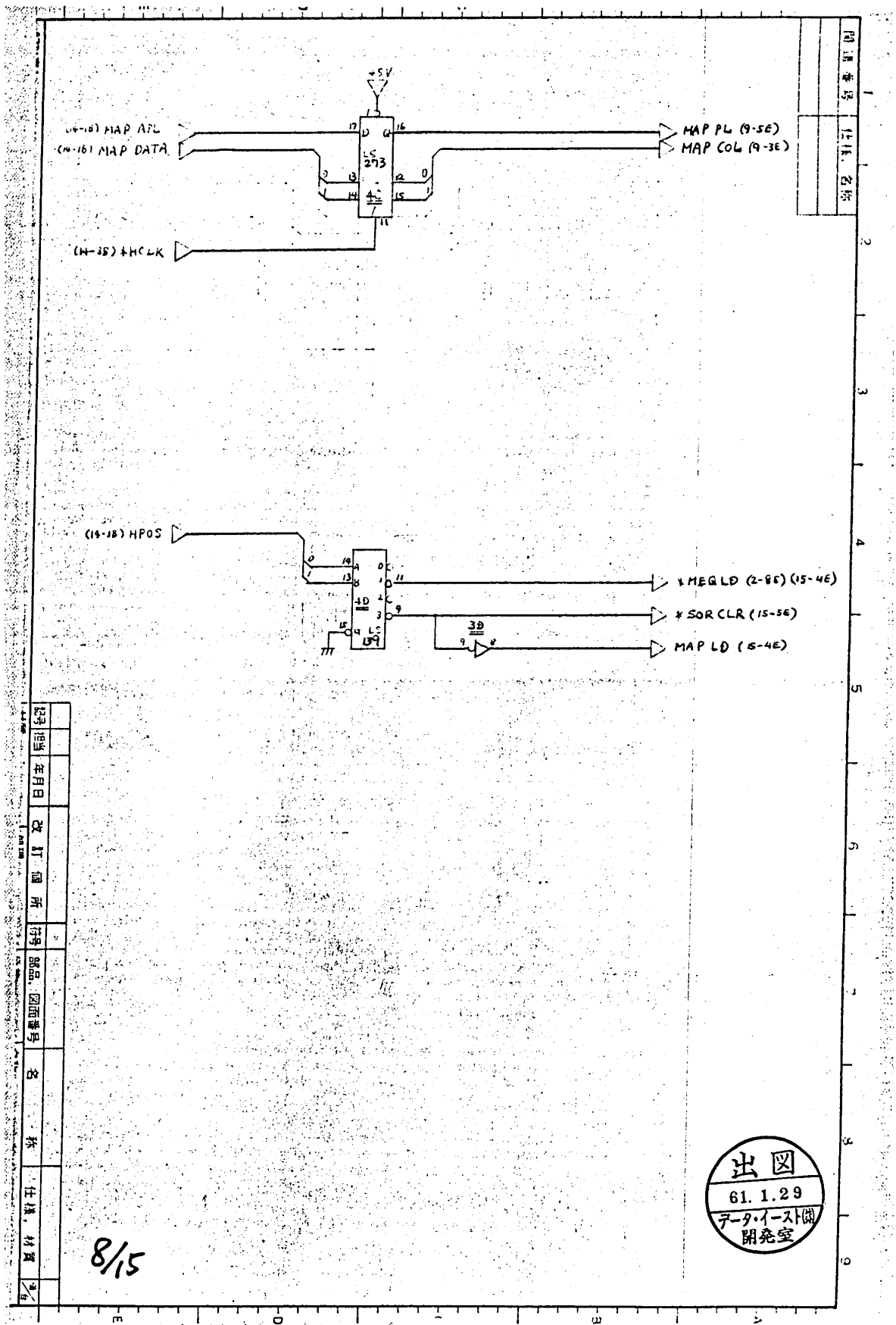
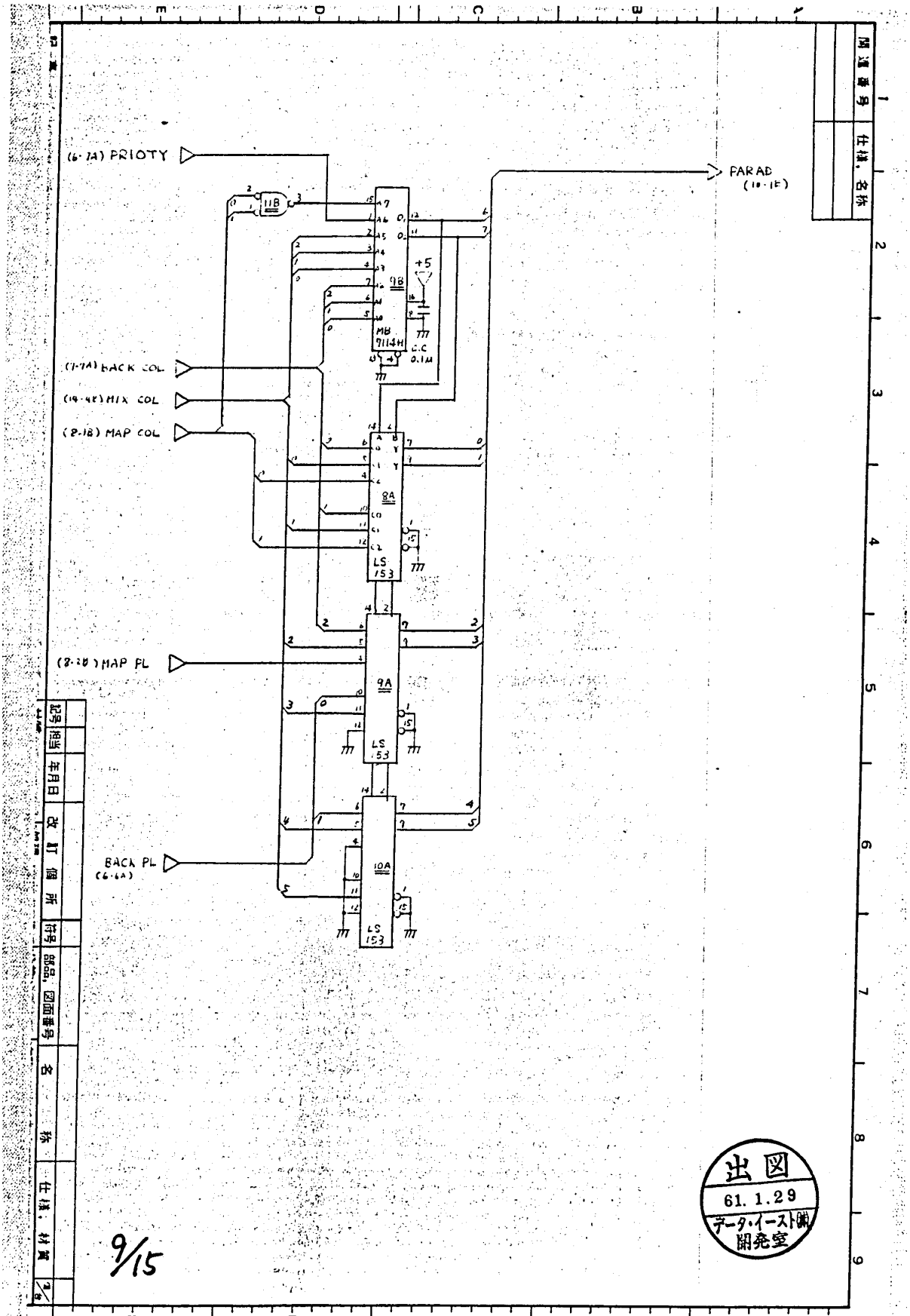
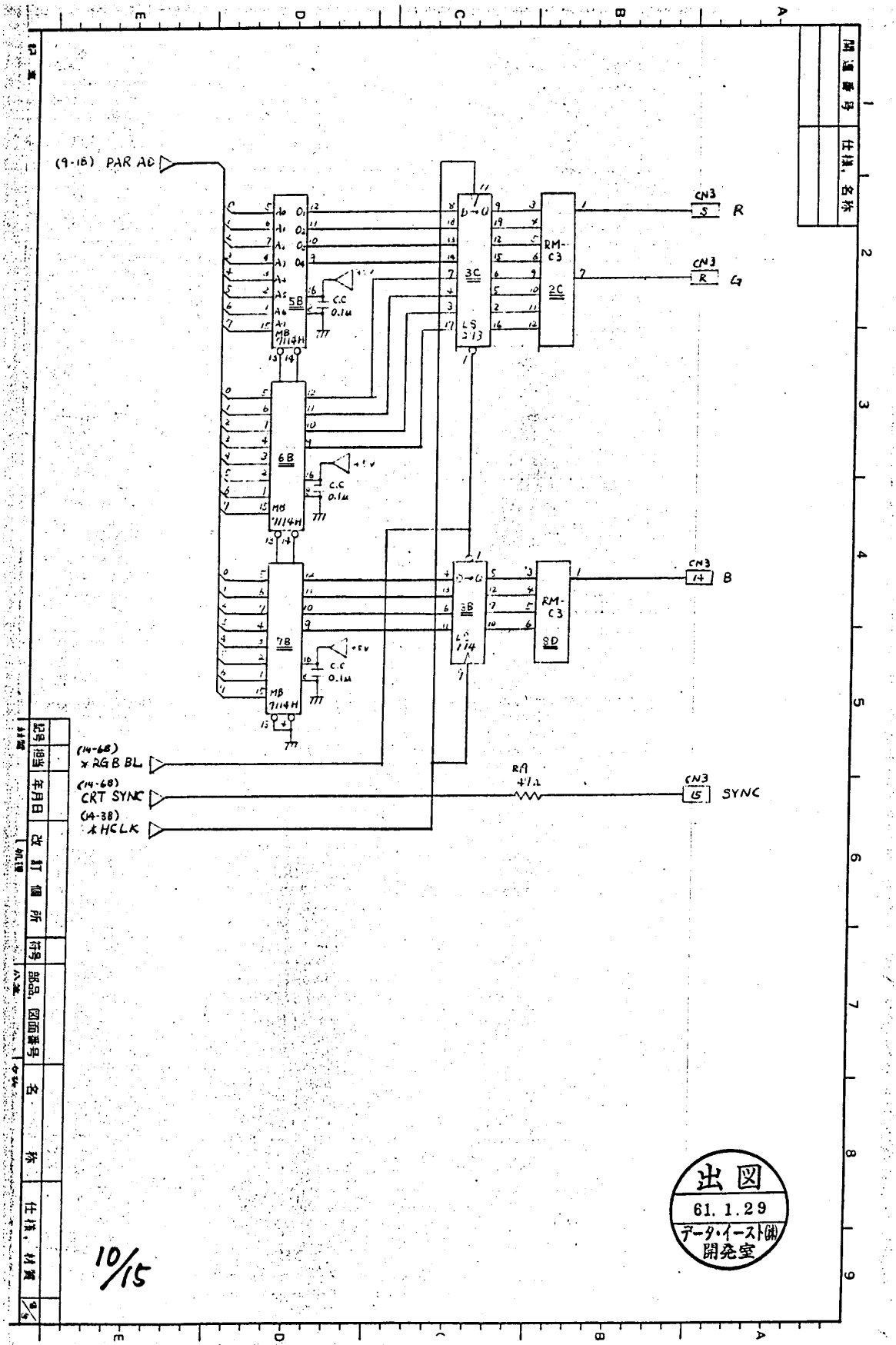
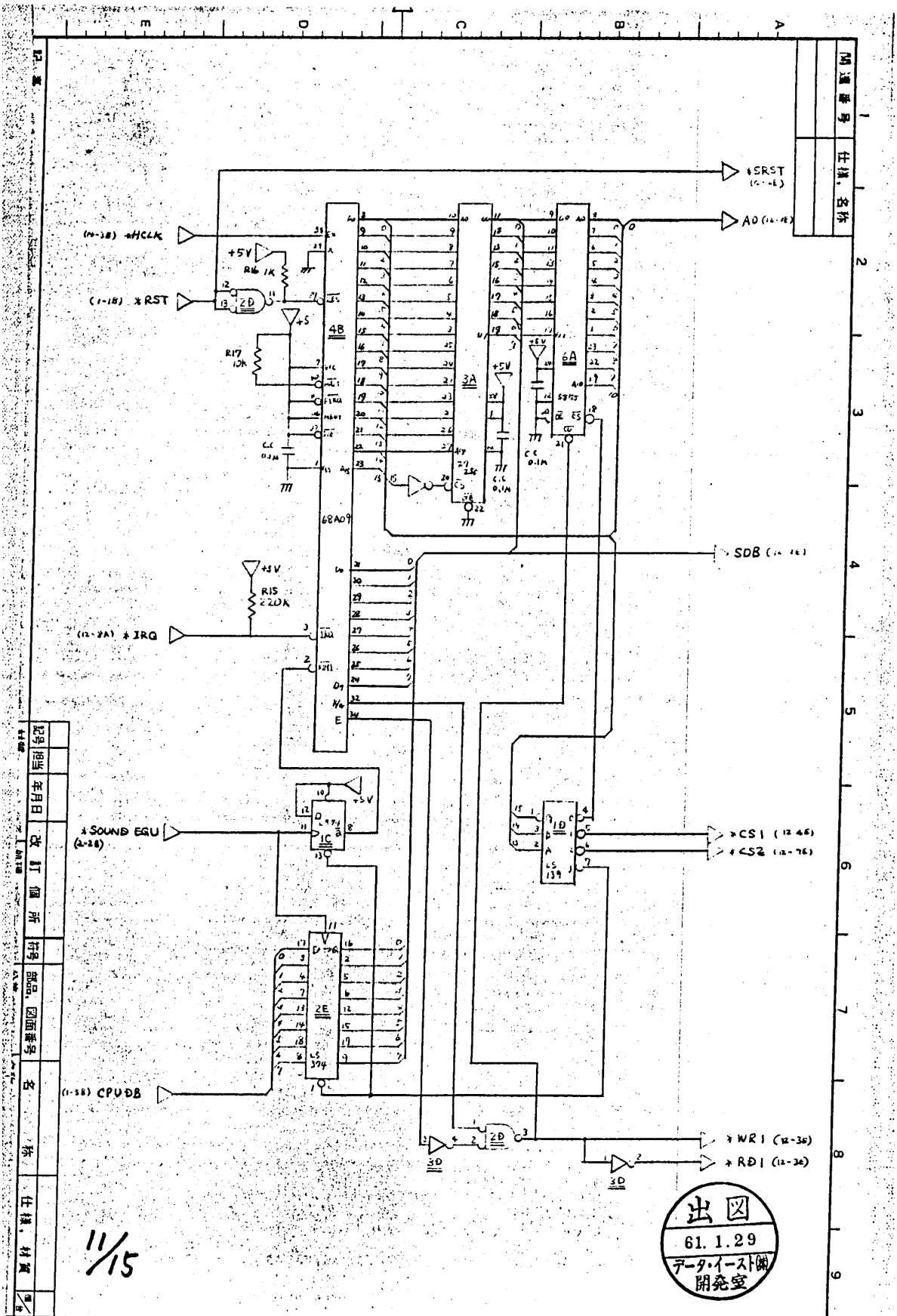


出図
61. 1. 29
データ・イースト㈱
開発室


(6·7A) PRIOTY
PARAD
(10·1E)
11B
9B
+5
MB
7114H
0.1M
(1·7A) BACK COL
(10·4E) MIX COL
(8·1B) MAP COL
8A
LS
153
(8·2B) MAP PL
9A
LS
53
BACK PL
(6·6A)
10A
LS
153
9/15
出図
61. 1. 29
データ・イースト㈱
開発室



出図
61. 1. 29
データ・イースト㈱
開発室



*SRST
AD
*HCLK
*RST
+5V
R16 1K
R17 10K
4B
3A
6A
68A09
SDB
R15 220K
*IRQ
*SOUND EGU
1C
1D
*CS1
*CS2
2E
CPUDB
*WR1
*RD1
3D
2D
出図
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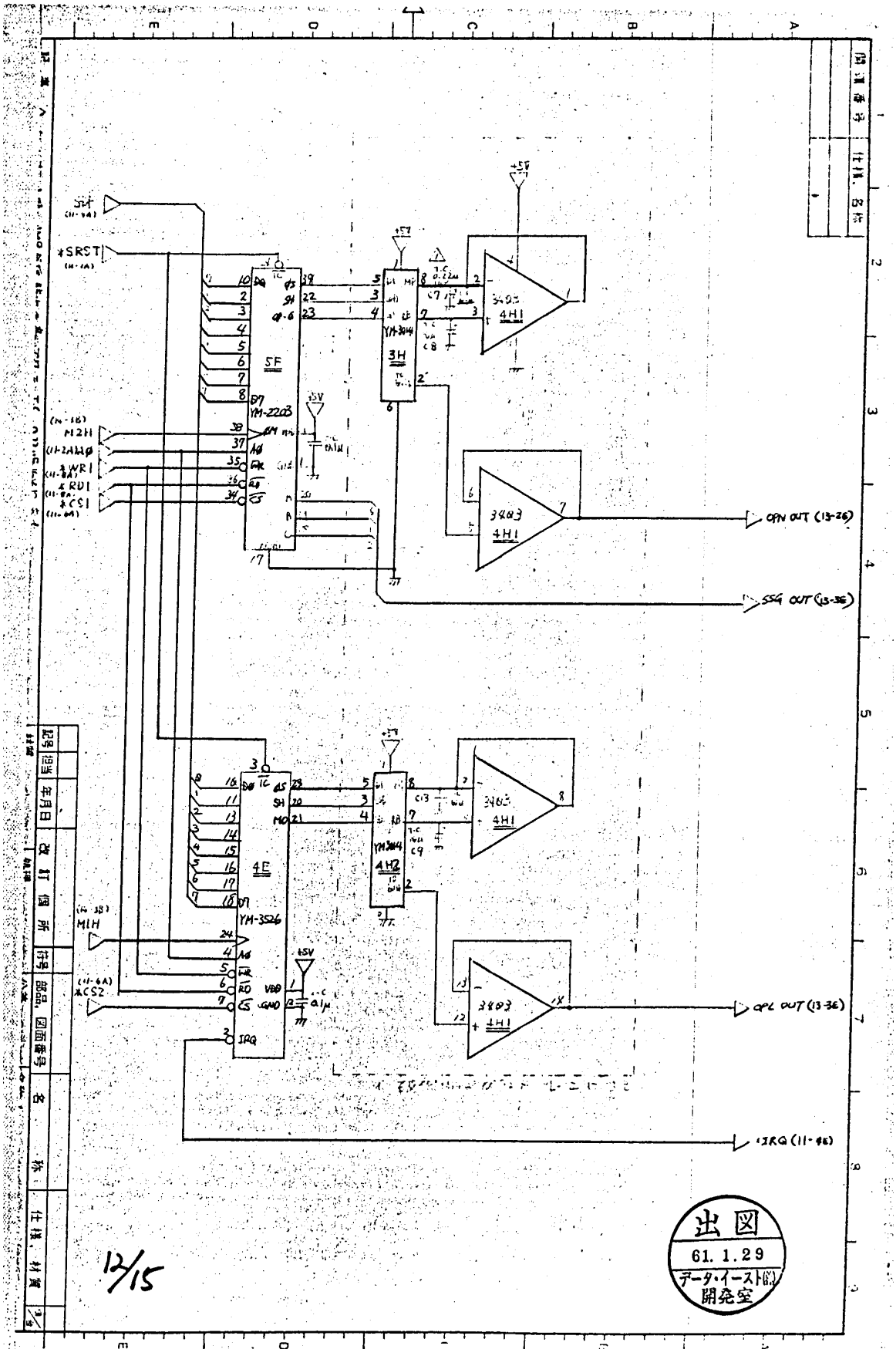
*SRST
YM-2203
YM-3014
YM-3526
YM3014
OPN OUT (13-26)
SSG OUT (13-36)
OPL OUT (13-36)
IRQ (11-46)
出図
61. 1. 29
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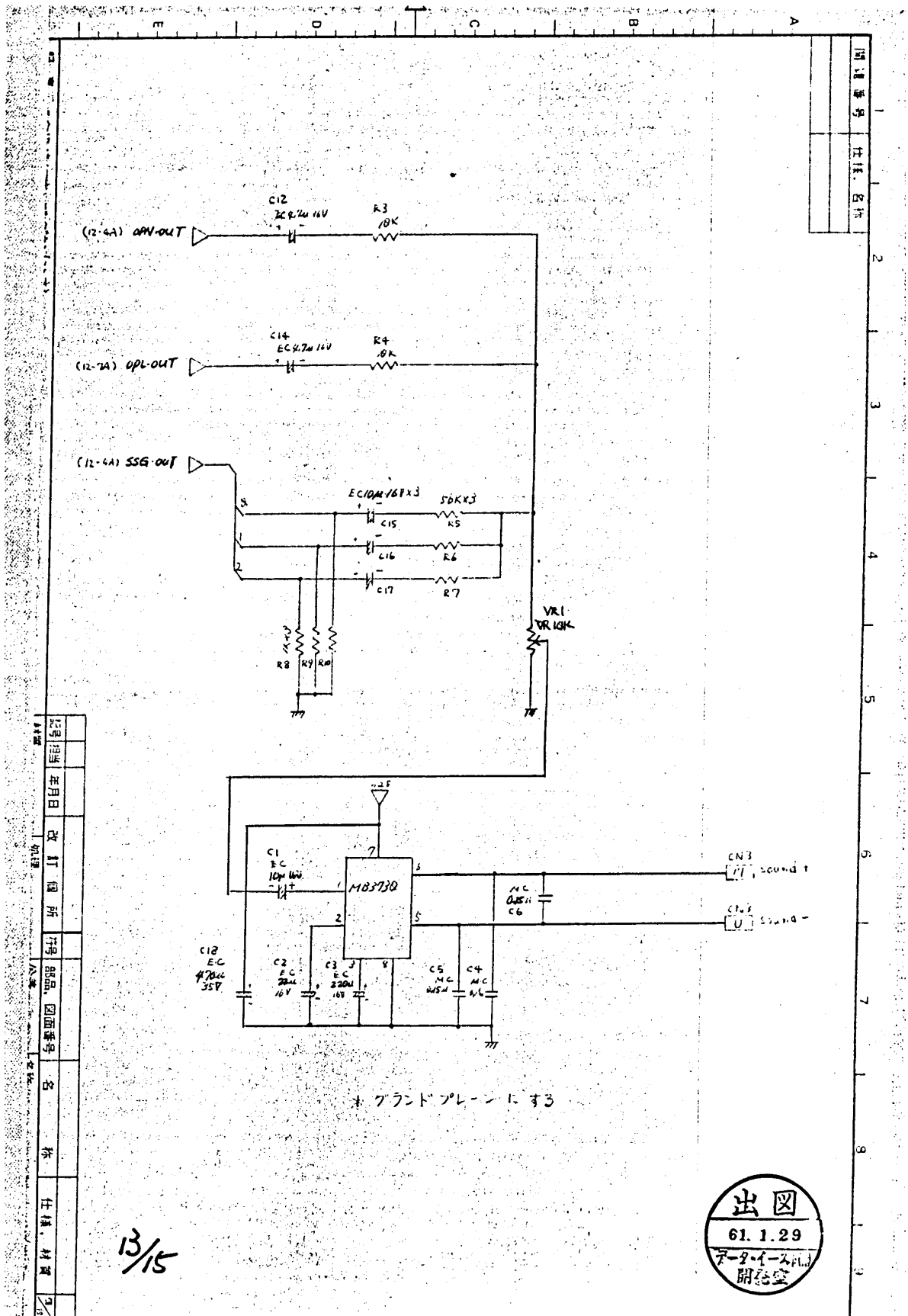
(12-4A) OPN-OUT
C12
R3
10K
(12-7A) OPL-OUT
C14
R4
10K
(12-4A) SSG-OUT
EC10μ 16V×3
56K×3
C15
R5
C16
R6
C17
R7
VR1
R8
R9
R10
C1
EC
10μ 16V
MB3730
C18
EC
470μ
35V
C2
EC
22μ
16V
C3
EC
220μ
16V
C5
MC
0.15μ
C4
MC
0.6
MC
0.15μ
C6
CN3
sound +
sound −
* グランドプレーンにする
出図
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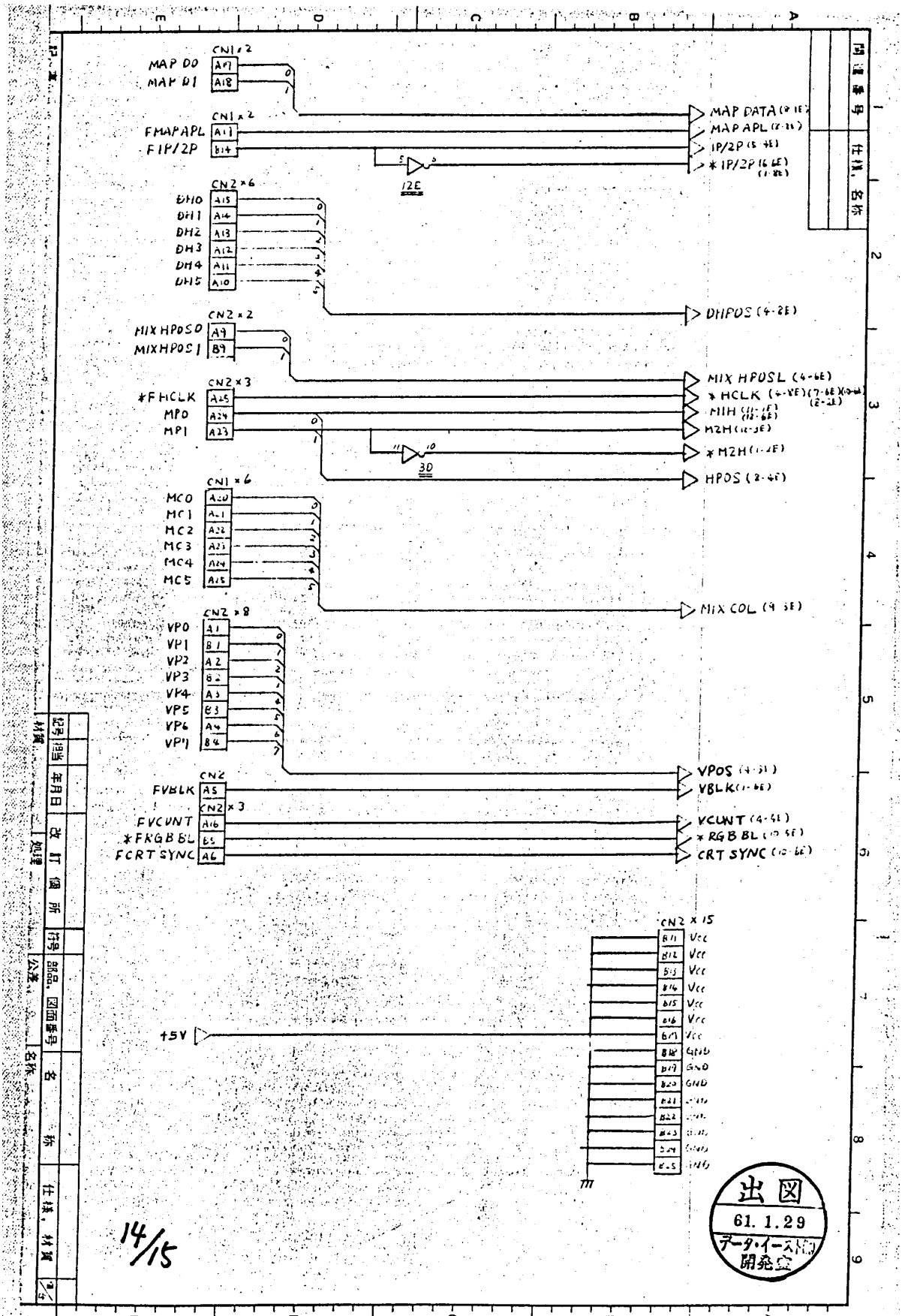
MAP D0
MAP D1
CN1×2
A17
A18
MAP DATA
MAP APL
FMAPAPL
F1P/2P
CN1×2
A11
B14
1P/2P
*1P/2P
12E
CN2×6
DH0
DH1
DH2
DH3
DH4
DH5
A15
A14
A13
A12
A11
A10
DHPOS
CN2×2
MIXHPOS0
MIXHPOS1
A9
B9
MIX HPOSL
CN2×3
*FHCLK
MP0
MP1
A25
A24
A23
*HCLK
MIH
M2H
*M2H
3D
HPOS
CN1×6
MC0
MC1
MC2
MC3
MC4
MC5
A20
A21
A22
A23
A24
A25
MIX COL
CN2×8
VP0
VP1
VP2
VP3
VP4
VP5
VP6
VP7
A1
B1
A2
B2
A3
B3
A4
B4
VPOS
VBLK
CN2
A5
CN2×3
FVBLK
FVCUNT
*FRGBBL
FCRTSYNC
A16
B5
A6
VCUNT
*RGB BL
CRT SYNC
CN2×15
+5V
Vcc
GND
14/15
出図
61. 1. 29
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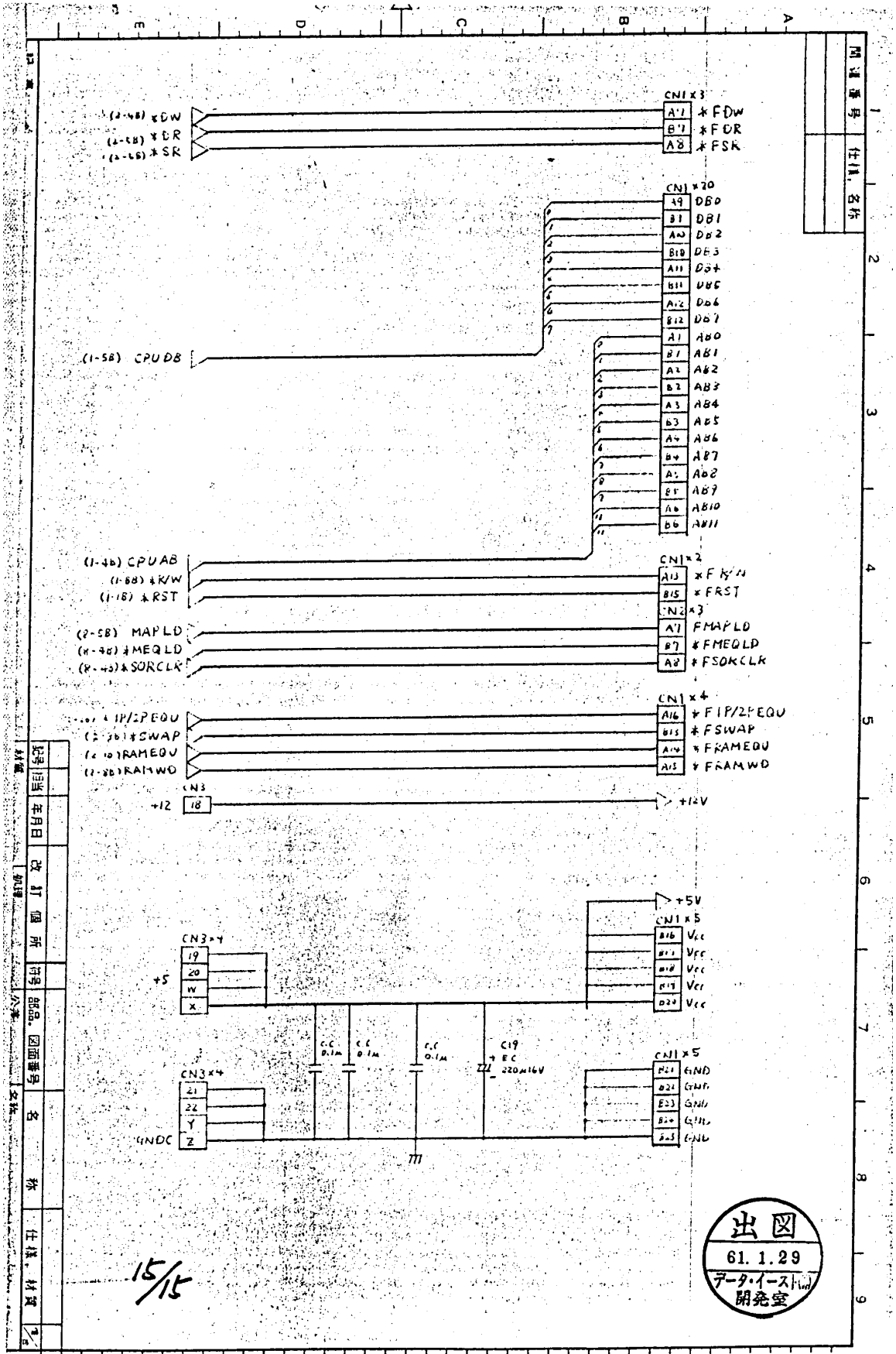

CN1×3
A7 *FDW
B7 *FDR
A8 *FSR
(2-4B) *DW
(2-5B) *DR
(2-6B) *SR
CN1×20
A9 DB0
B1 DB1
A10 DB2
B10 DB3
A11 DB4
B11 DB5
A12 DB6
B12 DB7
A1 AB0
B1 AB1
A2 AB2
B2 AB3
A3 AB4
B3 AB5
A4 AB6
B4 AB7
A5 AB8
B5 AB9
A6 AB10
B6 AB11
(1-5B) CPUDB
(1-4B) CPUAB
(1-8B) *R/W
(1-1B) *RST
CN1×2
A13 *FR/W
B15 *FRST
CN2×3
A7 FMAPLD
B7 *FMEQLD
A8 *FSORCLK
(2-5B) MAPLD
(8-4B) *MEQLD
(8-4B) *SORCLK
CN1×4
A16 *F1P/2PEQU
B13 *FSWAP
A14 *FRAMEQU
A15 *FRAMWD
(2-3B) *SWAP
(2-1B) RAMEQU
(2-8B) RAMWD
CN3
+12 18
+12V
+5V
CN1×5
B16 Vcc
B17 Vcc
B18 Vcc
B19 Vcc
B20 Vcc
CN3×4
19
20
W
X
+5
C.C 0.1μ
C.C 0.1μ
C.C 0.1μ
C19 EC 220μ16V
CN3×4
21
22
Y
Z
GNDC
CN1×5
B21 GND
B22 GND
B23 GND
B24 GND
B25 GND
出図
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