MEGA-CD HARDWARE MANUAL
THE HARDWARE

Sega Oldsoft

SEGA ENTERPRISES, LTD.

VER. 1.0 10/14/91

Sega Ozisoft

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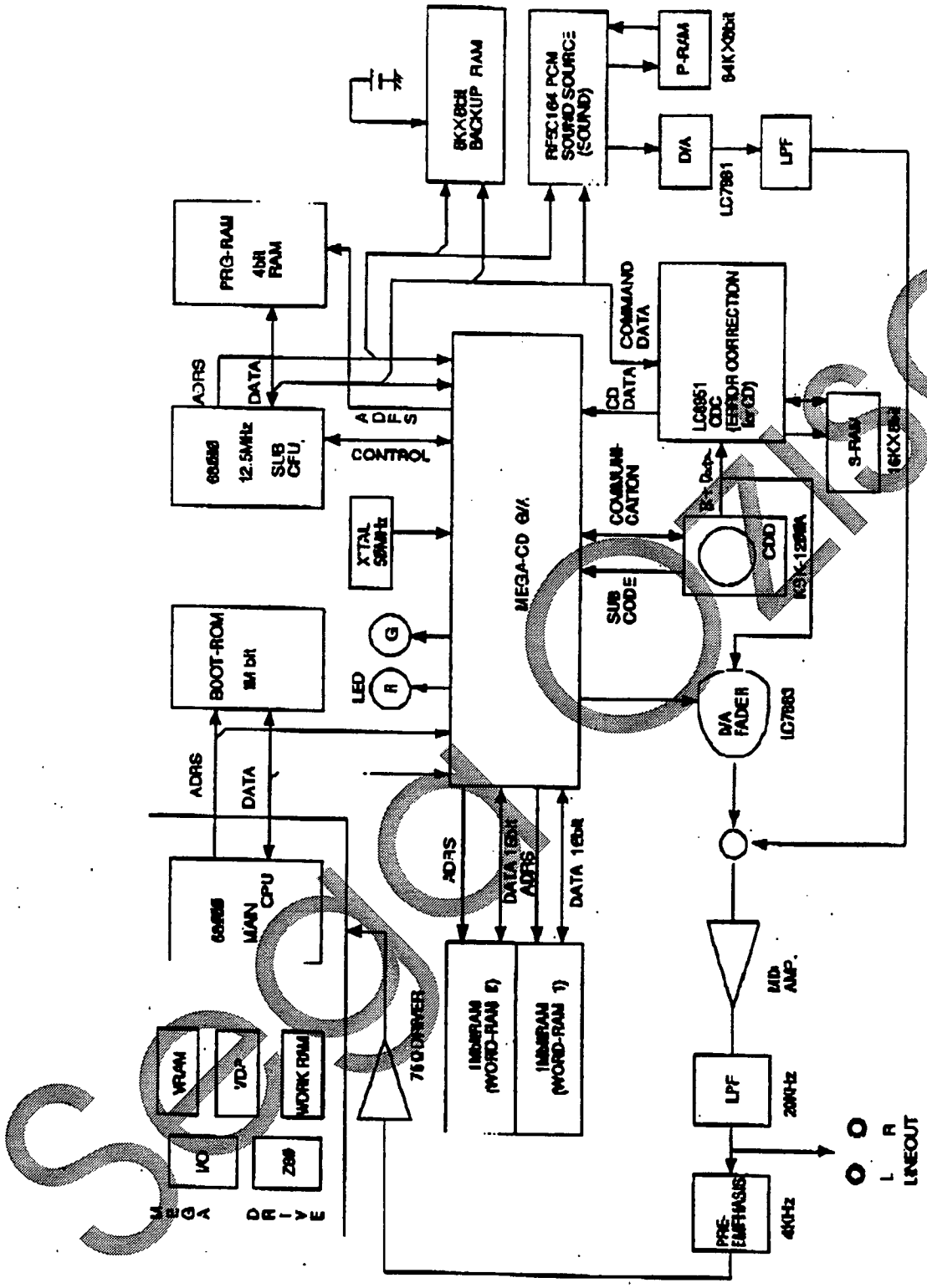

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TERMS USED IN THIS MANUAL

- MD
  The abbreviated name of MEGA DRIVEs.

- MEGA-CD
  The name of a CD-ROM system exclusively used with a MEGA DRIVE.
  This term can either refer to the MEGA-CD unit or the MEGA-CD system.

- MEGA-CD unit
  This includes the CDD of the mechanical section, the SUB-CPU of the control section, etc,. but excludes the MD.

- MEGA-CD system
  The name of a system comprising the MD and CD unit combined.

- MEGA-CD software
  CD-ROM software exclusively used by the MEGA-CD.

- MAIN-CPU
  The 68000CPU of the MD(CPU clock: 7.67MHz).

- SUB-CPU
  The 68000CPU of the MEGA-CD(CPU clock: 12.5MHz).

- PRG-RAM
  A RAM block used mainly as a program area for the SUB-CPU.

- WORD-RAM
  A RAM block used mainly for data transfer between the MAIN-CPU and SUB-CPU.

- Address image
  An area comprising WORD-RAM data which has been formatted for use as VRAM data(Decode Format).

- Normal format
  A term corresponding to the term, decode format.
  A VRAM data format used for the MD. 1 byte holds 2 pixels.
  (All 8 bits of each are used. In this system, the data in the area from $0C0000 to $0DFFFF on the SUB-CPU side in the WORD-RAM 1M mode are used.)

- Decode format
  A data format comprising decoded VRAM data. 1 byte holds 1 pixel; the higher order 4 bits are unused. (In this system, the data in the area from $000000 to $03FFFF on the SUB-CPU side in the WORD-RAM 1M mode are used.)

- HALT
  A control signal for the 68000CPU.
  When this signal is received, the 68000CPU opens the bus immediately after completing the current access(command read out, read, write, etc.). This state is called HALT.
  The CPU's bus can be used externally after creating this state.

- TOC : Table of Contents
  Retrieval data for the music or similar recorded information in the read-in area of the CD. <Refer to the format manual>

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- Stamp
  This term refers to the smallest unit of data which can be processed using numeric functions. A single stamp can be either 16x16 dots (128 bytes) or 32x32 dots(512 bytes) in size. It corresponds to the pattern generator data of the VDP.

- Stamp generator
  A data structure which defines a stamp of 32x32 dots(or 16x16 dots).

- Stamp No.
  Numbers which are assigned in order to the stored stamps beginning with 0, the first number of a stamp generator table. The stamp No. corresponds to the pattern generator numbers.

- Stamp map
  A map comprising stamp numbers arranged according to the screen structure.

- Stamp generator table
  The area where stamp generators are stored It corresponds to a VDP pattern generator.

- Stamp map table
  The area where stamp maps are stored.

- Stamp data
  The data which constitute a stamp map. Stamp data have stamp No./inversion/rotation information and correspond to VDP scroll data.

- Image buffer
  The data area where data processed using the numeric functions are written. The data format is the same as that used by the MD VRAM.

- Trace vector
  The data area where direction and increment description information are stored.
  It is used to transfer the stamp table data structure to an image buffer.

- Sub-code
  The data containing CD time information, CD-G graphics data, etc.
  <Refer to the format manual.>

- CDC : CD Data Controller
  The IC that uses CD-ROM standards to correct errors in CD data sent from the CDD.

- CDD : Compact Disc Driver
  The name of the mechanical section in which music and data are reproduced.
  The term, CD drive, means CDD.

- Emphasis
  Higher sound range emphasis

- Fader
  This circuit performs volume adjustment. By changing the volume setting, fade-ins and fade-outs of several ms can be accomplished. This eliminates the annoying pops which can otherwise be heard when settings are changed using software.

- D/A
  This circuit converts digital data into analog data. It converts the digital information stored in the memory into analog information such as sounds or images.

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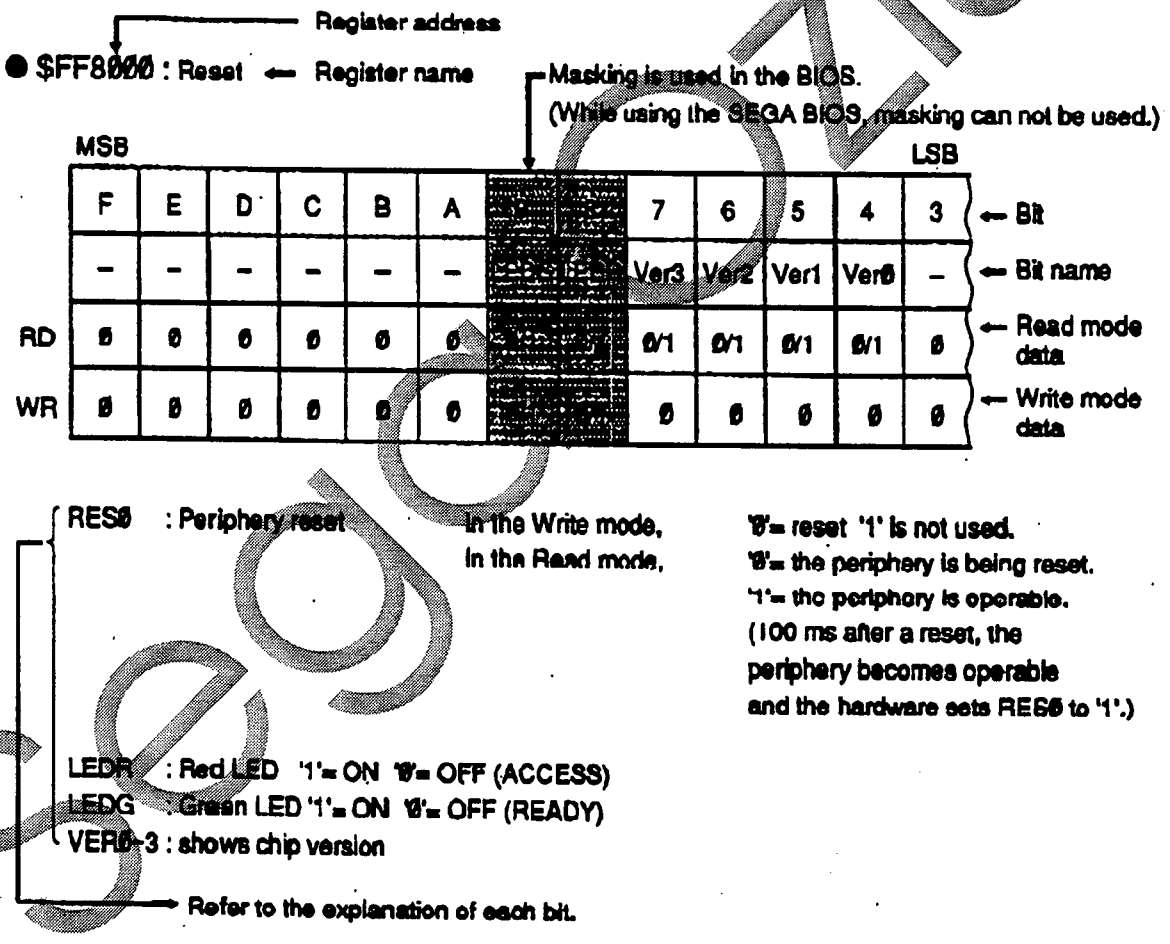
- PCM sound source
  The sound source method through which sounds are recorded as digital data and, when, required re-converted into sounds through the D/A conversion circuit. Original sounds can be faithfully reproduced; however, it requires a large memory capacity for storge.

- LED : Light Emitting Diode
  The LEDs show the CD drive's state.

- Host data
  The name of the CD data read after error correction by the CDC.

REGISTER EXPLANATION



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MEGA-CD CONSTRUCTION

- The MEGA-CD is front loading and is attached underneath the MD.
- The front section is provided with 2 LEDs(indicating working states) and a loading tray.
- The rear section has sound outputs(R & L), an input for sound mixing(the case where a mini jack is installed), and a DC jack(for the MEGA-CD).
- GAME-CD system operation specifications

  - SYSTEM MODE 0 — The case where neither GAME-CD nor cartridge are installed.

    Even while performing its other functions, the BOOT-ROM works as a CD PLAYER. In addition, the CD-G is also supported.

  - SYSTEM MODE 1 — When starting this system from the cartridge. (In this case, the cartridge area is assigned to the MAIN-CPU starting from $000000, and the BOOT-ROM starts from $400000.)

    - TYPE 1 — When only starting a game from a cartridge.
    - TYPE2 — The case where the cartridge(main) and a CD are shared.
      - The case where map data is on a CD.
      - The case where electronically published software is utilized (for example, EB format).

  - SYSTEM MODE 2 — When starting this system from a GAME-CD. (In this case, the cartridge area is assigned to the MAIN-CPU area from $400000 to $7FFFFF, and the BOOT-ROM starts from $000000.)

    - TYPE 1 — The case where a game is played only from a GAME-CD.
    - TYPE 2 — The case where the CD(MAIN) and a cartridge are shared.
      - Back-up cartridge
      - Extension RAM cartridge
      - Other functions(clock, co-processor, etc.)

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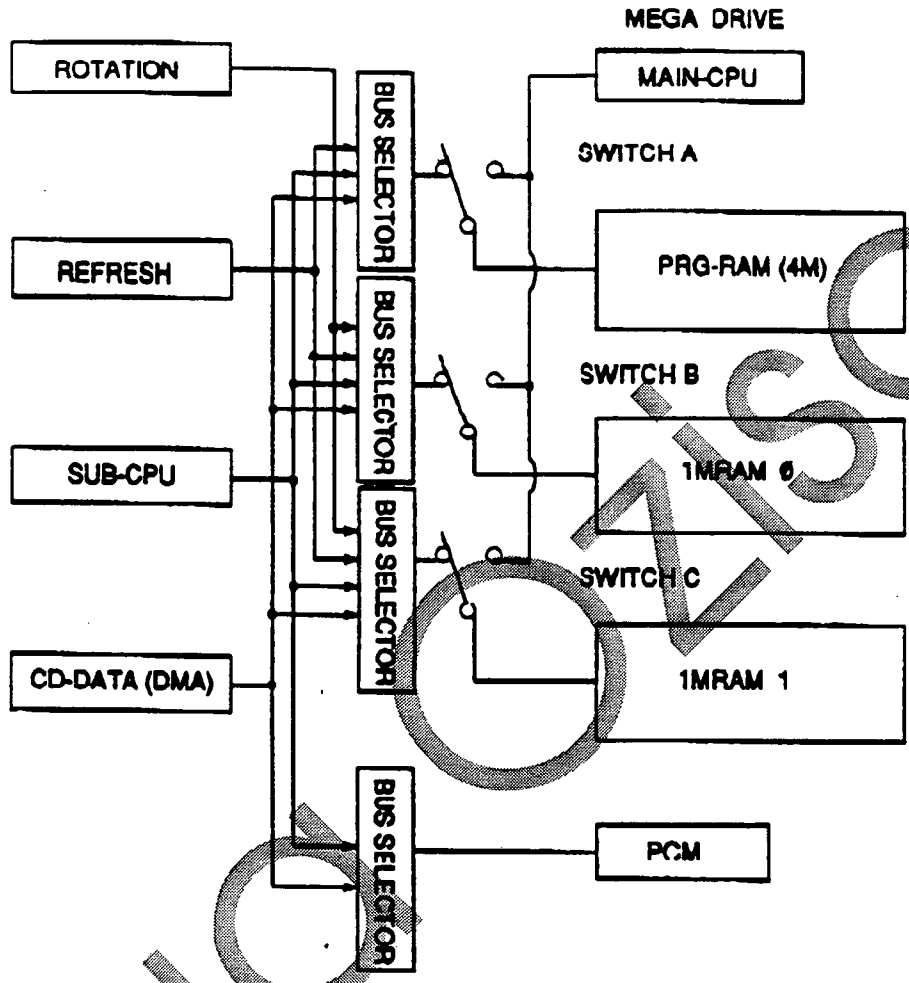
BUS CONSTRUCTION OF CD-ROM INTERIOR



Each memory attached to the CD-ROM has its own bus selection. When there is no competition from other devices, a device can access memory in a non-wait state.

■ Example:
SUB-CPU → PRG-RAM
CD-DATA → 1MRAM0
REFRESH → 1MRAM0
} Each memory can be accessed in a non-wait state.

Switch A: By setting SBRQ=1 or SRES=0 in the MAIN side register $A12001, switch A is set to the MAIN side.

Switch B: When RET=1 within $A12003 in the 2M mode or when RET=0 within $A12003 in the 1M mode, switch B is set to the MAIN side.

Switch C: When RET=1 within $A12003 in the 2M mode or 1M mode, switch C is set to the MAIN side. (For the setting of each switch, refer to $FF8002 of the SUB-CPU.)

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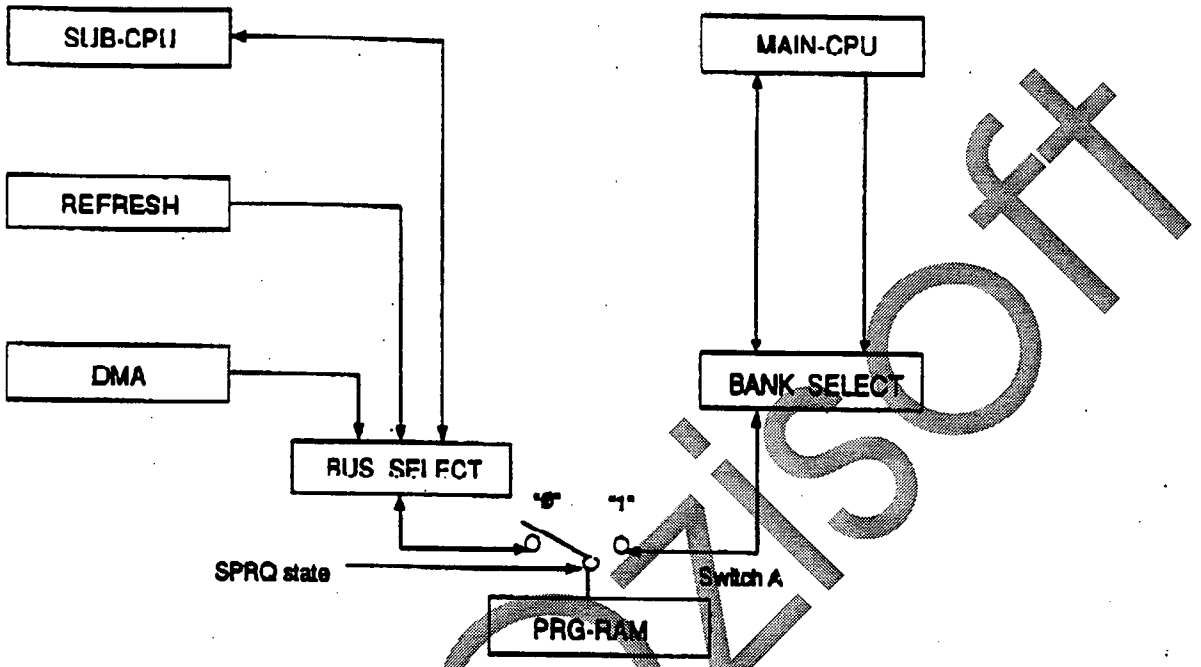
● PRG-RAM



In the figure above, the REFRESH or DMA can access the PRG-RAM unless the SUB-CPU is accessing it.

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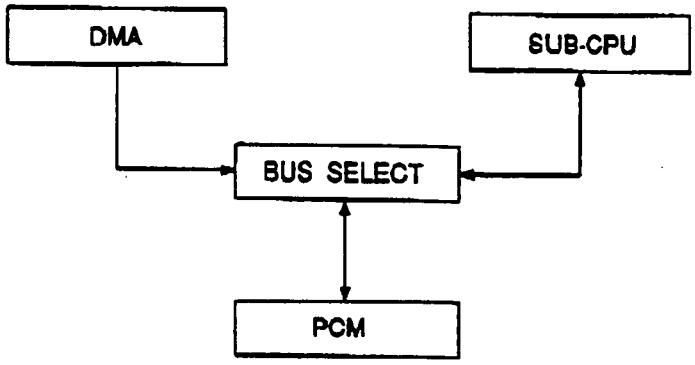
● PCM



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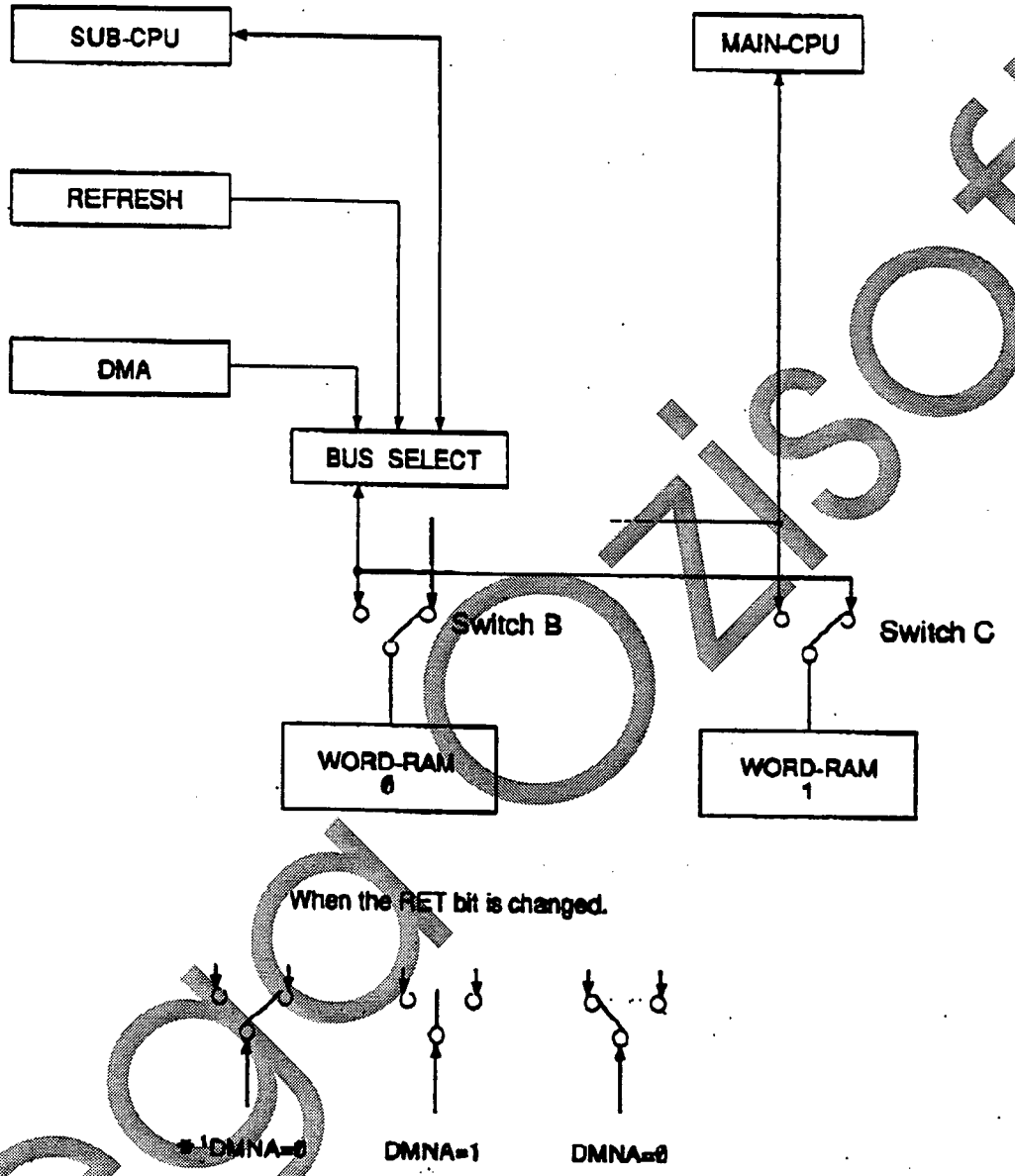
● 1M mode



*1 However, when the MAIN-CPU sets the DMNA bit to '1', the DMNA is set to '1'.

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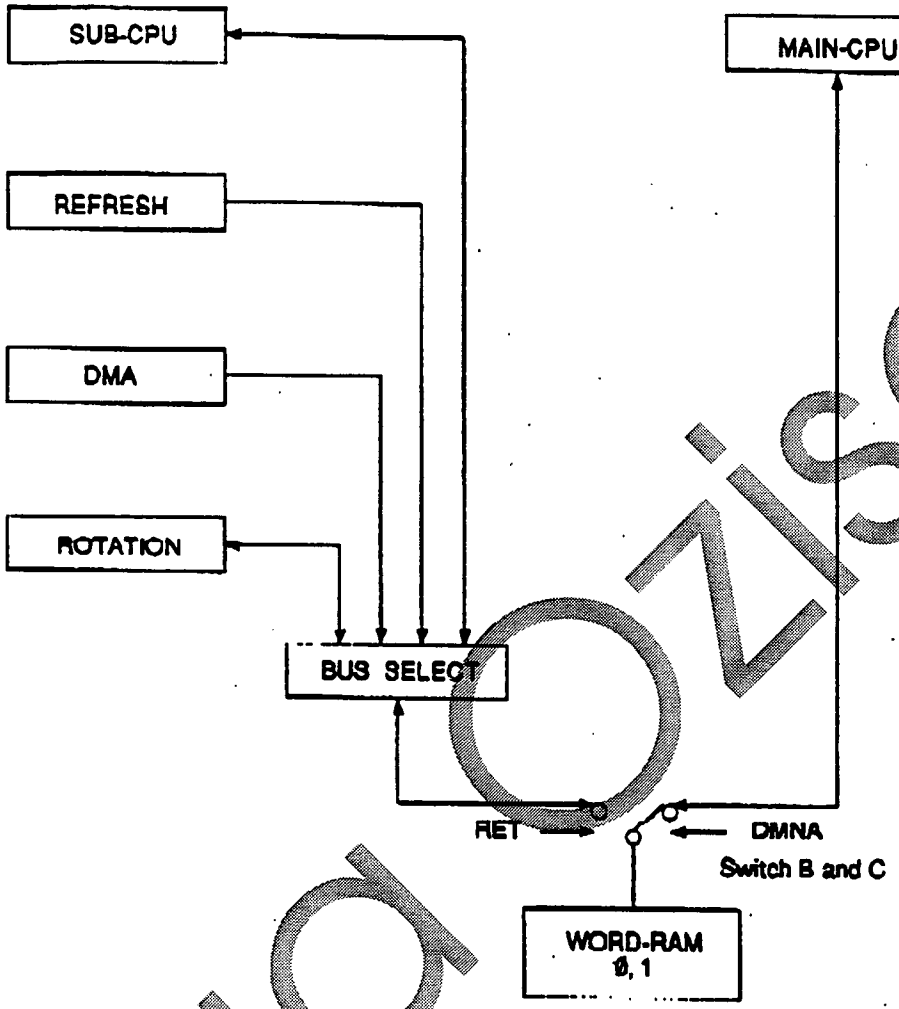
● 2M mode



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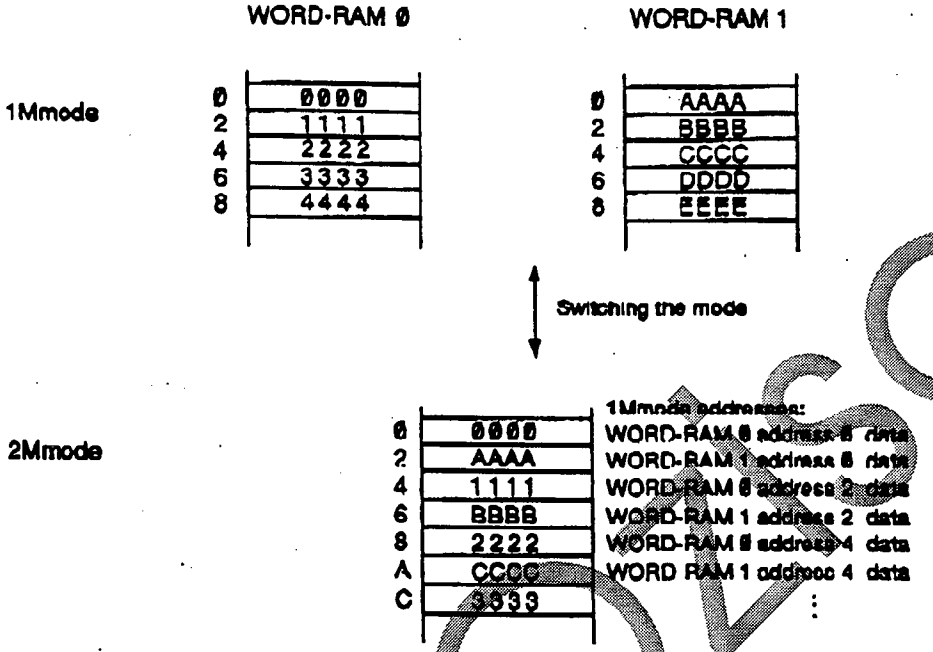
● Data arrangement of the RAM when the WORD-RAM mode is switched.



When the mode is switched, the organization of addresses will change as shown above.

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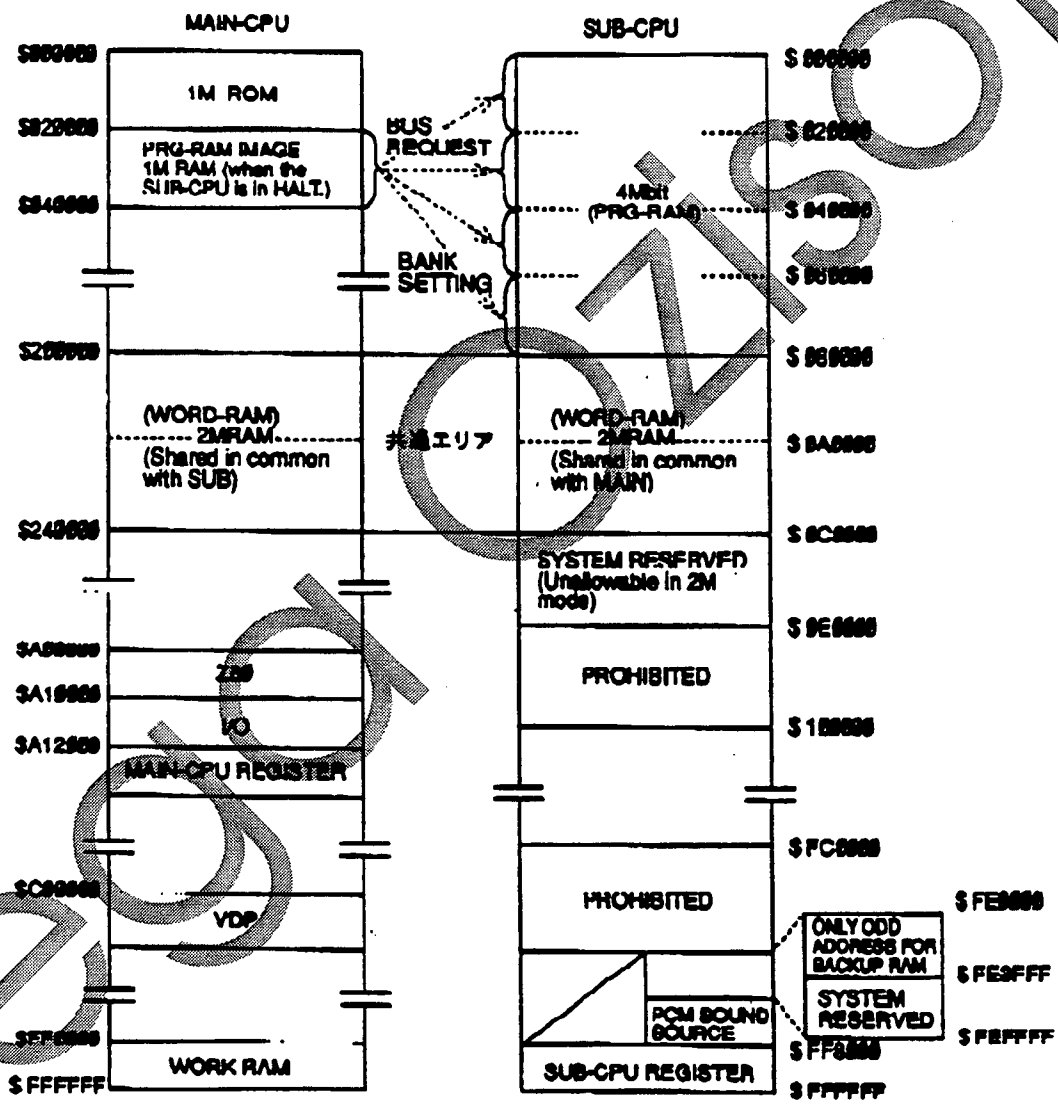
MEGA-CD HARDWARE SPECIFICATIONS

1. MAPPING

1.1 MAPPING MODE

● 2Mmode



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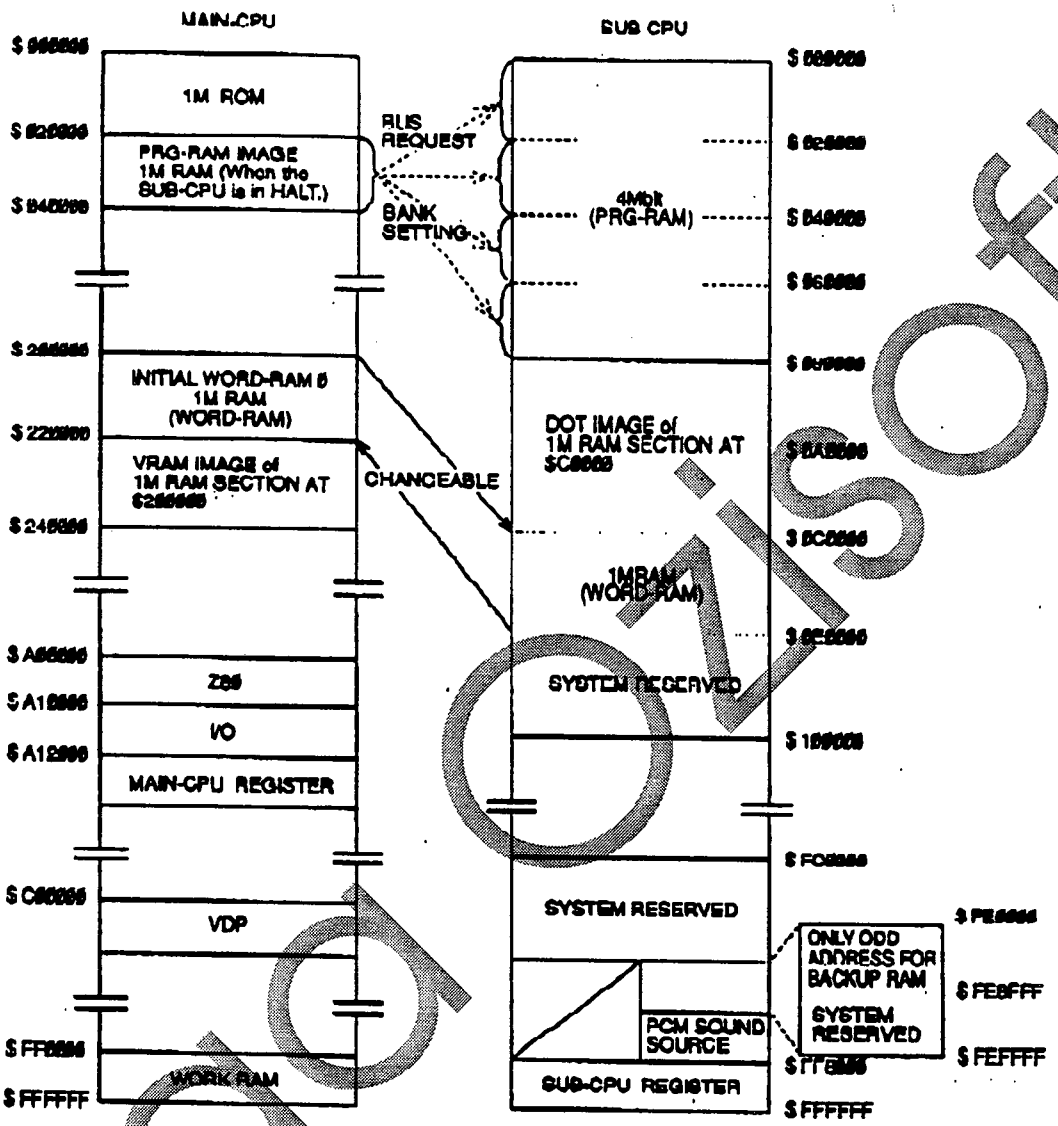
● 1M/1M mode



Note: Never modify data that is reserved by the system.

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1.2 SUB CPU MAPPING

● **$000000~$07FFFF** : Program RAM

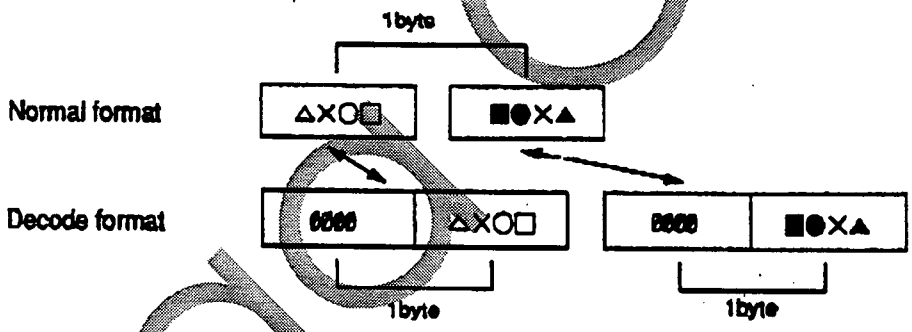
- SUB-CPU program
- CD TOC data
- PCM sound source data

To start this system, transfer a program from the MAIN-CPU to this 4M.
Write protection can be applied between $0 and $1FDFF in units of $200 by means of the MAIN-CPU register $A12002.

● **$080000~$0BFFFF** : When in 2M mode WORD-RAM
When in 1M/1M mode DOT IMAGE

- When in 2M mode, ($FF8002 bit2 mode=0)
  Rotation reduction and coordinate conversion are performed in this RAM.
  Registers from $FF8058 to $FF8066 are used for this.
  They can be used as ordinary RAM.

- When in 1M mode, ($FF8002 bit2 mode =1)
  RAM in this mode contains VRAM images which have been converted into decode format. Data with 2 pixels per byte is accessed as if it had 1 pixel per byte. The upper 4 bits are set to 0 in Read mode and decoded in Write mode.



1 pixel per byte. 1 pixel takes up 4 bits.

● **$0C0000~$0DFFFF** : WORD-RAM

- When in 2M mode, ($FF8002 bit2 mode=0)
  The RAM is not assigned here.
- When in 1M mode, ($FF8002 bit2 mode=1)
  1M of RAM is assigned here (from now on referred to as "WORD-RAM").

The WORD-RAM contains WORD-RAM 0 and WORD-RAM 1, which are exchanged with each other between the MAIN-CPU and SUB-CPU.
For details, refer to register $FF8002.

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● $FE0000-$FEFFFF : Reserved by the system
Under certain conditions the IMAGE may gain access to some of these locations. but it should never modify any of them because they may be used by the system.

● $FE0000-$FE3FFF : Battery backup RAM
8Kbyte. The address is set only in the lower byte (odd byte numbers).

● $FE4000-$FEFFFF : Reserved by the system
The battery back up RAM image may be displayed, but never access it.

● $FF0000-$FF3FFF : PCM sound source address
The address is set only in the lower byte.
For how to use, refer to Appendix 1, PCM Sound Source Manual.

● $FF4000-$FF7FFF : Reserved by the system
The PCM sound source image will be displayed, but never access it.

● $FF8000-$FF81FF : SUB-CPU registers

● $FF8200-$FFFFFF : Reserved by the system

● SUB-CPU INTERRUPT TABLE

INT-LEVEL		
LEVEL6	Sub-code	When 96 byte buffering is completed
LEVEL5	CDC	When error correction or buffering is completed
LEVEL4	CDD	When the reception of the command. Reception Status 7, is completed
LEVEL3	Timer	When the down counter is reset to 0
LEVEL2	MD	A software INT is issued on the MAIN-CPU.
LEVEL1	Graphics	This applies to 2M mode when a graphics numeric operation is completed

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1-3 MAIN-CPU MAPPING

- **$000000~$01FFFF :** for CD-ROM boot
- **$020000~$03FFFF :** If the BREQ and/or SRES are applied to the SUB-CPU, 1M bits out of 4M bits of the PRG-RAM on the SUB-CPU side can be Read/Written by setting the BANK.
- **$040000~$1FFFFF :** Reserved by the system
- **$200000~$23FFFF :** WORD-RAM

Refer to the register $FF8002 on the SUB-CPU side also.

- When in 2M mode, ($FF8002 bit 2 mode=0)
  Use the same WORD-RAM as that of the SUB-CPU by switching the mode.
  When the power is turned ON, the WORD-RAM is attached here in this mode.
- When in 1M mode, ($FF8002 bit 2 mode=1)
  Either WORD-RAM 0 or 1 is assigned to the address range $200000 to $21FFFF.
  The bit map image data which is stored in the address range $200000 to $21FFFF is converted into a cell image and written into the range $220000 to $23FFFF. When CG data cells are arranged in a line they form a cell image. A direct DMA transfer can be done upon a cell image.

(1) V-256 × H-512 dots and V-32-cells × H-64-cells stored in $200000 to $20FFFF are converted and written into $220000 to $22FFFF.

(2) V-128 × H-512 dots and V-16-cells × H-64 cells stored in $210000 to $217FFF are converted and written into $230000 to $237FFF.

(3) V-64 × H-512 dots and V-8-cells × H-64-cells stored in $218000 to $21BFFF are converted and written into $238000 to $23BFFF.

(4) V-32 × H-512 dots and V-4-cell × H-64-cells stored in $21C000 to $21DFFF are converted and written into $23C000 to $23DFFF.

(5) V-32 × H-512 dots and V-4-cells × H-64-cells stored in $21E000 to $21FFFF are converted and written into $23E000 to $23FFFF.

1) Dot-map address and cell map address corresponding to the dot

Dot number on the dot map	Dot map address $200000	Cell map address $220000	Dot number on the dot map.	Dot map address $200000	Cell map address $220000
0、 1 dot	$000	$000	512,513 dot	$100	$004
2、 3 dot	$001	$001	514,515 dot	$101	$005
4、 5 dot	$002	$002	516,517 dot	$102	$006
6、 7 dot	$003	$003	518,519 dot	$103	$007
8、 9 dot	$004	$400	520,521 dot	$104	$404
10、 11 dot	$005	$401	522,523 dot	$105	$405
12、 13 dot	$006	$402	524,525 dot	$106	$406

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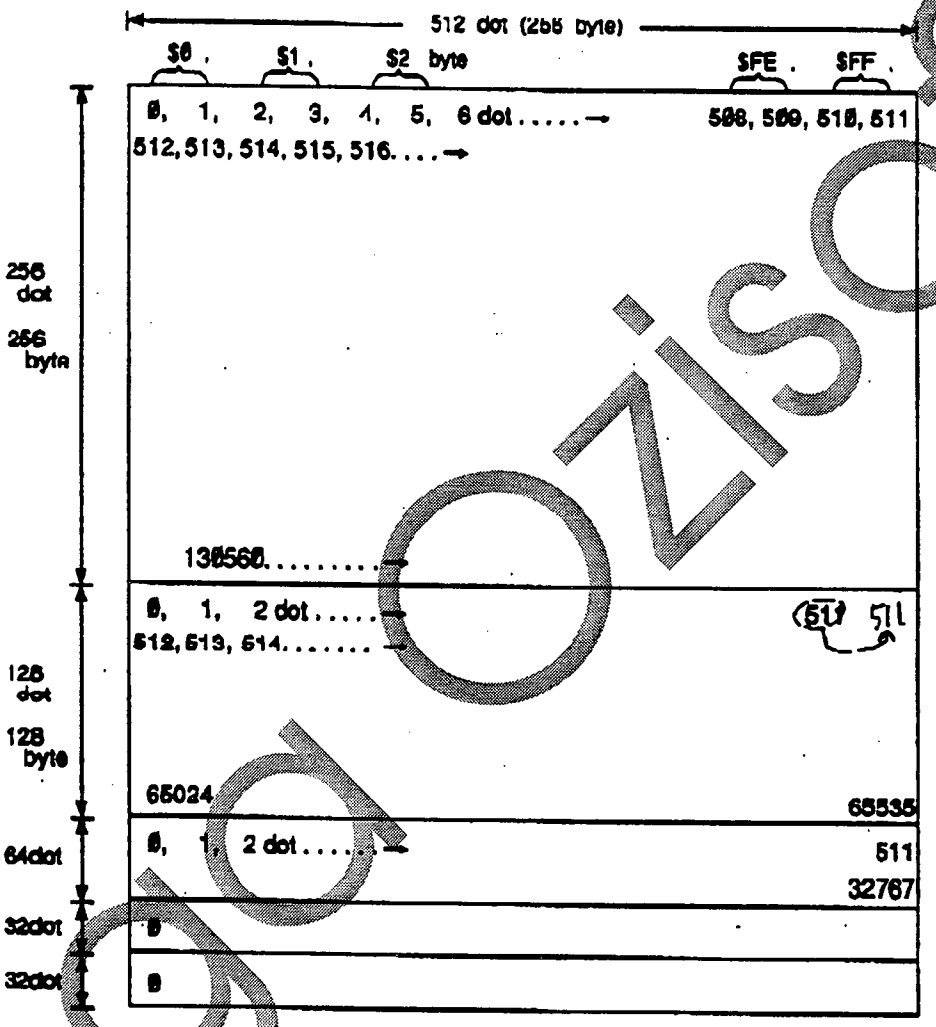
- **The WORD-RAM 0 or 1 addresses $200000 to $21FFFF can contain bit images structured as follows:**

Screen size.....H 512 dots fixed

Four types of V-256 dots, 128 dots, 64 dots, and 32 dots, but there are two 32 dot sizes.
1 dot consists of 4 bits. (Bit 7 to bit 4 create the 0 dot, and bit 3 to bit 0 create the 1 dot.)



The range $220000 to $23FFFF is used for transferring a cell image as mentioned above, and the data is transferred in the same way as the cells are arranged. The cells are arranged in a line as :

0, 1, 2, 3, 4, 5, 6, 7, 512, 513,...,1024, 1025,..., 1031,...,.

Then, when 130560 is reached, it continues as :

8, 9, 10, 11, 12, 13, 14, 15, 520, 523,... 527, 1032,..., and then cells become as follows.

The number of v-cells in a line is determined by a 1M address.

32 cells : $220000~
16 cells : $230000~
8 cells : $238000~
4 cells : $23C000~and $23E000~

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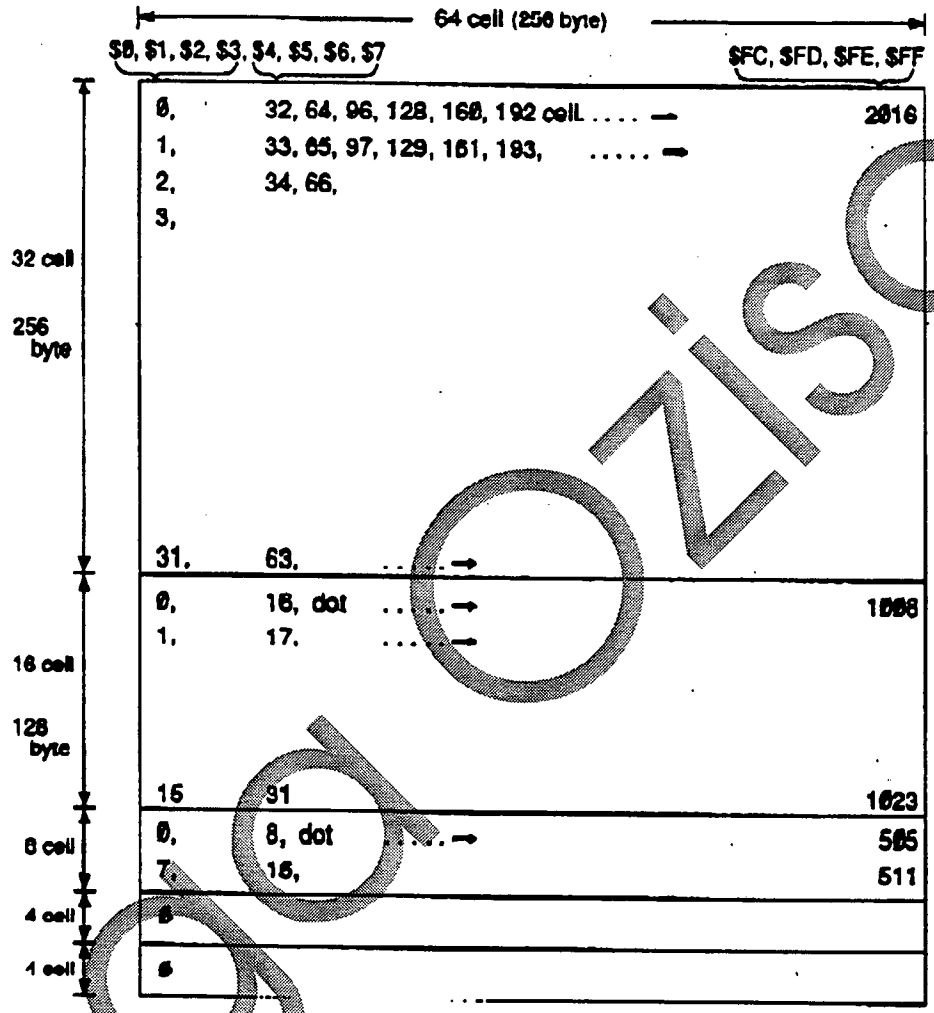
● **The dot image data in $200000 to $21FFFF can be converted into a cell image and written into $220000 to $23FFFF.**

Screen size ..... H-64 cells fixed
Four types of V-32 cells, 16 cells, 8 cells, and 4 cells, but there are two 4 cell sizes.
1 cell consists of 8 x 8 dots.



The range $220000 to $23FFFF is used for transferring a cell image as mentioned above, and the data is transferred in the same way as the cells are arranged. The cells are arranged in a line as :

0, 1, 2, 3, 4, 5, 6, 7, 512, 513,...,1024, 1025,...,1031,...

Then, when 1$0000 is reached, it continues as

8, 9, 10, 11, 12, 13, 14, 15, 528, 523,...527, 1032,...,

and then cells become as follows.

The number of v-cells in a line is determined by a 1M address.

32 cells : $220000~
16 cells : $230000~
8 cells : $238000~
4 cells : $23C000~and $23E000~

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2. MEGA-CD REGISTER TABLE

OFF SET	SIZE	SUB-CPU side Base address $FF8000	MAIN CPU side Base address $A12000
		Initialization	**Initialization**
00	1	VER NO./RESET/LED	Reset/INT2
02	1	Memory mode/Priority/Write protect	Memory mode/Write protect
		CDC (from INT5 LC8951)	**CDC**
04	1	CDC mode/CDC register address	CDC mode
06	1	CDC register data	H-INT
08	1	CDC host data (16 bit)	CDC host data (16 bit)
0A	1	CDC DMA address	
		Communication	**Communication**
0C	1	Stop watch	Stop watch
0E	1	Communication flag	Communication flag
10 ↓ 1E	8	Communication command R/O	Communication command R/W
20 ↓ 2E	8	Communication status R/W	Communication status R/O
		General purpose timer	
30	1	TIMER (INT 3)	
		Interrupt	
32	1	INT mask	
		CDD	
34	1	Fader	
36	1	CDD control	
38 ↓ 40	5	CDD status (INT 4)	
42 ↓ 4A	5	CDD command	
		Color arithmetic operation	
4C	1	Font color	
4E	1	Font bit	
50 ↓ 56	4	Font data	

※Size unit : WORD

※If not otherwise mentioned, byte/word access and bit operation commands are allowed.

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OFFSET	SIZE	SUB-CPU side Base address $FF8000	MAIN-CPU side Base address $A12000
		Rotation reduction	
		(INT 1 for only 2M mode)	
58	1	Stamp size	
5A	1	Stamp map base address	
5C	1	Image buffer V-cell size	
5E	1	Image buffer start address	
60	1	Image buffer offset	
62	1	Image buffer Hdot size	
64	1	Image buffer Vdot size	
66	1	Trace vector base address	
		Sub code	
68	1	Sub-code address	
6A ↓ FE	4B	Reserved by the system	
100 ↓ 17E	40	Sub-code data(INT6)	
180 ↓ 1FE	40	Sub-code data image	

※Size unit : WORD

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● **Initial values of registers after Power ON. (X means unknown.)**

■ SUB-CPU side

Register	Initial Value		Access	Bit operation command
FF8000	0000	However, the RES0 (bit 0) after approx.100ms automatically becomes '1'.	W/B	O
FF8002	0001		W/B	O
FF8004	0000		W/B	Only btst
FF8006	00XX		W/B	X
FF8008	XXXX		W	X
FF800A	XXXX		W	X
FF800C	----	Counting is started at approximately the same time when the MAIN-CPU is started.	W	X
FF800E	0000		W/B	O
FF8010 ~FF802E	0000		W/B	O
FF8030	0000		W/B	O
FF8032	0000		W/B	O
FF8034	0000		W	X
FF8036	0100		W/B	X
FF8038 ~FF804A	0000		W/B	X
FF804C	0000		W/B	O
FF804E	0000		W/B	O
FF8050 ~FF8056	0000		W/B	O
FF8058	0000		W/B	O
FF805A	0000		W	X
FF805C	0000		W/B	X
FF805E	0000		W	X
FF8060	0000		W/B	O
FF8062	0000		W	X
FF8064	0000		W	X
FF8066	XXXX		W	X
FF8068	00XX		W/B	O
FF8100 ~FF81FE	XXXX		W/B	O

■ MAIN-CPU side

Register	Initial value		Access	Bit operation command
A12000	0002		W/B	Only btst
A12002	0001		W/B	O
A12004	0000		W/B	O
A12006	FFFF		W	X
A12008	XXXX		W	X
A1200A	----			
A1200C	0000		W	X
A1200E	0000		W/B	O
A12010 ~A1202E	0000		W/B	O

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3. SUB-CPU REGISTERS

3.1 INITIALIZATION

● **$FF8000 : Reset**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	–	–	–	–	–	–	LEDR	LEDG	Ver3	Ver2	Ver1	Ver0	–	–	–	RES0
RD	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0/1
WR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RES0 : Periphery reset In the Write mode, '0'= reset '1'= not used
In the Read mode, '0'= the periphery is being reset.
'1'= the periphery is operable.
(100 ms after a reset, the periphery becomes operable and RES0 becomes '1'.)

LEDR : Red LED '1'= ON '0'= OFF(ACCESS)
LEDG : Green LED '1'= ON '0'= OFF(READY)
VER0~3 : shows chip version.

Green	Red	Operation indicators for the CPU and CDD(The BIOS is set.)
1	0/1	CD READY...No CD is installed, or waiting for the reading of the TOC to complete.
1	0	CD READY...A CD is installed(If the CD can be read).
1	1	CD ACCESS
0/1	0	STANDBY MODE

※Power-on and a reset cause the hardware to set LEDG and LEDR to '0'.
※Combinations other than the above require a special system mode.
※0/1 means blink.

● **$FF8002 : Memory mode**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0	–	–	–	PM1	PM0	MODE	DMNA	RET
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0	0/1

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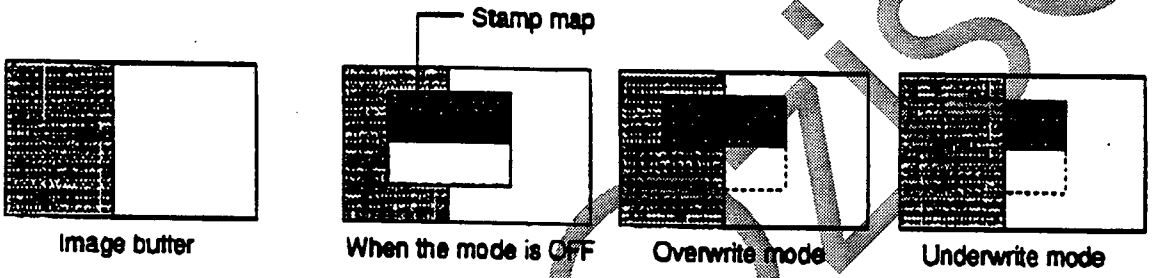
PM0,1 : Priority mode 0,1

PM1	PM0	Operation
0	0	MODE OFF(Default)
0	1	Underwrite mode
1	0	Overwrite mode
1	1	Prohibited

When writing from the SUB-CPU into WORD-RAM in 1M mode and when writing an image twice that of the WORD-RAM, the priority determines the write mode(normal, Underwrite, Overwrite).

In the 2M mode, only the rotation function can Overwrite and Underwrite data taken from the stamp map onto the image buffer.

MODE OFF .....All of the data from the stamp map is written to the image buffer.
Overwrite .....Non zero stamp map data overwrites data in the image buffer.
Underwrite .....If the data stored in the image buffer is $00, the data from the stamp map is Underwritten onto the image buffer.



MODE : RAM mode
'0'=2Mmode '1'=1Mmode

DMNA : Declaration of Main ram No Accsess
mode= '0' (2M mode)
When the DMNA bit is set to '1', the 2M RAM is returned to the SUB-CPU(the RET bit performs the opposite function).
In the Read mode, a DMNA of '0' means the 2M RAM has not yet been returned to the SUB-CPU, a DMNA of '1' means the 2M RAM has been returned to the SUB-CPU.
mode= '1' (1M mode)
In the Read mode, A DMNA of '1' indicates that the MAIN-CPU has made a swap request to the SUB-CPU. Setting the RET bit also causes the DMNA bit to be set to '1'.
In the Read mode, a DMNA of '0' means the completion of swap.

RET : RET bit
mode= '0' (2M mode)
The RET bit returns the 2M RAM to the MAIN-CPU (the DMNA bit performs the opposite function).
In the Write mode, when the RET bit is set to '1', the 2M RAM is returned to MAIN-CPU.
In the Read mode, a RET of '0' means the 2M RAM has not yet been returned to the MAIN-CPU, a RET of '1' means the 2M RAM has been returned to the MAIN-CPU.

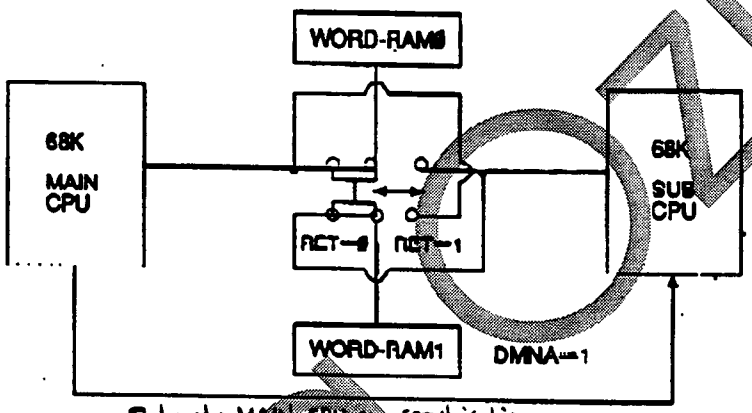
mode= '1' (1M mode)

When the RET bit is set to '0', WORD-RAM 0 is returned to the MAIN-CPU and WORD-RAM 1 is returned to the SUB-CPU. When the RET bit is set to '1', WORD-RAM 0 is returned to the SUB-CPU and WORD-RAM 1 is returned to the MAIN-CPU.

WP0-7 : The WP bits are used to determine the PRG-RAM addresses that are protected by the MAIN-CPU. The address range $0 to $1FDFF of the SUB-CPU is protected in multiples of $200 elements.
If a WP bit field is nonzero then the corresponding $200 element range is protected.

Note If the SUB-CPU accesses the WORD-RAM when mode is 0 and RET is 1, the CPU becomes hang up and will not operate after the access. In this case the back-up state of the SUB-CPU can not be canceled unless a forced reset is done.

● WORD-RAM switching in the 1M mode



Only the MAIN-CPU can set this bit.

The DMNA bit in the 1M mode: ~~WORD-RAM can be written only in the MAIN-CPU.~~ This bit is set to '1' to request switching, setting the bit to '0' has no significance. The SUB-CPU performs the switching request by setting the RET bit. After the WORD-RAM has been switched, the DMNA bit returns to '0'. In the READ mode a DMNA of '1' means switching requested, a DMNA of '0' means switching completed.

Only the SUB-CPU can set this bit.

The RET bit in the 1M mode: ~~WORD-RAM can be written only in the SUB-CPU.~~ When the RET bit is set to '1', WORD-RAM 1 is switched to the MAIN-CPU, and WORD-RAM 0 is switched to the SUB-CPU. When the RET bit is set to '0', WORD-RAM 0 is switched to the MAIN CPU, and WORD-RAM 1 is switched to the SUB-CPU. In READ mode, the current RET bit setting can be read.

※ In the initial state of the system, the MAIN-CPU is given access to WORD-RAM in the 2M mode.

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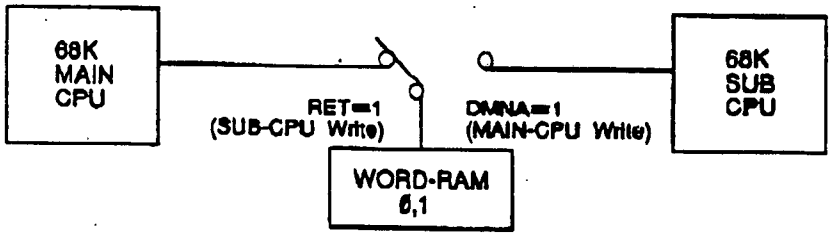
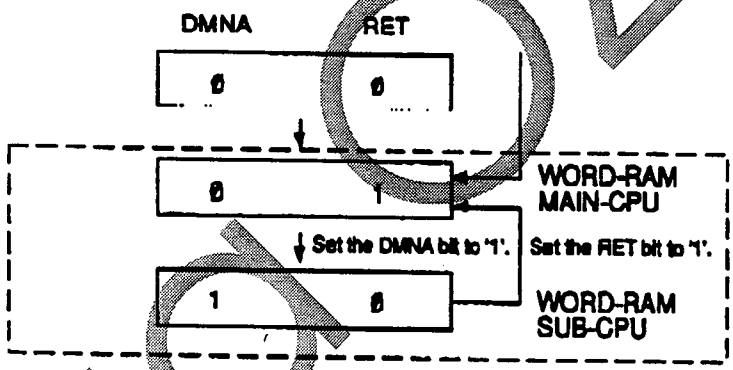
● WORD-RAM switching in the 2M mode



DMNA bit in the 2M mode : ~~WORD-RAM can be written only in the MAIN-CPU.~~ Only the MAIN-CPU can set this bit.
Setting this bit to '1' attaches both WORD-RAM 0 and 1 to the SUB-CPU. In the Read mode, a DMNA bit setting of '1' indicates that the attachment of the SUB-CPU to WORD-RAM 0 and 1 is complete.

RET bit in the 2M mode : ~~WORD-RAM can be written only in the SUB-CPU.~~ Only the SUB-CPU can set this bit.
Setting this bit to '1' attaches both WORD-RAM 0 and 1 to the MAIN-CPU. In the Read mode, a RET bit setting of '1' indicates that the attachment of the MAIN-CPU to WORD-RAM 0 and 1 is complete.



After setting the DMNA or RET bits, verify that both the DMNA and RET bits have changed to the desired state. Then access the WORD-RAM.

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3-2 CDC

● **$FF8004 : CDC mode/CDC register address**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	LSB
	EDT	DSR	UBR	–	–	DD2	DD1	DD0	–	–	–	–	CA3 CA2 CA1 CA0
RD	0/1	0/1	0	0	0	0/1	0/1	0/1	0	0	0	0	
WR	0	0	0	0	0	0/1	0/1	0/1	0	0	0	0	

CA0~3 : CDC register address

UBR : Upper Byte Ready
This indicates that the high order data has been sent from the CDC. When the low order data is sent, the UBR is cleared.

DSR : Data Set Ready
This indicates that the CDC has sent the low order data. After using the MAIN-CPU to read the data once and after transfering the data once to the DMA, in other words after the completion of data transfer, the DSR is cleared.
DD2~0=4 (In the case of doing DMA for the PCM sound source, when the gate array receives one byte from the CDC, the DSR is set to '1'. When the gate array sends one byte of data to the PCM, the DSR bit is reset.)
(When handling words, the DSR is set to '1' after the gate array receives two bytes of data from the CDC and after the gate array sends two bytes of data to the PCM, the DSR bit is reset.)

EDT : End of Data Transfer
This indicates that all the data has been transferred from the CDC.
This is reset when the device destination is set. When the data transfer from the CDC is complete, this is set. When the data transfer from the CDC starts again, this is reset.

DD0~2 : Device Destination
This indicates how to process the data from the CDC.

DD2	DD1	DD0	Destination 2Mmode	1Mmode
0	0	0	Do not set	Do not set
0	0	1	Do not set	Do not set
0	1	0	MAIN-CPU READ	MAIN-CPU READ
0	1	1	SUB-CPU READ	SUB-CPU READ
1	0	0	PCM sound source DMA	PCM sound source DMA
1	0	1	PRG-RAM DMA	PRG-RAM DMA
1	1	0	Do not set	Do not set
1	1	1	SUB-CPU side 2M RAM DMA	SUB-CPU side 1M RAM DMA

※ Only when attached to the SUB-CPU.
When attached to the MAIN-CPU, DMA can not be done.

Note Suspend of data transferring by resetting the CDD using the reset register in the CDC and then writing the proper values in DD2~DD1.

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※ For all resets except for Power-On, the DD2~DD0 hold previous values, but the circuit for transferring may sometimes be unsteady. Therefore, after a reset, set the register again.

※ When data is written in DD2~DD0, the DMA circuit is reset (The DMA address is also reset.).

● $FF8006 : CDC Register data

	MSB F	F	D	C	B	A	9	8	LSB
	–	–	–	–	–	–	–	–	
RD	0	0	0	0	0	0	0	0	
WR	0	0	0	0	0	0	0	0	

This register may not be accessed using commands such as BTST, BCLR, BSET, CLR, etc.

CD0~7 : CDC register

● $FF8008 : CDC host data(16 bits) Read Only Word Access

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	HD15	HD14	HD13	HD12	HD11	HD10	HD09	HD08	HD07	HD06	HD05	HD04	HD03	HD02	HD01	HD00
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

HD00~15 : CDC read data bits 00~15

Two bytes from the CDC are accumulated in the host data register and then transfered to the MAIN-CPU or SUB-CPU. After the data in HD 00-15 has been read, the CDC transfers the next 2 bytes of data into this register.

※ $FF8008 may be read when DSR, bit 15 of $FF8004, is 1.

● $FF800A : CDC DMA address Write Only Word Access

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03
RD	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

For the PCM sound source, the limit is A12, and A13 to A18 are '0'.

For WORD-RAM 0 (1M) and WORD-RAM 1 (1M), the limit is A16, and A17 and A18 are '0'.

In the 2M mode, A18 is '0'.

For the PRG-RAM, all can be used.

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3-3 COMMUNICATION

● **$FF800C : Stop watch** **Word Access**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	–	–	–	–	SW11	SW10	SW09	SW08	SW07	SW06	SW05	SW04	SW03	SW02	SW01	SW00
RD	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	W0	W0	W0	W0	W0	W0	W0	W0	W0	W0	W0	W0

SW00~11 : Timer data bit00~bit11
30.72 µs/count: Counting from 0 to 4095 is possible.
Set to '0' to clear the counter.
Upon overflow, the counter starts from '0' again.

W0 : When writing, only write '0'. A write causes the counter to restart from '0'.

● **$FF800E : Communication flag**

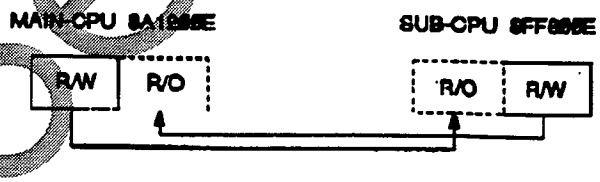
	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	CFM7	CFM6	CFM5	CFM4	CFM3	CFM2	CFM1	CFM0	CFS7	CFS6	CFS5	CFS4	CFS3	CFS2	CFS1	CFS0
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

CFS0~7 : Communication Flag for the SUB-CPU bit0~bit7
This is a flag for communications from the SUB-CPU to the MAIN-CPU.

CFM0~7 : Communication Flag for the MAIN-CPU bit0~bit7
This is a flag for communication from the MAIN-CPU to the SUB CPU.

When both the MAIN-CPU and SUB-CPU simultaneously Read and Write using the Communication flags, the write will execute normally, but the data resulting from the Read may sometimes include former data. For transferring byte data or word data, therefore, do not simultaneously Read and Write using the Flags. When only 1 bit for a bit test is of interest, the above problem will not occur.

The MAIN-CPU and SUB-CPU registers share data in common. Values written on lower bytes of the SUB-CPU appear on lower bytes of the MAIN-CPU.



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● **$FF8010~$FF801E : Communication command 8 words** **Read Only**

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Communication command 0															
Communication command 1															
Communication command 2															
Communication command 3															
Communication command 4															
Communication command 5															
Communication command 6															
Communication command 7															

● **$FF8020~$FF802E : Communication status 8 words** **Read/Write**

MSB LSB

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
Communication status 0															
Communication status 1															
Communication status 2															
Communication status 3															
Communication status 4															
Communication status 5															
Communication status 6															
Communication status 7															

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3-4 GENERAL PURPOSE TIMER

● $ FF0030 :Timer W/INT3

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	–	–	–	–	–	–	–	–	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
RD	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

TD0~7 : Timer data bit0-bit7
30.72μs/count : Count down from n to 0 is started when 'n' is written.(0<n≤255)
When the counter counts to '0', INT LEVEL 3 will be generated.
If '0' is set, INT3 will not be generated.
In the read mode, set values can be reread.(This does not include the count value.)
The reset value is '0'.
The interrupt interval will be (n+1) x 30.72 μs. (However, 0<n≤255)

3-5 INTERRUPT

● $FF0032 : Interrupt mask control

	MSB F	E	D	C	B	A	9	8	7				3		1	LSB 0
	–	–	–	–	–	–	–	–	–				IEN3		IEN1	–
RD	0	0	0	0	0	0	0	0	0				0/1		0/1	0
WR	0	0	0	0	0	0	0	0	0				0/1		0/1	0

IEN1~6 : Interrupt enable level 1~6
Each interrupt can be Enabled or Disabled.
'0'-Disable '1'-Enable : The Reset mask is usable.

INT-LEVEL		
LEVEL 6	Sub-code	When 98 byte buffering is completed
LEVEL 5	CDC	When errors are corrected or buffering is completed
LEVEL 4	CDD	When the reception of receiving status 7 is completed
LEVEL 3	Timer	When the timer counts to '0' from n
LEVEL 2	MD	Software INT is issued by the MAIN-CPU
LEVEL 1	Graphics	In the 2M mode and when a graphics unmeric operation completes

※ For proper synchronization LEVEL 2 should be issued from V-INT.

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3.6 CDD

● **$FF8034 : CD fader** **Word Access**

※ Direct access to this register using application software is prohibited. ※



FD00~10 : Fade volume data bit04~bit14

The sound volume is adjusted using decay depth. The time taken to go from the present sound volume to the assigned sound volume (the adjustment time) is determined by the following equation.

Adjustment time = 22 µs x adjusted depth

The decay depth is minimum when FD00~10 are %00000000000 and is maximum when they are %11111111111.

When FD09~FD00 are %0000000100 or more, the decay value can be determined by the following expression. In this case FD01~FD00 are not used arithmetically.

-20Log ((FD09 FD08...FD03 FD02)/256)

EFDT : End of Fade Data Transfer

This indicates whether the FD00~FD10 data are still in the process of being sent to the Fader.

'1'=Busy; means that the FD00~FD10 data is being transferred.

'0'=Ready; means that the data can be set.

DEF 1,0 : De-Emphasis Flag

DEF 1	DEF 0	Operation
0	0	OFF
0	1	Fs=44.1KHz
1	0	Fs=32KHz
1	1	Fs=48KHz

Usually OFF

The emphasis which is required by old style classical music CDs is adjusted by DEF.

FD10~FD00	Decay depth	Sound volume is maximum.
%100 0000 0000	0	
011 11111111		
011 11111110		
011 11111101		
011 11111100		
011 11111011		
011 11111010		
⋮		
000 0000 0101		
000 0000 0100		
000 0000 0011		
000 0000 0010		
000 0000 0001		
000 0000 0000	-∞	0

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● $FF8036 : CDD control

※ Direct access to this register using application software is prohibited. ※

	MSB F	E	D	C	B	A	9	[illegible]	7	6	5	4	3	[illegible]	LSB
	–	–	–	–	–	–	–		–	–	–	–	–		
RD	0	0	0	0	0	0	0		0	0	0	0	0		
WR	0	0	0	0	0	0	0		0	0	0	0	0		

WR: In the Write mode, only write '0'

bset and bclr can not be used.

DTS : Data Transmission Status
'1' means that data is being transferred from the communication buffer to the CDD. (When a communication error occurs, current communication is aborted within 240 µs.)
Setting DTS to '0' also aborts the communication.

DRS : Data Receiving Status
'1' means that data is being transferred from the CDD to the communication buffer.(When a communication error occurs, current communication is aborted within 240 µs.)
Setting DRS to '0' also aborts the communication.

HOCK : Host Clock
After the Power is ON, initial value is set to '0'. Changing '0' to '1' starts communication to the CDD.

D/M : Data/Music
D/M indicates whether the current data from the CDD is ROM data or music data.
'1'=ROM data (including STOP and PAUSE.)
'0'=Music data

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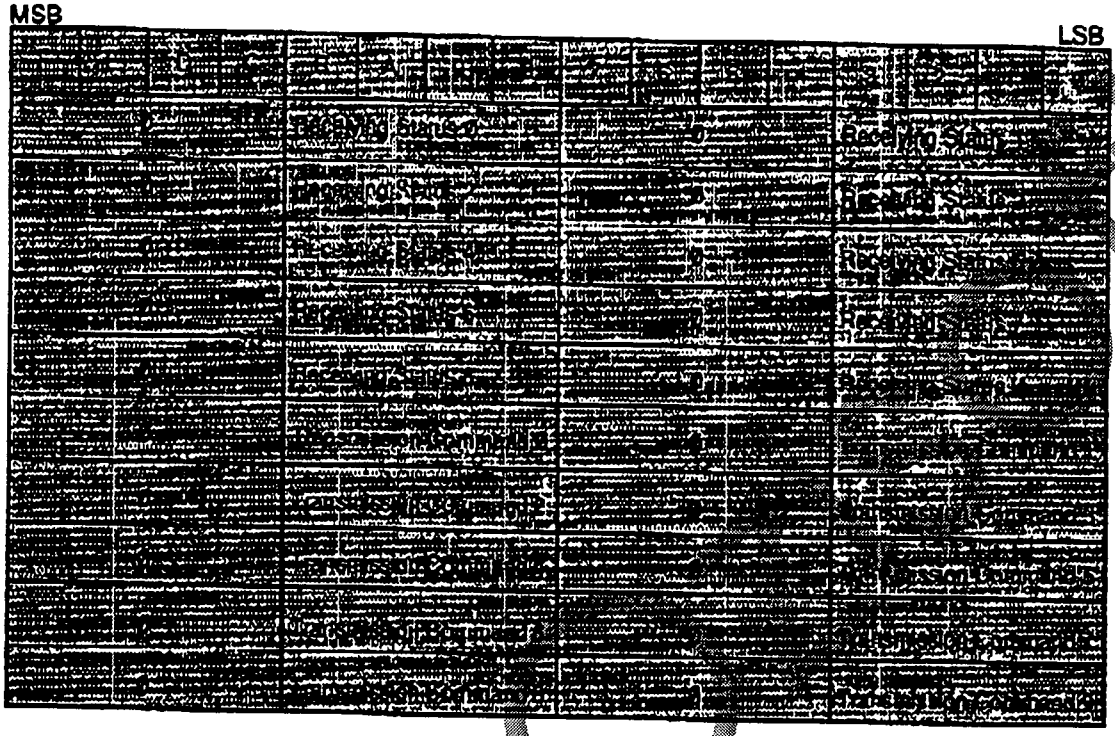
● $FF8038-$FF804A : Communication with the CDD

※ Direct access to this register using application software is prohibited. ※

MSB LSB



When the reception of Receiving Status 7 is complete, INT4 will be generated.
When the SUB-CPU writes Transmission Command 0, communication with the CDD is started.

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3.7 COLOR NUMERIC OPERATION

● **$FF804C : Font color**

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	–	–	–	–	–	–	–	–	SC13	SC12	SC11	SC10	SC03	SC02	SC01	SC00
RD	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SC00~03 : Source Color Data 00~03
These are color codes which are allocated where '0' is set as font bit data.

SC10~13 : Source Color Data 10~13
These are color codes which are allocated wherever font bit data is set to '1'.

● **$FF804E : Font bit**

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	SBF	SBE	SBD	SBC	SBB	SBA	SB9	SB8	SB7	SB6	SB5	SB4	SB3	SB2	SB1	SB0
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

SFB0~F : Source Font Bit 0~F
These registers contain bit pattern data such as Chinese letter font data. This data is converted to the MD VRAM data format using the specified font color data. The converted data is included in the next font data.

● **$FF8050~$FF8056 : Font data** **Read Only**

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
+0	FDF3	FDF2	FDF1	FDF0	FDE3	FDE2	FDE1	FDE0	FDD3	FDD2	FDD1	FDD0	FDC3	FDC2	FDC1	FDC0
+2	FDB3	FDB2	FDB1	FDB0	FDA3	FDA2	FDA1	FDA0	FD93	FD92	FD91	FD90	FD83	FD82	FD81	FD80
+4	FD73	FD72	FD71	FD70	FD63	FD62	FD61	FD60	FD53	FD52	FD51	FD50	FD43	FD42	FD41	FD40
+6	FD33	FD32	FD31	FD30	FD23	FD22	FD21	FD20	FD13	FD12	FD11	FD10	FD03	FD02	FD01	FD00

↑ OFF SET

■ Example: When SC10~SC13=F and SC00~SC03=1, If SB0=0, Then FD00~FD03=1,
If SB0=1, Then FD00~FD03=F

correspondence between bit pattern data and font data: SB0 → FD00~FD03
SB1 → FD10~FD13
⋮
SBF → FDF0~FDF3

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3-8 ROTATION SCALING

● **$FF8058 : Stamp data size**

	MSB															LSB
	F	E	C	D	B	A	9	8	7	6	5	4	3	2	1	0
	GRON	–	–	–	–	–	–	–	–	–	–	–	–	SMS	STS	RPT
RD	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1

STS : Stamp size
This assigns the size of a stamp whithin a Stamp map.
'0'=16x16 dot
'1'=32x32 dot

SMS : Stamp map size
'0'=1x1 screen(256x256 dots)
'1'=16x16 screen(4096x4096 dots)

RPT : Repeat
'1'= Stamp map size The map is repeated.
'0'= When the Stamp map size is exceeded, the data is set to '0'.

GRON: Indicates that a graphics operation is in process.
0 : Operation is completed.
1 : Operation is in process.

● **$FF805A : Stamp map base address** **Word Access**

■ When SMS=0, and STS=0, (1x1 screen, 16x16 dots)

	MSB															LSB
	F	E	C	D	B	A	9	8	7	6	5	4	3	2	1	0
	A17	A16	A15	A14	A13	A12	A11	A10	A09	–	–	–	–	–	–	–
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0	0	0
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0	0	0

■ When SMS=0, and STS=1, (1x1 screen, 32x32 dots)

	MSB															LSB
	F	E	C	D	B	A	9	8	7	6	5	4	3	2	1	0
	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	–	–	–	–	–
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0

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■ When SMS=1, and STS=0 (16×16 screen, 32×32 dots), only A17 can be used.
When using A17, set A17='1'.

■ When SMS=1, and STS=1(16x16 screen, 16x16 dots)

MSB LSB

	F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
	A17	A16	A15	-	-	-	-	-	-	-	-	-	-	-	-	-
RD	0/1	0/1	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0
WR	0/1	0/1	0/1	0	0	0	0	0	0	0	0	0	0	0	0	0

This address determines where the map is allocated in the 2Mbit when the WORD-RAM is in the 2M ROTATION mode.

Stamp data is as follows.

F	E	C	D	B	A	9	8	7	6	5	4	3	2	1	0
HFLP	RT1	RT0	0	0	SNOA	SNO9	SNO8	SNO7	SNO6	SNO5	SNO4	SNO3	SNO2	SNO1	SNO0

HFLP : Crosswise reversion

SNO0~A: Stamp No. When the stamp is 32x32 dots, set SNO0 and SNO1 to '0'.

RT1	RT0	
0	0	: 0°
0	1	: 90°
1	0	: 180°
1	1	: 270°

The beginning address of the Stamp generator is the start of the 2M RAM (for the SUB-CPU, this is $080000). Stamp generators and sprites are organized in the same way.
In the case of 16x16 dots, the arrangement of Addresses is as follows.

$00	$01	$02	$03	$40	$41	$42	$43
$04	$05	$06	$07	$44	$45	$46	$47
$08	$09	$0A	$0B	$48	$49	$4A	$4B
$0C	$0D	$0E	$0F	$4C	$4D	$4E	$4F
$10	$11	$12	$13	$50	$51	$52	$53
$14	$15	$16	$17	$54	$55	$56	$57
$18	$19	$1A	$1B	$58	$59	$5A	$5B
$1C	$1D	$1E	$1F	$5C	$5D	$5E	$5F
$20	$21	$22	$23	$60	$61	$62	$63
$24	$25	$26	$27	$64	$65	$66	$67
$28	$29	$2A	$2B	$68	$69	$6A	$6B
$2C	$2D	$2E	$2F	$6C	$6D	$6E	$6F
$30	$31	$32	$33	$70	$71	$72	$73
$34	$35	$36	$37	$74	$75	$76	$77
$38	$39	$3A	$3B	$78	$79	$7A	$7B
$3C	$3D	$3E	$3F	$7C	$7D	$7E	$7F

2dot /1byte

1 cell

- 1 dot for D7~D4, 1 dot for D3~D0
- D7~D4 of $00 represents the leftmost dot of the top line.
- D3~D0 of $1F represents the rightmost dot of the bottom line.

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In the case of 32x32 dots, the arrangement of addresses is as follows.

$0000	$0001	$0002	$0003	$0080	$0081	$0082	$0083	$0100	$0101	$0102	$0103	$0180	$0181	$0182	$0183
$0004	$0005	$0006	$0007	$0084	$0085	$0086	$0087	$0104	$0105	$0106	$0107	$0184	$0185	$0186	$0187
$0008	$0009	$000A	$000B	$0088	$0089	$008A	$008B	$0108	$0109	$010A	$010B	$0188	$0189	$018A	$018B
$000C	$000D	$000E	$000F	$008C	$008D	$008E	$008F	$010C	$010D	$010E	$010F	$018C	$018D	$018E	$018F
$0010	$0011	$0012	$0013	$0090	$0091	$0092	$0093	$0110	$0111	$0112	$0113	$0190	$0191	$0192	$0193
$0014	$0015	$0016	$0017	$0094	$0095	$0096	$0097	$0114	$0115	$0116	$0117	$0194	$0195	$0196	$0197
$0018	$0019	$001A	$001B	$0098	$0099	$009A	$009B	$0118	$0119	$011A	$011B	$0198	$0199	$019A	$019B
$001C	$001D	$001E	$001F	$009C	$009D	$009E	$009F	$011C	$011D	$011E	$011F	$019C	$019D	$019E	$019F
$0020	$0021	$0022	$0023	$00A0	$00A1	$00A2	$00A3	$0120	$0121	$0122	$0123	$01A0	$01A1	$01A2	$01A3
$0024	$0025	$0026	$0027	$00A4	$00A5	$00A6	$00A7	$0124	$0125	$0126	$0127	$01A4	$01A5	$01A6	$01A7
$0028	$0029	$002A	$002B	$00A8	$00A9	$00AA	$00AB	$0128	$0129	$012A	$012B	$01A8	$01A9	$01AA	$01AB
$002C	$002D	$002E	$002F	$00AC	$00AD	$00AE	$00AF	$012C	$012D	$012E	$012F	$01AC	$01AD	$01AE	$01AF
$0030	$0031	$0032	$0033	$00B0	$00B1	$00B2	$00B3	$0130	$0131	$0132	$0133	$01B0	$01B1	$01B2	$01B3
$0034	$0035	$0036	$0037	$00B4	$00B5	$00B6	$00B7	$0134	$0135	$0136	$0137	$01B4	$01B5	$01B6	$01B7
$0038	$0039	$003A	$003B	$00B8	$00B9	$00BA	$00BB	$0138	$0139	$013A	$013B	$01B8	$01B9	$01BA	$01BB
$003C	$003D	$003E	$003F	$00BC	$00BD	$00BE	$00BF	$013C	$013D	$013E	$013F	$01BC	$01BD	$01BE	$01BF
$0040	$0041	$0042	$0043	$00C0	$00C1	$00C2	$00C3	$0140	$0141	$0142	$0143	$01C0	$01C1	$01C2	$01C3
$0044	$0045	$0046	$0047	$00C4	$00C5	$00C6	$00C7	$0144	$0145	$0146	$0147	$01C4	$01C5	$01C6	$01C7
$0048	$0049	$004A	$004B	$00C8	$00C9	$00CA	$00CB	$0148	$0149	$014A	$014B	$01C8	$01C9	$01CA	$01CB
$004C	$004D	$004E	$004F	$00CC	$00CD	$00CE	$00CF	$014C	$014D	$014E	$014F	$01CC	$01CD	$01CE	$01CF
$0050	$0051	$0052	$0053	$00D0	$00D1	$00D2	$00D3	$0150	$0151	$0152	$0153	$01D0	$01D1	$01D2	$01D3
$0054	$0055	$0056	$0057	$00D4	$00D5	$00D6	$00D7	$0154	$0155	$0156	$0157	$01D4	$01D5	$01D6	$01D7
$0058	$0059	$005A	$005B	$00D8	$00D9	$00DA	$00DB	$0158	$0159	$015A	$015B	$01D8	$01D9	$01DA	$01DB
$005C	$005D	$005E	$005F	$00DC	$00DD	$00DE	$00DF	$015C	$015D	$015E	$015F	$01DC	$01DD	$01DE	$01DF
$0060	$0061	$0062	$0063	$00E0	$00E1	$00E2	$00E3	$0160	$0161	$0162	$0163	$01E0	$01E1	$01E2	$01E3
$0064	$0065	$0066	$0067	$00E4	$00E5	$00E6	$00E7	$0164	$0165	$0166	$0167	$01E4	$01E5	$01E6	$01E7
$0068	$0069	$006A	$006B	$00E8	$00E9	$00EA	$00EB	$0168	$0169	$016A	$016B	$01E8	$01E9	$01EA	$01EB
$006C	$006D	$006E	$006F	$00EC	$00ED	$00EE	$00EF	$016C	$016D	$016E	$016F	$01EC	$01ED	$01EE	$01EF
$0070	$0071	$0072	$0073	$00F0	$00F1	$00F2	$00F3	$0170	$0171	$0172	$0173	$01F0	$01F1	$01F2	$01F3
$0074	$0075	$0076	$0077	$00F4	$00F5	$00F6	$00F7	$0174	$0175	$0176	$0177	$01F4	$01F5	$01F6	$01F7
$0078	$0079	$007A	$007B	$00F8	$00F9	$00FA	$00FB	$0178	$0179	$017A	$017B	$01F8	$01F9	$01FA	$01FB
$007C	$007D	$007E	$007F	$00FC	$00FD	$00FE	$00FF	$017C	$017D	$017E	$017F	$01FC	$01FD	$01FE	$01FF

1 dot in D7~D4, 1 dot in D3~D0
D7~D4 of $0000 represents the leftmost dot of the top line.
D3~D0 of $01FF represents the rightmost dot of the bottom line.

This section corresponds to 1 cell of the MD.
The arrangement of cells is the same as the MD Sprite.

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● **$FF805C : Image buffer V cell size(0-31 cells)**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	-	-	-	-	-	-	-	-	-	-	-	VCS4	VCS3	VCS2	VCS1	VCS0
RD	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1

VCS0~4 : This determines the number of image buffer vertical cells.
When setting, set the value to (actual value-1).

● **$FF805E : Image buffer start address** **Word Access**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	-	-	
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0

● **$FF8060 : Image buffer offset**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	-	-	-	-	-	-	-	-	-	-	LN2	LN1	LN0	dot2	dot1	dot0
RD	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1

LN0~2 : These indicate line numbers in the first cell written into the image buffer.
dots 0~2 : These indicate dot number in the lines indicated by LN0~2.

● **$FF8062 : Image buffer H dot size(horizontal dot size to be rewritten in the buffer)**

Word Access

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	-	-	-	-	-	-	-	HW08	HW07	HW06	HW05	HW04	HW03	HW02	HW01	HW00
RD	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

HW00~08 : These indicate the number of horizontal dots to write. The location for writing is determined by the image buffer start address and the image buffer offset.

● **$FF8064 : Image buffer Vdot size(vertical dot size to be rewritten in the buffer)**

Word Access

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	–	–	–	–	–	–	–	–	VW07	VW06	VW05	VW04	VW03	VW02	VW01	VW00
RD	0	0	0	0	0	0	0	0	[illegible]							
WR	0	0	0	0	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

The Vdot size register can be read before graphics and numeric operations, but is decremented during graphics and numeric operations. When these operation are complete, the Vdot size value becomes 0. Therefore, for graphics and numeric operations, resetting this value is essential.

VW00~08 : This indicates the number of vertical dots to write.
The location for writing is determined by the image buffer start address and the image buffer offset.

● **$FF8066 : Trace vector base address(TVBA)** (X start, Y start, Δx, Δy, Table base address)

Write Only **Word Access**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	–
RD	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0

Coordinate conversion(graphics and numeric operations) are begun when this location is set. When these operations complete, a LEVEL1 interrupt will be generated.

Start position, ΔX, ΔY → Stamp map → Stamp generator → Image buffer table

● **The value to be set to the pointer of TVBA**

	MSB D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0
Xst	X12	X11	X10	X9	X8	X7	X6	X5	X4	X3	X2	X1	X0	PX1	PX2	PX3
Yst	Y12	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	PY1	PY2	PY3
Δx	+/-	Δx3	Δx2	Δx1	Δx0	ΔPx1	ΔPx2	ΔPx3	ΔPx4	ΔPx5	ΔPx6	ΔPx7	ΔPx8	ΔPx9	ΔPx10	ΔPx11
Δy	+/-	Δy3	Δy2	Δy1	Δy0	ΔPy1	ΔPy2	ΔPy3	ΔPy4	ΔPy5	ΔPy6	ΔPy7	ΔPy8	ΔPy9	ΔPy10	ΔPy11

→ Data for 1 line

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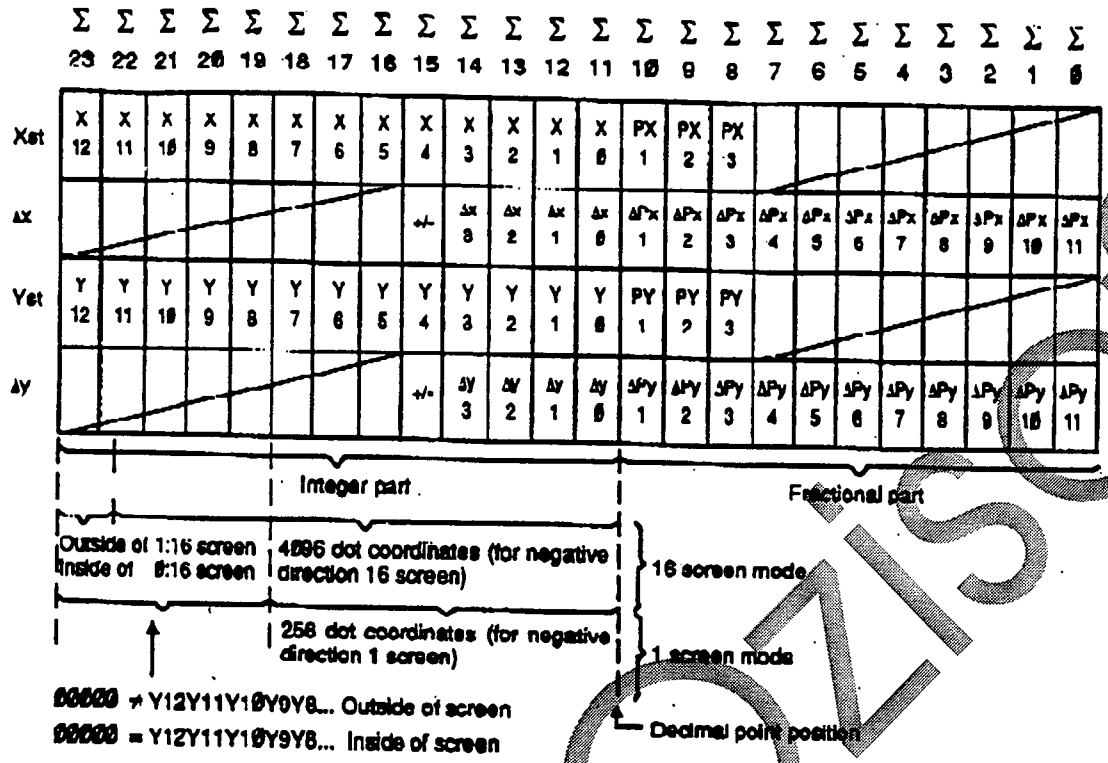

00000 ≠ Y12Y11Y10Y0Y8... Outside of screen

00000 = Y12Y11Y10Y9Y8... Inside of screen

※Two compensatory methods are used to compute ΔX and ΔY.

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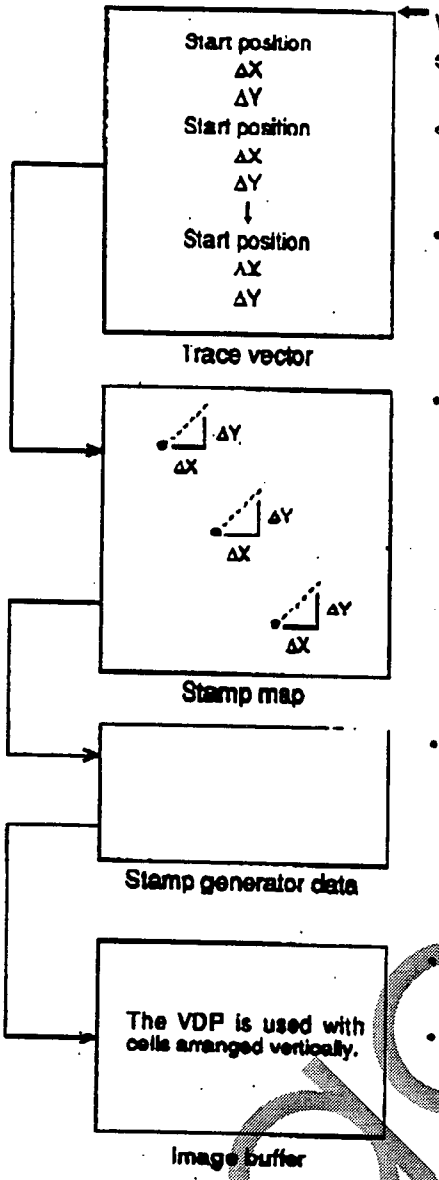

When this trace vector address is set, coordinate conversion is started.

- The ΔX and ΔY, start positions in this area are calculated by the SUB-CPU.
- The line number to be converted has V dot size($FF8064)
- Beginning from the start position, the trace vector samples the line numbers for Hdot size ($FF8062).
- The characters which are sampled by the Stamp map are displayed.
- The collected characters are stored in the MD's VRAM image.
- When the last 1 dot is written, an INT LEVEL 1 is generated.

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● Stamp data organization

When a 16x16 dot size is stamped

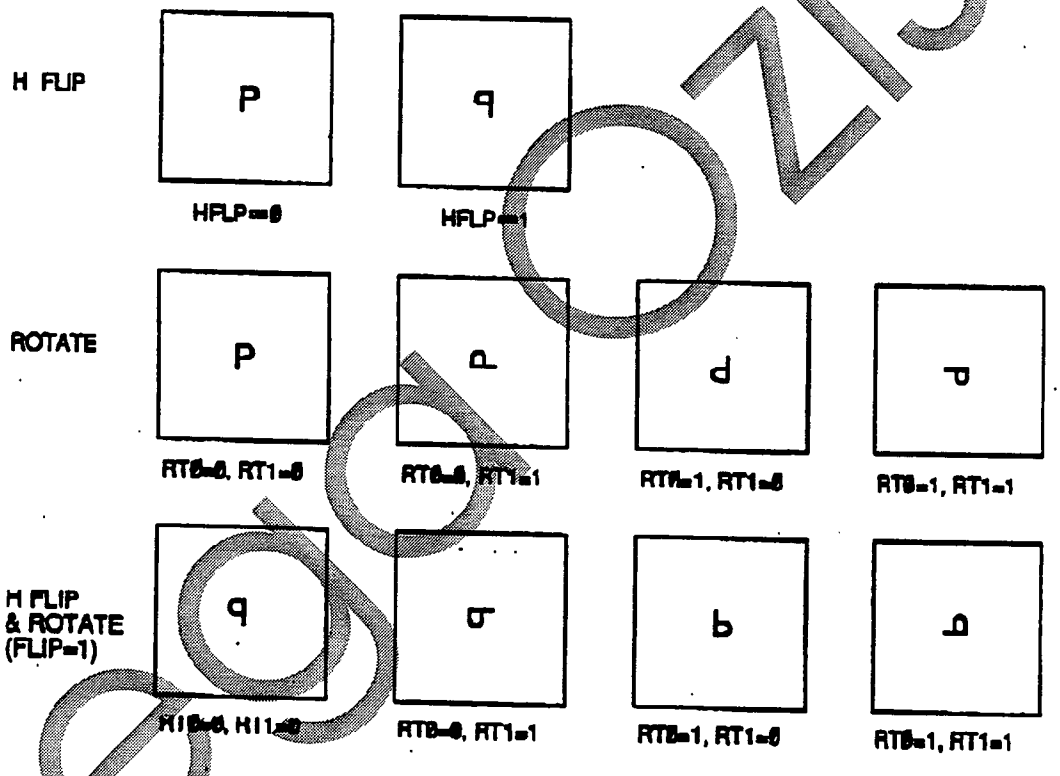
H F L P	RT 1	RT 0	0	0	SNO A	SNO 9	SNO 8	SNO 7	SNO 6	SNO 5	SNO 4	SNO 3	SNO 2	SNO 1	SNO 0

Stamp No.

When a 32x32 dot size is stamped

H F L P	RT 1	RT 0	0	0	SNO A	SNO 9	SNO 8	SNO 7	SNO 6	SNO 5	SNO 4	SNO 3	SNO 2	0	0

Stamp No.



• Stamp No.

- For a 16x16 dot size... up to 2048 of stamp No. can be assigned SNO A~0.
- For a 32x32 dot size... up to 512 of stamp No. can be assigned by SNO A~2.

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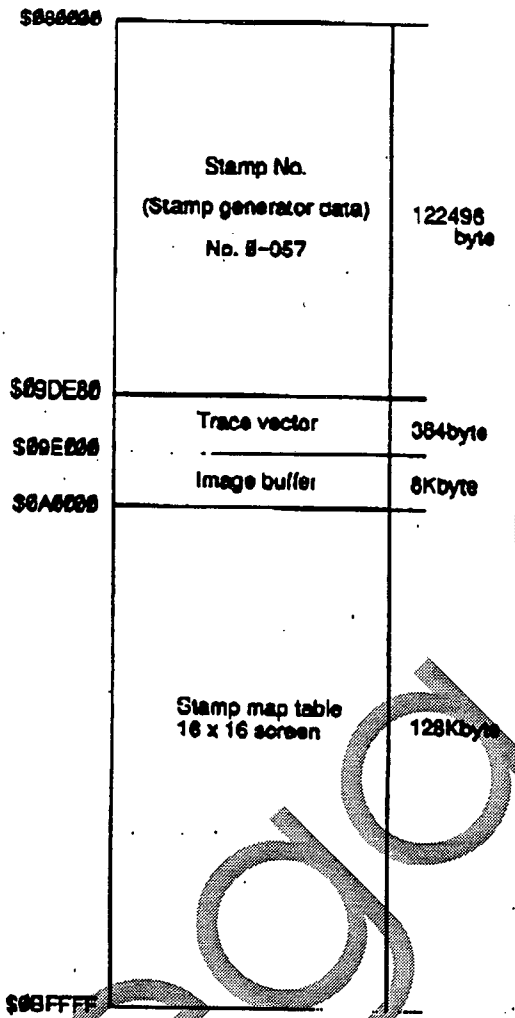
● Examples of mapping in the rotation mode

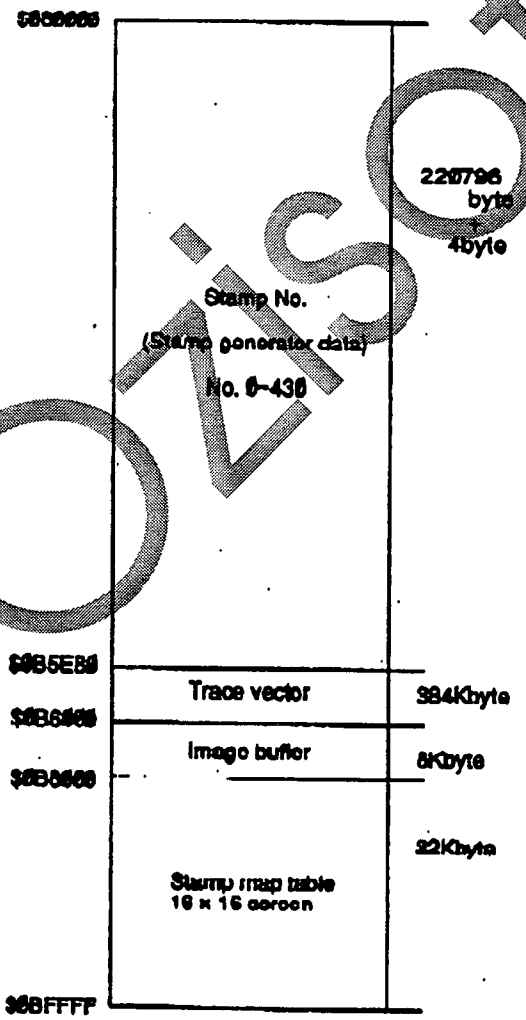
16x16 dot stamp
16x16 screen mode
Image buffer(for 6x30 cell)
Trace vector table(for 6x8 line)

■ When the SUB-CPU is operating



32x32 dot stamp
16x16 screen mode
Image buffer(for 6x38 cell)
Trace vector table(for 6x8 line)

■ When the SUB-CPU is operating



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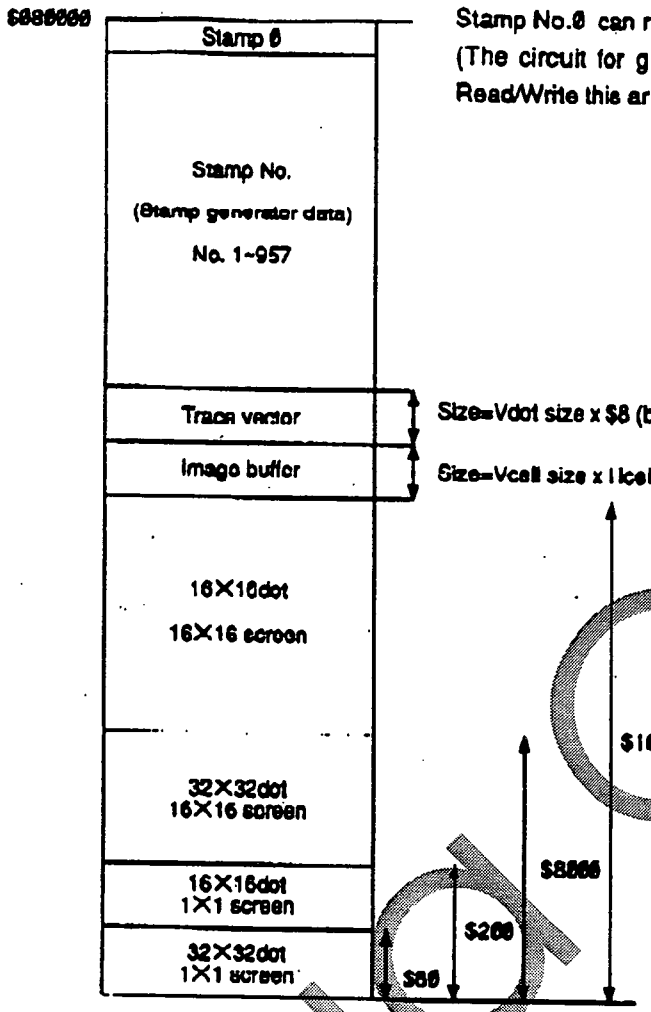
■ When the SUB-CPU is operating



Stamp No.0 can not be used, but operates as ordinary RAM. (The circuit for graphics and numeric operations does not Read/Write this area.)

Stamp No.0 on the Stamp map indicates the character ALL0.

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Blank Page

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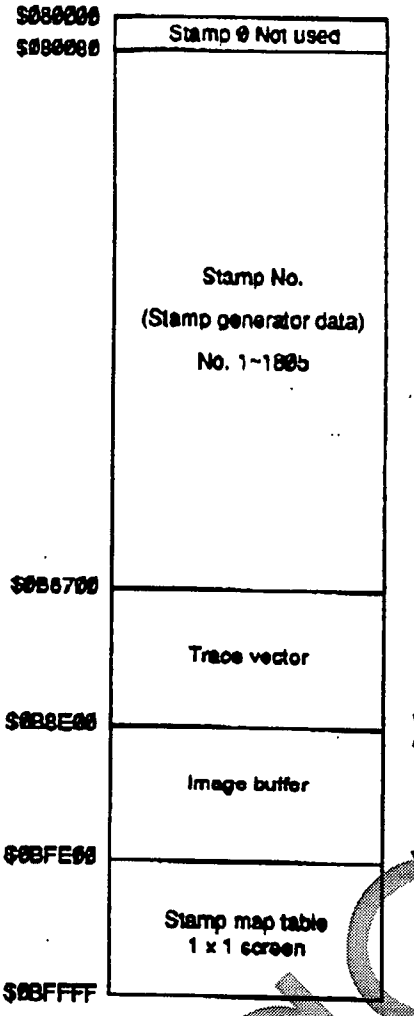
16 x16 dot
1x1 screen mode
Image buffer(for 32x28 cell)



Stamp No.0 can not be used. but operates as ordinary RAM.

For 224 lines(8x224 bytes)

For 32x28 cell(32x28x$20bytes)

When '0', the Stamp map No. signifies that there is no character (0FILL is used in this case).

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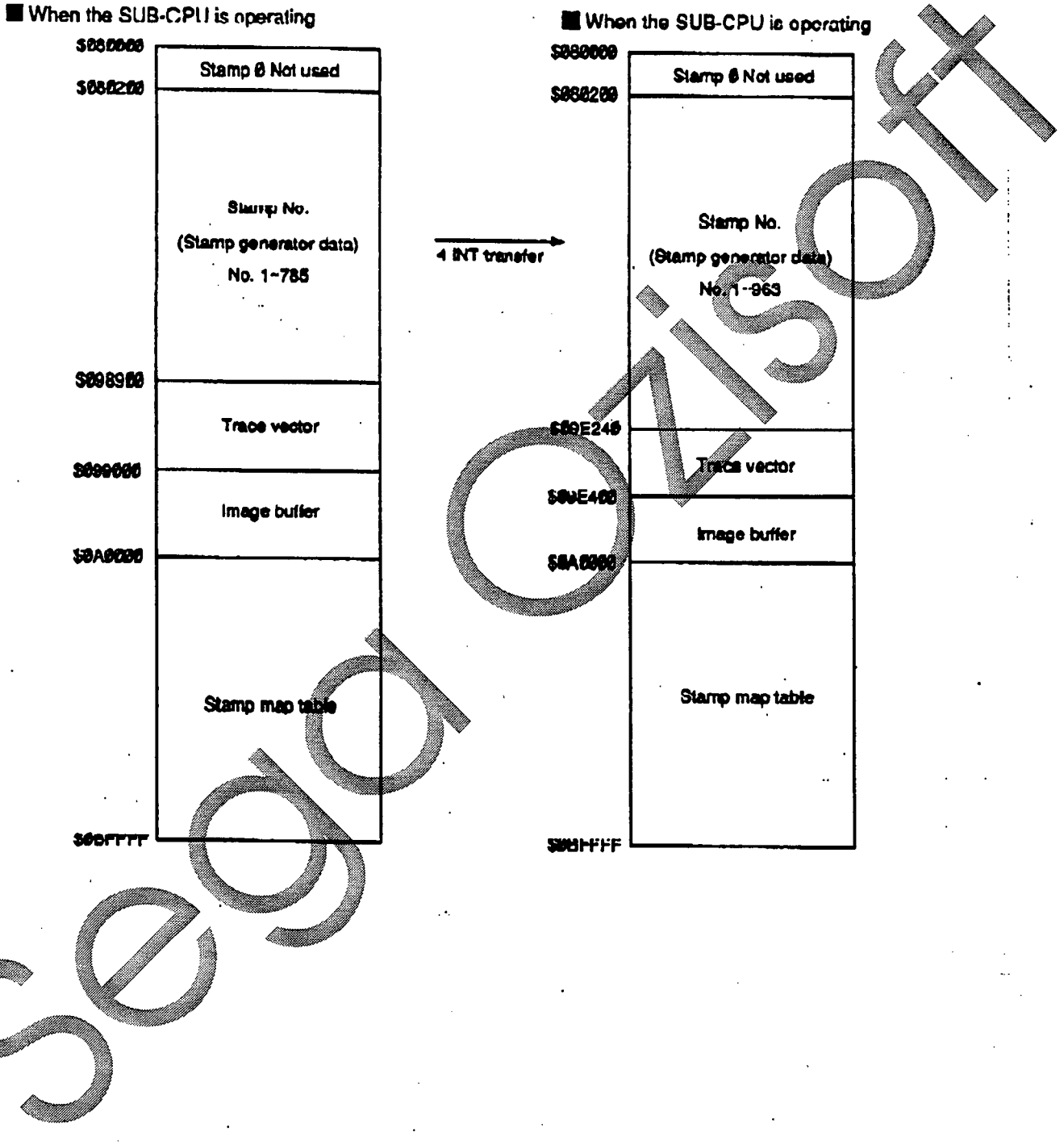
32x32 dot
16x16 screen mode
Image buffer(for 32x28 cell)



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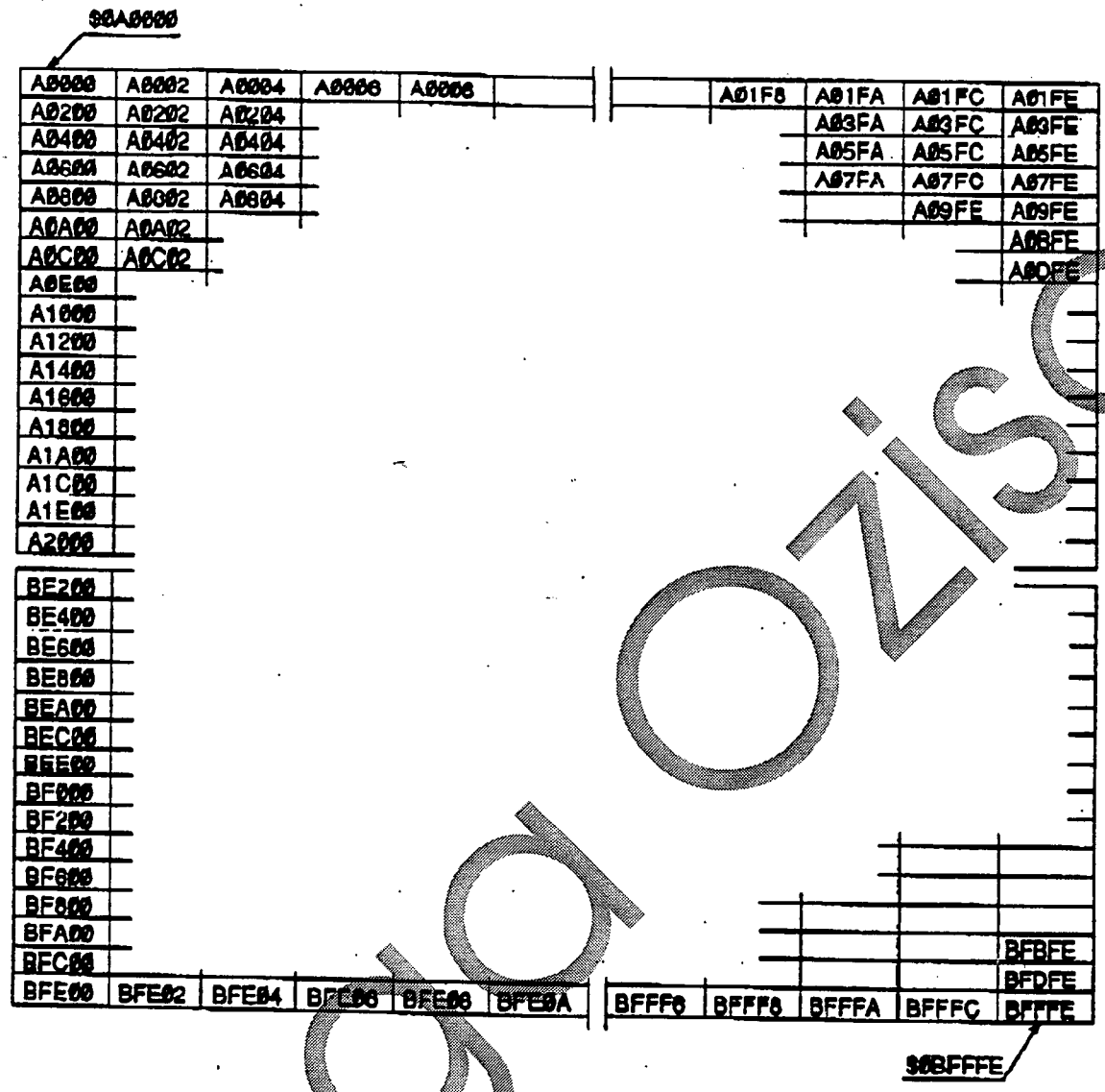
- **The location of a Stamp map base address when a 16x16 screen, 16x16 dot size stamped.**



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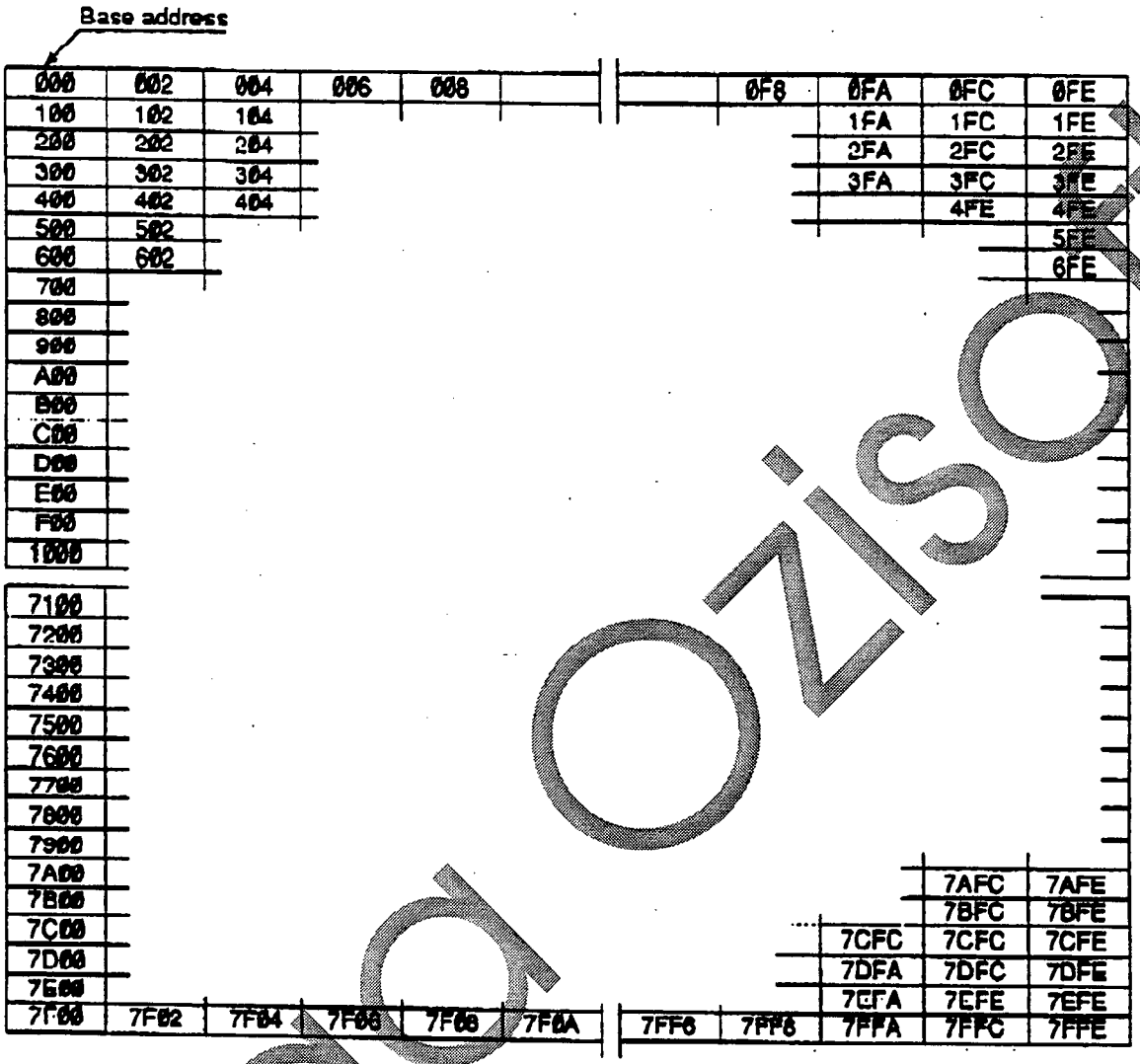
● **The Stamp map base address when a 16x16 screen, 32x32 dot size is stamped.**



• Stamp map base address

$080000
$090000
$098000
$0A0000
$0A8000
$0B0000
$0B8000

The Stamp map can use the 8 banks on the left. However, in practice, some space should be left free for defining stamp data.

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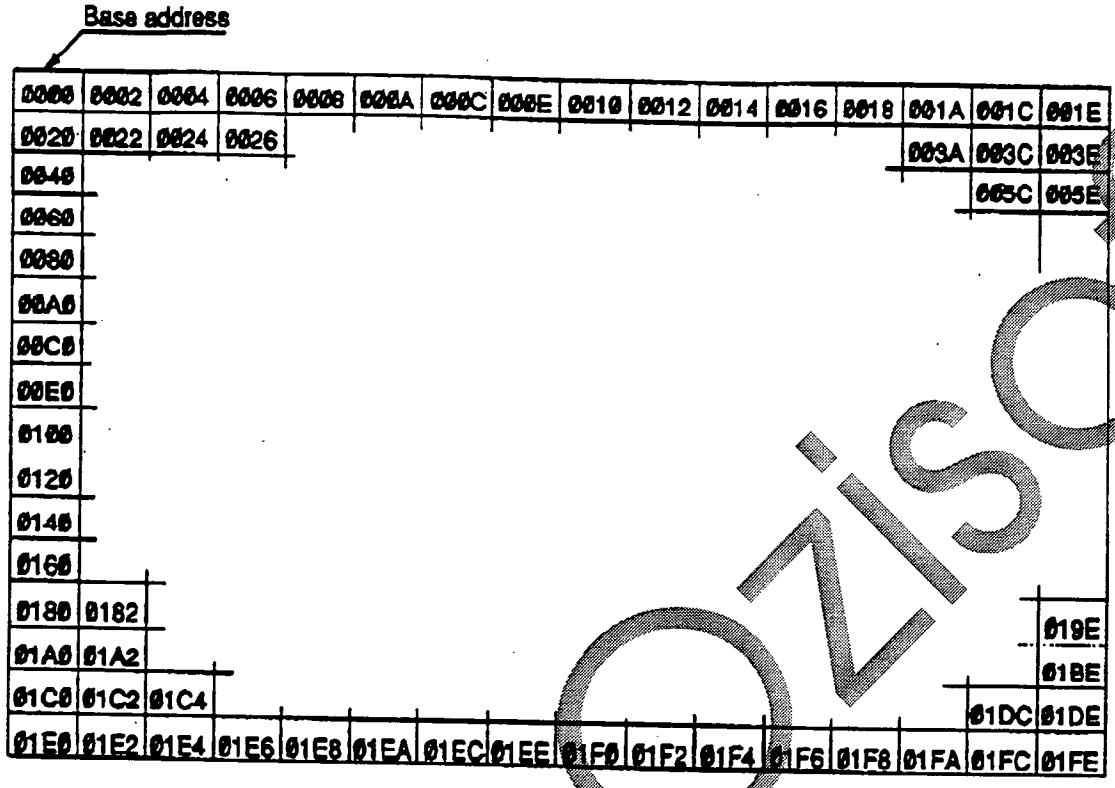
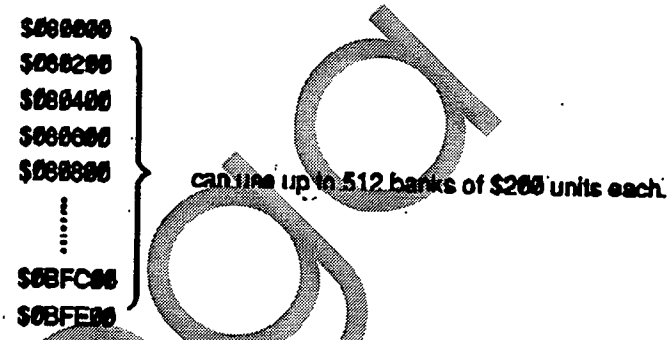
● **The Stamp map base address when a 1x1 screen, 16x16 dot size is stamped.**



• Stamp map base address



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● **The Stamp map base address when a 1x1 screen, 32x32 dot size is stamped.**

0000	0002	0004	0006	0008	000A	000C	000E
0010	0012	0014	0016	0018	001A	001C	001E
0020	0022	0024	0026	0028	002A	002C	002E
0030							003E
0040							004E
0050							005E
0060							006E
0070	0072	0074	0076	0078	007A	007C	007E

• Stamp map base address

$000000
$000080
$000100
$000180
$000200
⋮
$0BFF00
$0BFF80

} can use up to 2048 banks of $80 units each.

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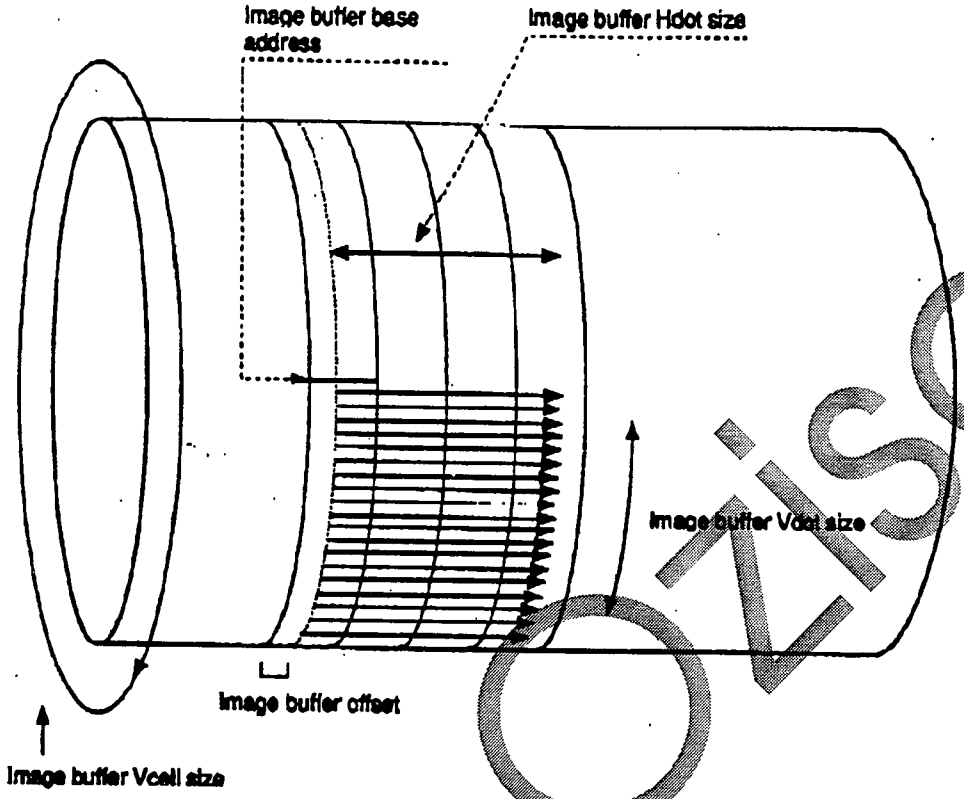
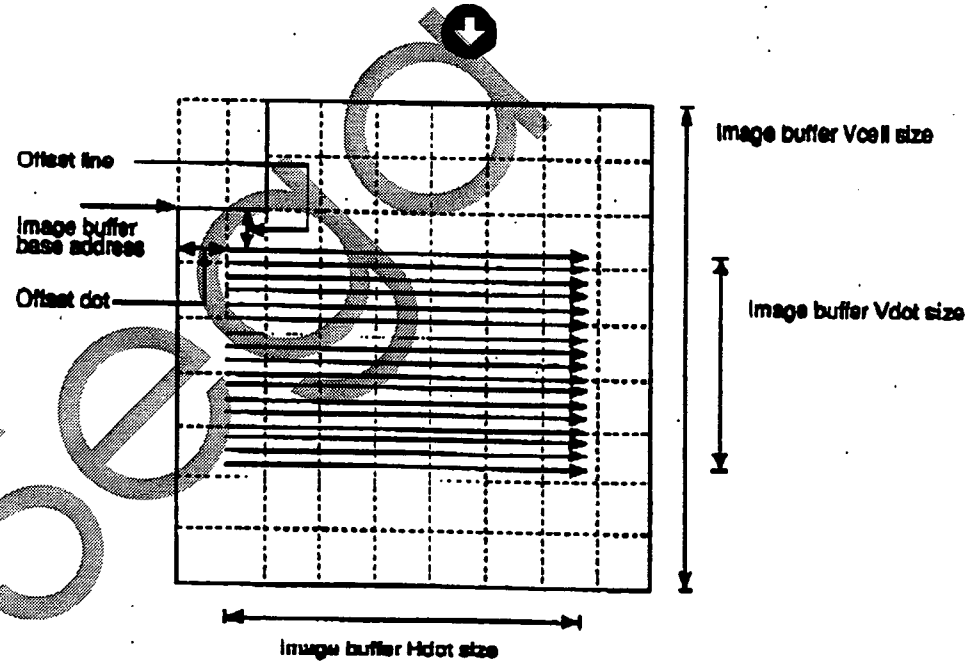
● **Image buffer basic concept**





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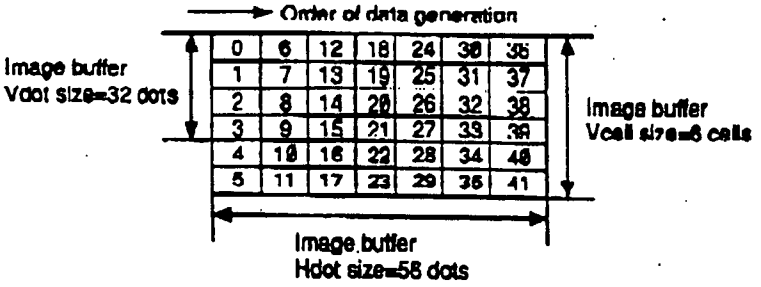
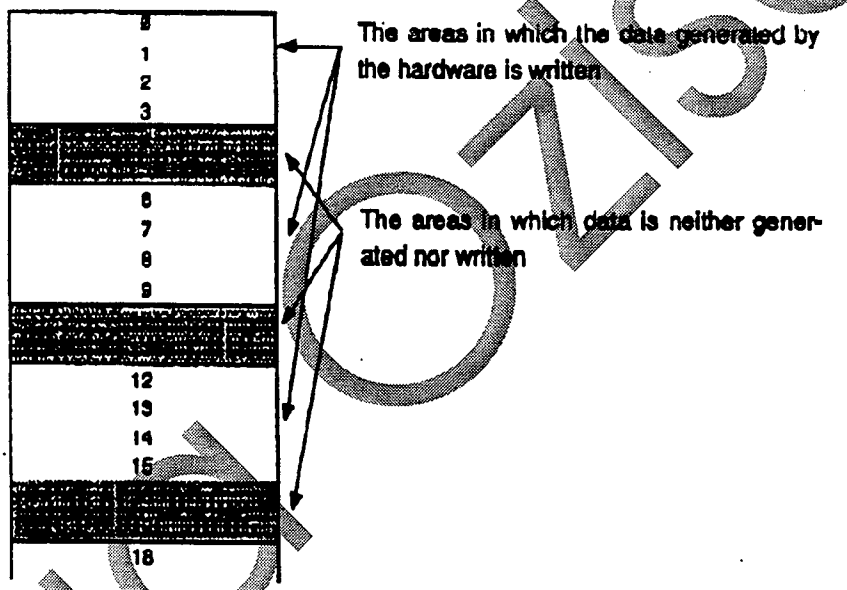
● Image buffer conceptual figure



Buffer size is determined by Vcell size and Hdot size, but the size of the actual data area used in practice is determined by Vdot size and Hdot size.

● Image buffer map



Data is generated line by line as shown in the figure above. For example, first, the first line of cell No.6. Second, the first line of cell No.. 8. Third, ... Graphics operations complete when the data generation of the eighth line of cell No. 99 is complete.

■ Graphics operation time(1 clock =80ns)

- The minimum clock number needed to complete a graphics operation
  = Vdot size(13-2(3.and.offset)-9[2.SHR.(H dot+offset-1)]]
- SUB-CPU access clock number = access times to the 2M RAMx3 (In the case where the SUB-CPU accesses the 2M RAM during graphics work)
- DMA clock number = access times to the 2M RAMx3 (In the case where the DMA accesses the 2M RAM during graphics work)
- Refresh clock number= 3[INT(minimum clock number to complete graphics operation+SUB-CPU access clock number+DMA clock number/192)]
- Maximum clock number needed to complete graphics operation
  = minimum clock number to complete operations+SUB-CPU access clock number+DMA clock number+refresh clock number

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● Offset

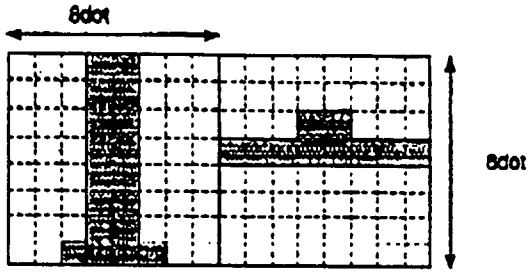


Fig.1

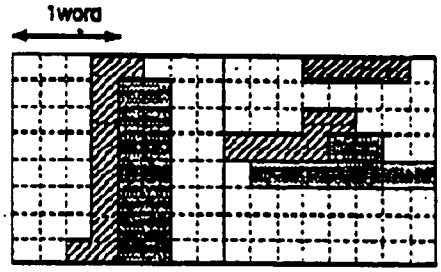


Fig.2

When the line and dot in Fig.1 are shifted by 1 dot, the previous data in the parts indicated by ▒ is kept unchanged regardless of the priority. The parts indicated by ▨ are formed from the data pushed out by adjacent cells. Fig.2 indicates the case in which cell size is 1 cell. In changing offset, therefore, Vcell size must be set larger than the actual cell size. (If Hdot size is 8 or less, however, there is no problem.)

● Priority

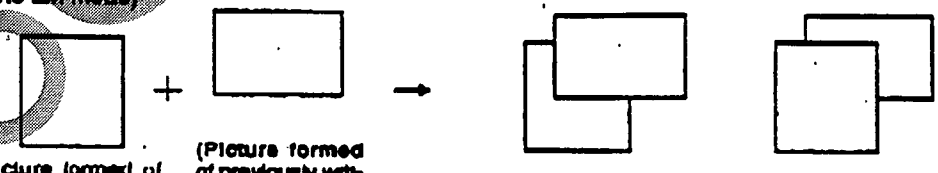
- When the WORD-RAM is in the 2M mode, priority is applied to the data written to the image buffer by graphics operations. Therefore, when the CPU writes in the WORD-RAM, the WORD-RAM works as ordinary RAM.

- When the WORD-RAM is in the 1M mode, priority is applied to the data written to a dot image area.

(In the 1M mode)
In the following example, $0C0000 contains the original data '9A', and $080000 contains the write data. The contents of $0C0000 will appear as follows after the write:

(Write Data)	(Normal)	(Overwrite)	(Underwrite)
$0507	57	57	5A
$0B0B	B0	BA	BA

In the Overwrite mode, only the '0' portion of the new data is not overwritten onto the corresponding portion of the previous data. In the Underwrite mode, new data is written only to the '0' portion of the previous data.
(In the 2M mode)



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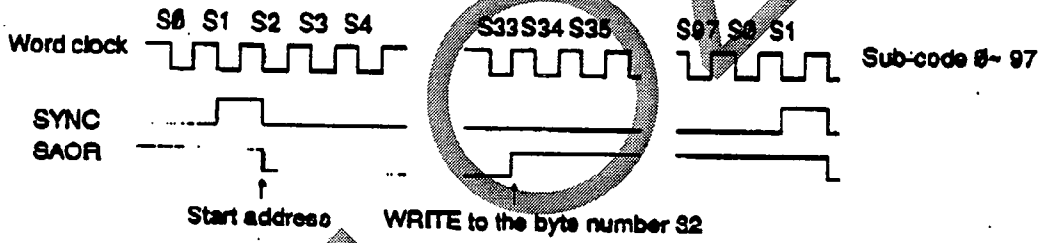
3-9 SUB-CODE

Sub-code are generally controlled by BIOS and can not be accessed.

● $FF8068 : Sub-code address

	MSB F	E	D	C	B	A	9	8							LSB 0
	-	-	—	—	—	—	—	—	SA6	SA5	SA4	SA3	SA2	SA1	SAOR
RD	0	0	0	0	0	0	0	0	STA6	STA5	STA4	STA3	STA2	STA1	0
WR	—	—	—	—	—	—	—	—							—

STA1~6 Sub-code top address
SAOR Sub-code address overrun
Set to '1' when writing in 32 bytes.
This is cleared by SYNC



● $FF806A~$FF80FE : Reserved by the system

● $FF8100~$FF817E : Sub-code buffer area of 64 words x 15 bits

● $FF8180~$FF81FE : Image of Sub-code buffer area

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4 MAIN-CPU SIDE REGISTERS

4-1 INITIALIZATION

● $A12000 : BUSREQ, RESET

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	LSB 1	0
	IEN2	—	—	—	—	—	—	IFL2	—	—	—	—	—	—	SBRQ	SRES
RD	0/1	0	0	0	0	0	0	0/1	0	0	0	0	0	0		
WR	0	0	0	0	0	0	0	0/1	0	0	0	0	0	0		

※ bset and beir can not be used.

SRES : SUB-CPU RESET
In the Write mode, '0'=RESET / '1'=RUN
In the Read mode, '0'=reset in process / '1'=RESET finished

SBRQ : SUB-CPU BUS request
In the Write mode, '0'=cancel BUS request / '1'=BUS request
In the Read mode, '0'=SUB-CPU is operating / '1'=BUS request satisfied

IFL2 : This gives the SUB-CPU INTERRUPT LEVEL2.
In the Write mode, '0' is not used / '1' INT Level 2 is generated (When IEN2=1)
In the Read mode, '0'= In the process of doing a LEVEL2 interrupt. / '1'=Level 2 is not treated yet.

IEN2 : The mask state of INT LEVEL2 on the SUB-CPU side
'0' : Mask, '1' : Enable

● Timing for initializing the interior of the Gate Array<Forced Reset>

When the MAIN-CPU executes a specific command pattern, the interior of the Gate Array is initialized.

- Execution command

```
MOVE.W #$FF00, $A12002
MOVE.B #$03, $A12001
MOVE.B #$02, $A12001
MOVE.B #$00, $A12001
```

※Attention must be paid to address and size.

NOTE Remember that a <Forced Reset> is not executed by command patterns other than those mentioned above.

※System areas which can not be initialized /All the registers belonging to the MAIN-CPU.

- Registers of MAIN-CPU

$A12000=XX00 The setting is completed by the BUSREQ and RESET, H-INT commands.
$A12002=FF00 The setting is completed by the STATUS REGISTER command.
$A12004 (H-INT)
$A12006 (STATUS REGISTER)
:
$A1200E (COMMUNICATION STATUS)

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※ Initialized areas (All the functions other than the MAIN-CPU registers are reset.)

Registers and functions connected to the SUB-CPU
Refresh/Timer/Stop watch/DMA/Rotation/Interrupt/CDD communication/Sub-code reception/Fader, etc.

● $A12002 : Memory mode/Write protect

	MSB							LSB						
	[illegible]							[illegible]	5	4	3	2	1	0
WR	WP7	WP6	WP5	WP4	WP3	WP2	WP1	WP0	-	-	-	MODE	DMNA	RET
RD	[illegible]							[illegible]	0	0	0	0/1	0/1	0/1
WR	[illegible]							[illegible]	0	0	0	0	0/1	0

WP0~7 : The address range $0 to $1FDFF of the SUB-CPU is protected in multiples of $200. If a WP bit field is set to '1' than the corresponding $200 element range is protected.

MODE : In the READ mode '0'=2M mode/'1'=1M/1M mode

DMNA : Declaration of MAIN-CPU No Access on the ram.
When MODE='0', (2M mode). For the details, see the SUB-CPU side.
In the Write mode '0' = no significance/'1' returns the 2M RAM to the SUB-CPU
In the Read mode '0' = In the process of returning the 2M RAM
'1' = Completion of the return of the 2M RAM to the SUB-CPU

When MODE ='1'(1M mode)
In the Write mode '0' = Swap request
'1' = No significance
In the Read mode '0' = Swap completion/
'1' = In the process of requesting a swap

BK0,1 : When accessing the PRG-RAM(4M bits) by the MAIN-CPU, an area of only 1M bits is allocated on the MAIN side.
Therefore, the PRG-RAM is accessed through 4 BANKs. (When SBRQ=1 or SRES=0)

RET : RET bit
When MODE='0'(2M mode) For the details, see the SUB-CPU
In the Read mode, '0' = the SUB-CPU is in the process of returning the 2M RAM,
'1' = the 2M RAM has been returned to the MAIN-CPU.

MODE='1'
In the Read mode, '0' = the 1M of WORD-RAM 0 is attached to the MAIN-CPU, and the 1M of WORD-RAM 1 is attached to the SUB-CPU.
'1' = WORD-RAM 0 is attached to the SUB-CPU and WORD-RAM 1 to the MAIN-CPU.

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● $A12006 : H-INT vector (level 4) **Word Access**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	HIBF	HIBE	HIBD	HIBC	HIBB	HIBA	HIB9	HIB8	HIB7	HIB6	HIB5	HIB4	HIB3	HIB2	HIB1	HIB0
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

When H-INT is generated in the MAIN-CPU, the addresses placed on $70 and $72 are ignored and a jump address is formed using $70 for the high order portion of the address and HIR15-0 for the low order portion of the address. After a reset, $A12006 is set to -1.

4-2 CDC

● $A12004 : CDC mode

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	EDT	DSR	–	–	–	DD2	DD1	DD0	–	–	–	–	–	–	–	–
RD	0/1	0/1	0	0	0	0/1	0/1	0/1	0	0	0	0	0	0	0	0
WR	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

DD0-2 : Device Destination
Refer to the SUB-CPU register $FF8004

EDT : End of Data Transfer
This indicates that all data has been transferred from the CDC.

DSR : Data Set Ready
This indicates that the data from the CDC has been put into the $A12008 register.

● $A12008 : CDC host data(16 bits) **Word Access**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	HD15	HD14	HD13	HD12	HD11	HD10	HD09	HD08	HD07	HD06	HD05	HD04	HD03	HD02	HD01	HD00
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

HD00-15 : CDC read data, bits 00-15
Two bytes from the CDC are accumulated in the host data register and then transfered to the MAIN-CPU or SUB-CPU. After the data in HD00-15 has been read, the CDC transfers the next 2 bytes of data into this register.

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● $A1200A : Reserved by the system

4-3 COMMUNICATION

● $A1200C : Stop watch **Word Access**

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	–	–	–	–	TD11	TD10	TD09	TD08	TD07	TD06	TD05	TD04	TD03	TD02	TD01	TD00
RD	0	0	0	0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–

TD00~11:Timer Data

This timer counts from 0 to 4095, one count taking 30.72µs. $FF800C of the SUB-CPU clears the timer.

● $A1200E : Communication flag

	MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
	CFM7	CFM6	CFM5	CFM4	CFM3	CFM2	CFM1	CFM0	CFS7	CFS6	CFS5	CFS4	CFS3	CFS2	CFS1	CFS0
RD	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
WR	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0	0	0	0	0	0	0	0

CFM0~7 :Communication flag MAIN-CPU

CFS0~7 : Communication flag SUB-CPU

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● $A12010~$A1201E : Communication command, 8 Words **Read/Write**

MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
Communication command 0															
Communication command 1															
Communication command 2															
Communication command 3															
Communication command 4															
Communication command 5															
Communication command 6															
Communication command 7															

● $A12020~$A1202E : Communication status, 8 Words **Read Only**

MSB F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	LSB 0
Communication status 0															
Communication status 1															
Communication status 2															
Communication status 3															
Communication status 4															
Communication status 5															
Communication status 6															
Communication status 7															

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SUPPLEMENTS

1. Precautions in using DMA from WORD-RAM to V-RAM, C-RAM and VS-RAM

● **Precautions in using DMA of the VDP of the MEGA-DRIVE to transfer data from WORD-RAM on the MEGA-CD to V-RAM, C-RAM and VS-RAM.**

■ **WORD-RAM mode**

- In the 2M mode...the WORD-RAM must be switched to the MAIN side at the time of DMA.
- In the 1M/1M mode...use the RAM installed on the MAIN side as the source for the transfer.

■ **Regarding the action at the time of DMA**

- In the case where the 68000 CPU on the MAIN side access the WORD-RAM, ordinary Read/Write is possible.
- In the case where the VDP accesses the WORD-RAM by DMA, the data read from the WORD-RAM will be output with a one cycle delay, because VDP read-out is slow and the time from the start of read-out to the output of the data is short.

※Solutions※

- Set the source address to one word greater than the original address.
- Since the top word of an address might be destroyed due to certain restrictions (See p.28 in MEGA DRIVE software Development Manual), rewrite 2 words including the top word after the DMA transfer.

※For a SAMPLE program, see p.63.

2. Restrictions in using DMA from the MEGA-DRIVE side to the MEGA-CD side

■ **Regarding PRG-RAM**

- Never access the PRG-RAM from the MAIN-CPU. (This is equivalent to executing a HALT on the SUB-CPU.)

■ **Regarding WORD-RAM**

- Do not put the DMA transfer program for VDP onto WORD-RAM.
  ※Put the program in the WORD-RAM.

■ **Be sure to observe the restrictions and PRECAUTIONS described in the [MEGA DRIVE SOFTWARE DEVELOPMENT MANUAL].**

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3. Other precautions

1. After changing the mode of WORD-RAM or swapping WORD-RAM, make sure that the mode is changed completely and that the WORD-RAM actually exists before accessing WORD-RAM.

2. In the CDC mode ($FF8004) register, all bits are set to '0' when they are initialized. Therfore, define the destination in order to read the CDC data.

3. When turning On/Off sounding of the PCM sound source, wait for more than 30 µs before accessing PCM RAM.

4. Do not apply following to Z80:

   1. Accessing the WORD-RAM.
   2. Accessing the PRG-RAM.
   3. Accessing all the area of 68000 CPU side.

   However, Z80 can use its 8K-RAM.

5. READOUT-TIME of the productive model DISC is the same value of that 1 frame is added to the READOUT-TIME of the DISC created by WRITEONCE. Therefore, do not make a program using READOUT-TIME.

6. Do not change the setting of BIOS without permission.

7. Do not call BIOS related to LED. (except for developing.)

8. Since privileged instructions are used for BIOS, do not use the User mode for SUB-CPU. When using User mode for MAIN-CPU, do not call the BIOS that uses privilege instructions.

9. Never write on the boot area 6000000 ~ 6000080 on SUB-CPU.

10. During graphic operations, do not change WORD-RAM from SUB-CPU to MAIN-CPU.

11. Do not mask LEVEL 4, 5 and 6 incorrectly.

12. Although the speed for switching the mode from pause to stand-by is changable, keep the data between 4500 ($1194) ~ 65534 ($FFFE) (1 min ~ 15 min).

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```
*ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc*
*  Word Ram to Vram copy by DMA :Included VDP. PRG of BOOT-ROM Sample Disc      *
*-------------------------------------------------------------------------------*
*       input   d0. l = vram destination address code                           *
*               d1. l = ram source address                                      *
*               d2. w - Length (word)                                           *
*       output  nothing                                                         *
*       use     d3, a6                                                          *
*ccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccccc*
lh=length high
ll=length low
sh=source address high (sa17~sa23)
sm=source address middle (sa9~sa16)
sl=source address low(sa1~sa8)

wmov-dma:
                pushl   a1                      * For MACRO, see MACRO.MAC in BOOT-ROM
                                                  SAMPLE DISC.
                movea.l d1, a1
                addq.l  #2, d1                  *offset adjust 1 word shift
                asr.l   #1, d1                  */2

                lea     vdp_cmd, a6
                move.w  #$8f02, (a6)            *change auto-inclirnent
                move.w  rg1_dat, d3
                bset    #4, d3
                move.w  d3, (a6)                *DMA si
                *
                move.l  # ($86+20) *$10000, d3  *d3=$00910000
                move.w  d2, d3                  *set lg8~lg15
                lsl.l   #8, d3                  *d3=$94lhl00
                move.w  # ($86+19) *$100, d3    *d3=$94lh9300
                move.b  d2, d3                  *set lg0~lg7 d4=$94lh93ll
                move.l  d3, (a6)                *set length to vdp register
                *
                move.l  # ($86+22) *$10000, d3  *d3=$00960000
                move.w  d1, d3                  *set sa8~sa15
                lsl.l   #8, d3                  *d3=$96smsl
                move.w  # ($86+21) *$100, d3    *d3=$96sm9500
                move.b  d1, d3                  *d3=$96sm95sl
                move.l  d3, (a6)                *Set source ram address
                *
                swap    d1
                move.w  # ($86+23) *$100, d3    *d3=$9700
                move.b  d1, d3                  *d3=$97sh
                move.w  d3, (a6)                *set Vreg #23
                *
                ori.l   #$40000080, d0          *set DMA code
                swap    d0
                move.w  d0, (a6)                *set vram address low
                swap    d0
                move.w  d0, -(sp)
                move.w  (sp)+, (a6)             *set Vram address high
                *
                move.w  rg1_dat, (a6)           *DMA di

                andi.w  #$ff7f, d0              *DMA code --- write code
                move.l  d0, (a6)                *set top vram address
                move.l  (a1), -4(a6)            *write 1st & 2nd data
                move.w  rg15_dat, (a6)
                popl    a1
                rts
```

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MEGA-CD HARDWARE MANUAL

PCM SOUND SOURCE

Sega Oasoft

SEGA ENTERPRISES, LTD.

VER. 1.0 10/14/91

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PCM SOUND SOURCE (RF5C164)

1 OVERVIEW OF THE PRODUCT

The RF5C164 is a PCM sound source IC which is manufactured by the 1.5μ silicon gate CMOS process. Included inside the IC are the DCO (digital control oscillator), the DCA (digital control amplifier), and other functions. A PCM sound source system can be configured by connecting an external wave (form) data memory (Pseudo SRAM, SRAM or mask ROM) and an external D/A converter, and using a microcomputer to control the system. When compared with other methods, the PCM sound source method has the following advantages:

1. Natural tones can be produced;
2. Software to produce sounds is more easily developed.

● Features:

- PCM sound source method.
- Number of channels : 8 channels.
- Clock frequency of the source : Up to 12 MHz.
- Sampling frequency : 31.9 KHz.
- Wave data width : 8 bits.
- Number of wave words : Any.
- Wave memory space : 1. Up to 64 Kbytes when RAM is used.
  2. Up to 128 Kbytes when ROM is used.
- Envelope data width : 8 bits.
- L/R stereo output at any fixed level (16 levels each for both L and R).
- Can be interfaced with a general-purpose 8-bit CPU.
- Package : Flat 86-pin package.
- Interface with the wave memory can be directly connected to a
  256K (32Kx8) Pseudo SRAM.
  256K (32Kx8) MASK ROM.
  256K (32Kx8) SRAM.
  1M MASK ROM.
- Interface with the D/A converter.
  Can be directly connected to the digital-audio 16-bit D/A converter (Sanyo LC7881).
- Can read out a specific address in real-time for accessing the wave RAM (when RAMAX is not used).

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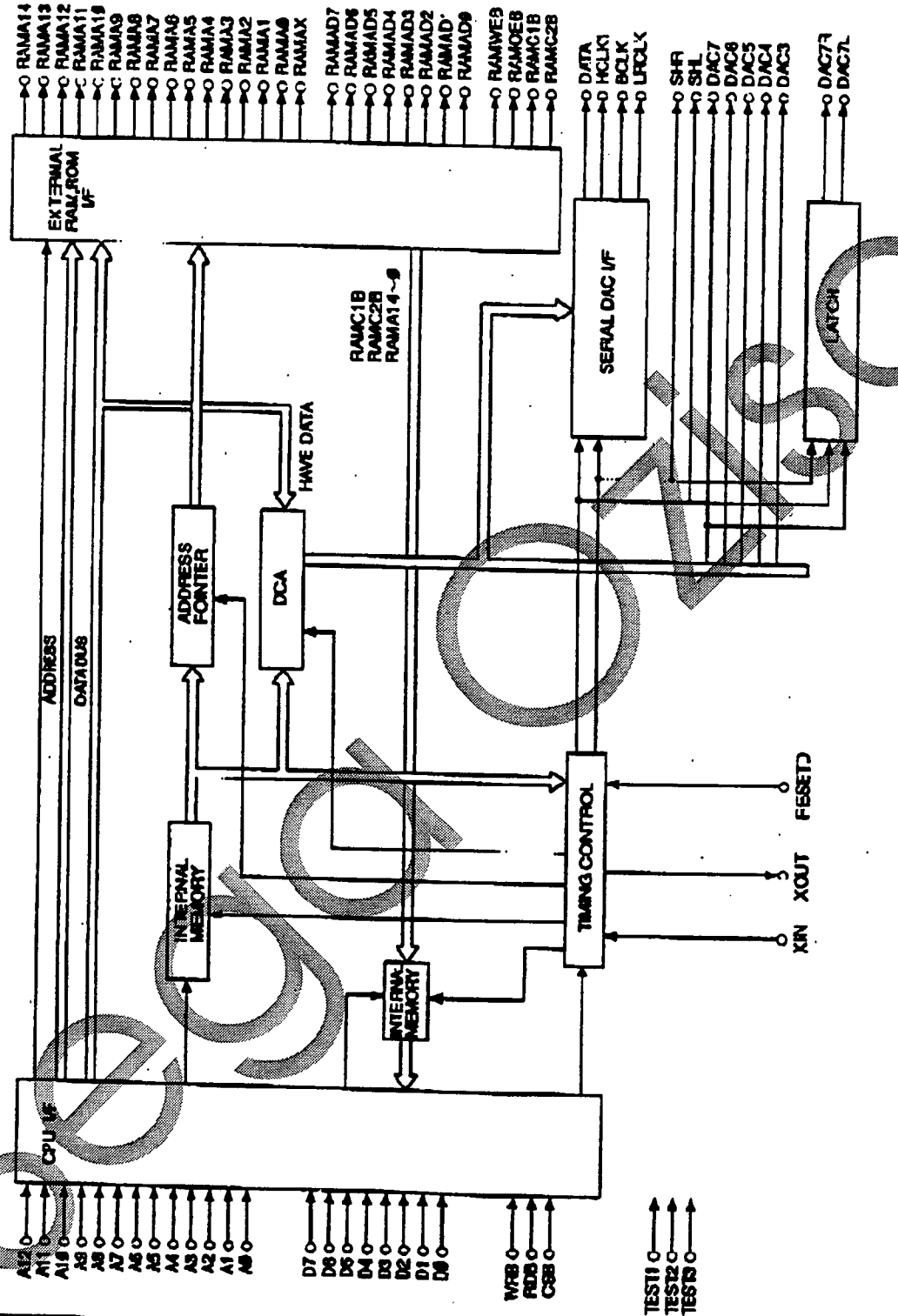
2 BLOCK DIAGRAM



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3 DESCRIPTION OF PINS

PIN	INPUT/OUTPUT	FUNCTION
A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0	I	Address signals from the microcomputer.
D7 D6 D5 D4 D3 D2 D1 D0	I/O	Data bus signals from or to the microcomputer
CSB	I	Chip select signals from the microcomputer.
RDB	I	Read signals from the microcomputer.
WRB	I	Write signals from the microcomputer.
RAMAD7 RAMAD6 RAMAD5 RAMAD4 RAMAD3 RAMAD2 RAMAD1 RAMAD0	I/O	Multiplexed signals of the lower-address/data from and to the SRAM when connected to the Pseudo SRAM; data input siganals from the MROM when connected to the MROM; data bus signals from and to the SRAM when connected to the SRAM.

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PIN	INPUT/OUTPUT	FUNCTION
RAMA14 RAMA13 RAMA12 RAMA11 RAMA10 RAMA9 RAMA8	O O O O O O O	Upper-address signals of the SRAM & MROM.
RAMA7 RAMA6 RAMA5 RAMA4 RAMA3 RAMA2 RAMA1 RAMA0	O O O O O O O O	Lower-address signals of the SRAM & MROM.
RAMAX	O	Lowest-address signals of the MROM.
RAMC2B	O	Upper 32Kbytes SRAM & MROM select signals.
RAMC1B	O	Lower 32Kbytes SRAM & MROM select signals.
RAMWEB	O	Pseudo SRAM & SRAM write signals.
RAMOEB	O	Pseudo SRAM & SRAM & MROM read signals.
DAC7 DAC6 DAC5 DAC4 DAC3	O O O O O	Multiplexed signals of output "R" data/"L" data to the parallel DAC.
SHL	O	"L" data sample/hold signals for DAC7 to DAC3.
SHR	O	"R" data sample/hold signals for DAC7 to DAC3.
DAC7R	O	Sample/hold signals of DAC7 output with SHR.
DAC7L	O	Sample/hold signals of DAC7 output with SHL.
WCLK1	O	Word clock signals are output to the serial DAC.
LRCLK	O	LR clock signals are output to the serial DAC.
DATA	O	Digital audio data signals output to the serial DAC.
BCLK	O	Bit clock signals output to the serial DAC.

※Interfacing with the serial DAC is made in the MSB-First mode.

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PIN	INPUT/OUTPUT	FUNCTION
RESETB	I	Reset signals
XIN	I	These are external pins of the crystal-oscillator. Clock can take input directly from XIN.
XOUT	O	
TEST1 TEST2 TEST3	I I I	These are test signal input pins, and fixed to "L" for normal use. TEST2 pin is fixed to "H" when MROM or SRAM is used.
VCC	—	Power supply
GND	—	Ground

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4 DESCRIPTION OF FUNCTIONS

4.1 ADDRESS MAP

1FFFH ~ 1000H	Wave data area (same as for the RF5C105)
0FFFH ~ 0020H	Not used (impossible to access)
001FH	WAVE RAM ADDRESS 8CH. HIGH
001EH	WAVE RAM ADDRESS 8CH. LOW
001DH	WAVE RAM ADDRESS 7CH. HIGH
001CH	WAVE RAM ADDRESS 7CH. LOW
001BH	WAVE RAM ADDRESS 6CH. HIGH
001AH	WAVE RAM ADDRESS 6CH. LOW
0019H	WAVE RAM ADDRESS 5CH. HIGH
0018H	WAVE RAM ADDRESS 5CH. LOW
0017H	WAVE RAM ADDRESS 4CH. HIGH
0016H	WAVE RAM ADDRESS 4CH. LOW
0015H	WAVE RAM ADDRESS 3CH. HIGH
0014H	WAVE RAM ADDRESS 3CH. LOW
0013H	WAVE RAM ADDRESS 2CH. HIGH
0012H	WAVE RAM ADDRESS 2CH. LOW
0011H	WAVE RAM ADDRESS 1CH. HIGH
0010H	WAVE RAM ADDRESS 1CH. LOW
000FH ~ 0009H	Not used (impossible to access)
0008H	Sound ON/OFF register
0007H	Control register
0006H	ST data memory
0005H	LSH data memory
0004H	LSL data memory
0003H	FDH data memory
0002H	FDL data memory
0001H	PAN data memory
0000H	ENV data memory

Notice: 0000H to 0007H are used as write only registers, and selected by using the bank function of the control register.
0010H to 001FH are used as read only registers.

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4.2 CONTROL REGISTER

This register sets up the IC mode, the bank address of the wave memory, and the bank channel of the internal memory. This register can only be written.

7	6	5	4	3	2	1	0	Bit
ON OFF	MOD	—	—	WB3	WB2	WB1	WB0	Address
				—	CB2	CB1	CB0	0007H

■ **Bit 7 : ON/OFF**
When this bit is set, the IC starts sounding; when it is reset, sounding is suspended. The external wave memory of the microcomputer can be read only while sounding is suspended. When the IC is sounding, further restrictions described below apply for writing into the external wave memory.

■ **Bit 6 : MOD**
This bit is used to control the selection of a particular register into which the contents of bits 3 to 0 are to be written. When this bit is set to "H", the microcomputer writes the contents in bits 2 to 0 into bits CB2 to CB0 of this register; when it is "L", it writes the contents in bits 3 to 0 into bits WB3 to WB0.

● **When MOD = "H"**

■ **Bits 2 to 0 : CB2 to CB0**
These bits control the selection of a particular channel when the microcomputer accesses the internal memories (FNV, PAN, FDL, FDH, LSL, LSH, ST).

CB2	CB1	CB0	Channel No.
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

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● **When MOD = "L"**

■ **Bit 3 to 0 : WB3 to WB0**

These bits control the higher address when the microcomputer accesses the external wave memory. The table below shows the relationships between the setup values in WB3 to WB0 and the address for accessing the external wave memory.

WB3	WB2	WB1	WB0	EXTERNAL WAVE MEMORY ADDRESS	
				MEMORY NO.	ADDRESS
0	0	0	0	1	0000H~0FFFH
0	0	0	1	1	1000H~1FFFH
0	0	1	0	1	2000H~2FFFH
0	0	1	1	1	3000H~3FFFH
0	1	0	0	1	4000H~4FFFH
0	1	0	1	1	5000H~5FFFH
0	1	1	0	1	6000H~6FFFH
0	1	1	1	1	7000H~7FFFH
1	0	0	0	2	0000H~0FFFH
1	0	0	1	2	1000H~1FFFH
1	0	1	0	2	2000H~2FFFH
1	0	1	1	2	3000H~3FFFH
1	1	0	0	2	4000H~4FFFH
1	1	0	1	2	5000H~5FFFH
1	1	1	0	2	6000H~6FFFH
1	1	1	1	2	7000H~7FFFH

Notes Memory No.1 is the memory to be selected by RAMC1B.
Memory No.2 is the memory to be selected by RAMC2B.

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4.3 INTERNAL MEMORY

This internal memory stores sound data described below for each of the eight channels.

● ST data (Address = 0006H)

The high 8 bits in this address is the ST data that reads the wave memory of the channel which starts sounding. In this case, "00H" is set in the lower address.

● LSH data (Address = 0005H)

When the stop data is read from the wave memory during sounding, the upper address for reading the wave address is changed into LSH data, and the wave memory is read out again.

● LSL data (Address = 0004H)

When the stop data is read from the wave memory during sounding, the lower address for reading the wave address is changed into LSL data, and the wave memory is read out again.

● FDH data (Address = 0003H)

This data controls the address counter that generates an address used to read from the wave memory during sounding. Use the FDH bits to set up the up-counts of addresses per sampling time as shown in the table below.

RAMAX	NOT USED	USED
FDH BIT	ACCESS UP-COUNT	
7	2^4	2^8
6	2^3	2^4
5	2^2	2^3
4	2^1	2^2
3	2^0	2^1
2	2^{-1}	2^0
1	2^{-2}	2^{-1}
0	2^{-3}	2^{-2}

■ Example: When only FDH bits 4 and 3 are set, the address is incremented by 9 ($=2^1 + 2^0$) counts per sampling (when RAMAX is not used).

● FDL data (Address = 0002H)

This data controls the address counter that generates an address used to read from the wave memory during sounding. Use the FDL bits to set up the up-counts of addresses per sampling time as shown in the table on the next page.

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RAMAX	NOT USED	USED
FDL BIT	ADDRESS UP-COUNT	
7	2^{-4}	2^{3}
6	2^{-5}	2^{4}
5	2^{-6}	2^{5}
4	2^{-7}	2^{6}
3	2^{-8}	2^{7}
2	2^{-9}	2^{8}
1	2^{-10}	2^{9}
0	2^{-11}	2^{10}

■ Example: When only FDL bits 4 and 3 are set, the address is incremented by $2^{7} + 2^{8}$ counts per sampling (when RAMAX is not used).

● **PAN data (Address = 0001H)**

This data controls the process through which output generated in the while-sounding channel is converted into stereo sounds and fed separately into the "L" and "R" channels. The higher 4-bits of PAN data become the coefficients of the "R" output and the lower 4-bits become the coefficients of the "L" output.

7	6	5	4	3	2	1	0	Bit
MSB			LSB	MSB			LSB	Address
Coefficients of "R" output				Coefficients of "L" output				0001H

● **ENV data (Address = 0000H)**

This ENV data is multiplied by the wave data which is read from the wave memory in the while-sounding channel in order to put a stress on the amplitudes of the wave data. In this case, bit 7 becomes the MSB and bit 0 becomes the LSB.

4.4 CHANNEL ON/OFF REGISTER

This register serves to control the sounding/sounding suspended status in each channel. However, the control of the control register has priority. Therefore, if the control register is set to the sounding status, this register can be used. Bit 0 corresponds to channel 1 and bit 7 to channel 8.

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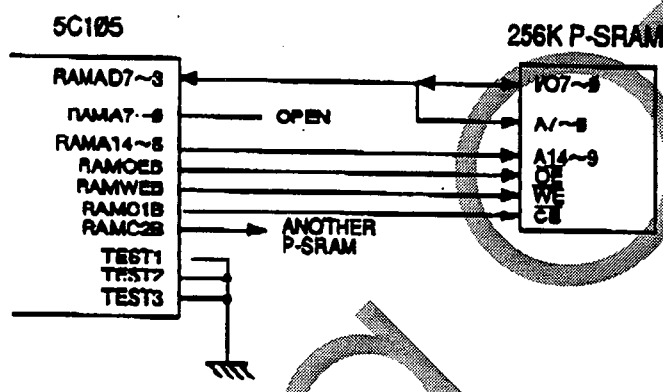
4.5 MICROCOMPUTER INTERFACE IC

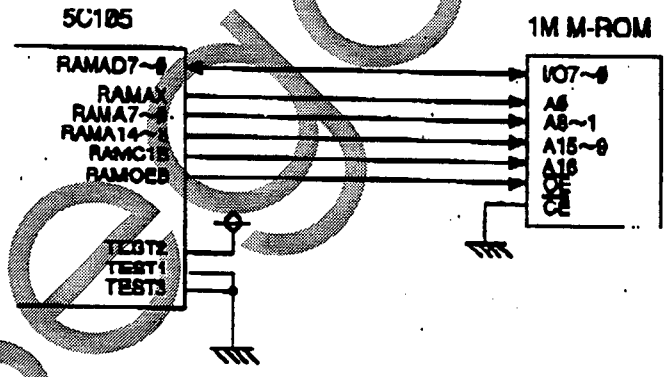
This IC can be used as a peripheral IC for the general-purpose 8-bit CPU.
The table below should be referenced, since the conditions for access of this IC from the microcomputer vary with the setting of the sounding/sounding suspend status which is selected by the control register.

Status	External wave memory		Internal wave memory	
	Read	Write	Read	Write
While sounding	Impossible	Access in a period of 16 source clock cycles or more.	Impossible	Access in a period of 384 source clock cycles or more. (0068H)
While sounding suspended	Possible	Possible	Impossible	Access in a period of 48 source clock cycles or more (0008H).

4.6 WAVE MEMORY INTERFACE IC

This IC is used as a wave memory, and connects the external Pseudo SRAM, SRAM or MROM. The typical connections are illustrated below.





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4-7 INTERNAL REGISTERS READ CYCLE

By accessing internal registers 0010H to 001FH, the address of the current wave RAM can be read. You must wait for 5 or more cycles after accessing the wave RAM access in order to get the correct address.

HIGH BYTE

MSB	6	5	4	3	2	1	LSB
A15	A14	A13	A12	A11	A10	A9	A8

A15 = "0" applies for RAMC1B = "0" and A15 = "1" applies for RAMC2B = "0".

LOW BYTE

MSB	6	5	4	3	2	1	LSB
A7	A6	A5	A4	A3	A2	A1	A0

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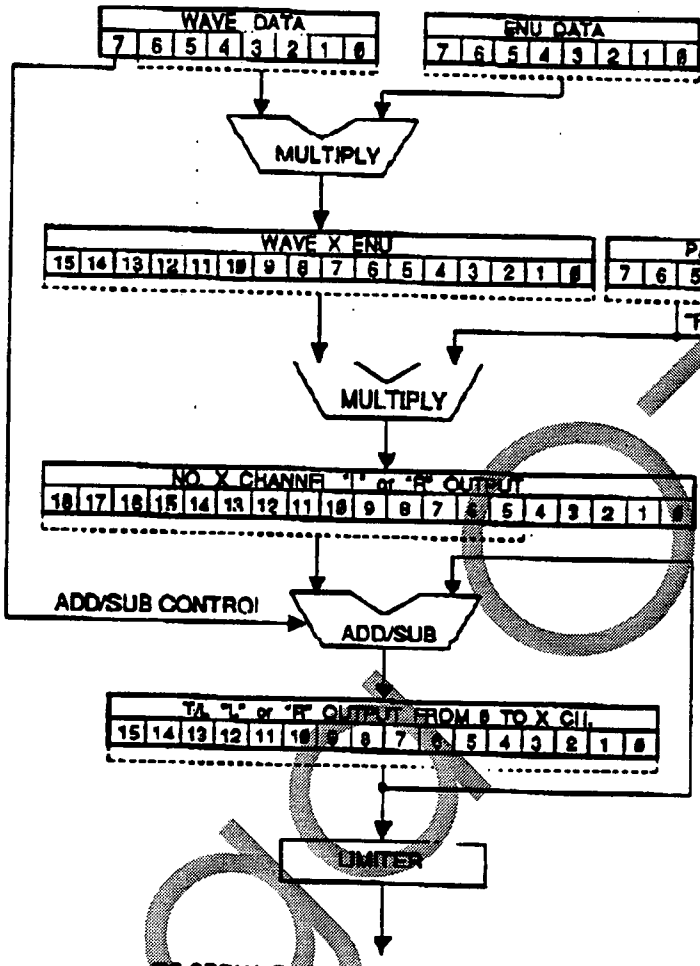
4-8 PCA (PCM DIGITAL CONTROL AMPLIFIER)

This block is used to generate tones by using data which is read from the external and internal devices. The data processing is illustrated below.

The processes shown below are executed in each channel in order from channel 1 through channel 8. Every time the values for "R" and "L", which are summed over 8 channels, are accumulated, the sample/hold signals are generated for "R-" and "L-" output. The limiter circuit sets the accumulated results to FFFFH, if the result value overflows in the positive direction while accumulating data over the eight channels. If it overflows in the negative direction, it is set to 0000H.



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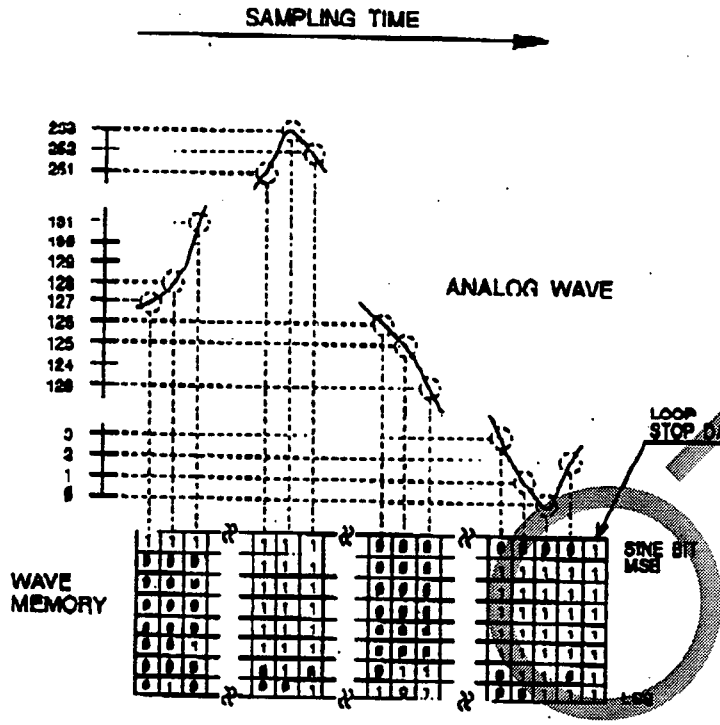
4.9 WAVE DATA FORMAT

The figure below shows an example of data stored in the external wave memory using wave data format. In this example, the analog waveform is digital-sampled with a center value of 127, a maximum of 253 and a minimum of 0. The wave data "FFH" is used as the loop stop data. Once this data is read from the wave memory, the address for reading the wave memory is reset to the LSH and LSL data, and the wave data is read again.



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5 DC ELECTRICAL SPECIFICATIONS

Ta=0~70°C, VCC=5V±5%

	Symbol	Item	Test condition	Standard values min.	typ.	max.	Units
Input	VIH1	"H" input voltage (TTL compatible)		2.0		VCC +0.3	V
	VIL1	"L" input voltage (TTL compatible)		-0.3		0.8	V
	VIH2	"H" input voltage (XIN pin)		3.5		VCC +0.3	V
	VIL2	"L" input voltage (XIN pin)		-0.3		1.5	V
	ILI	Input leak current	0≤VI≤VCC	-10		10	µA
Output	VOH	"H" output voltage	IOH=-4.0mA	2.4			V
	VOL	"L" output voltage	IOL=4.0mA			0.4	V
	IOZ	Output leak current when off	0≤VO≤VCC	-10		10	µA
Current	ICC0	Power supply current not in operation	VIN=0V, VCC			300	µA
	ICC1	Power supply current in operation	XIN=16MHz With no load			30	mA

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6 AC ELECTRICAL SPECIFICATIONS

Ta=0~70°C, VCC=5V±5%

Symbol	Item	Test condition	Standard values			Units
			min	typ	max	
fOPR	Input clock frequency				10	MHz
TCE	External memory chip enable pulse width	Fopr=10MHz	200			ns
TAS	Address setup time	Fopr=10MHz	0			ns
TRAH	Lower address hold time	Fopr=10MHz	30			ns
TOHC	Output enable hold time	Fopr=10MHz	0			ns
TOEA	Output enable/output delay time	Fopr=10MHz			50	ns
TOHZ	Output disable/output delay time	Fopr=10MHz	20			ns
TCW	Chip enable time	Fopr=10MHz	200			ns
TWP	Write signal pulse time	Fopr=10MHz	30			ns
TDW	Output data setup time	Fopr=10MHz	30			ns
TDH	Output data hold time	Fopr=10MHz	0			ns
TRDA	External CPU read signal enable/output delay time	Fopr=10MHz			100	ns
TRDH	External CPU read signal disable/output delay time	Fopr=10MHz	10			ns
TWRA	Write data setup time	Fopr=10MHz	30			ns
TWRG	Write data hold time	Fopr=10MHz	30			ns

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Symbol	Item	Test condition	Standard values			Units
			min	typ	max	
TAH	Address hold time (CSB-An)	Fopr=10MHz	0			ns
TAH1	Address hold time (RDB-An)	Fopr=10MHz	30			ns
TAH2	Address hold time (WRB-An)	Fopr=10MHz	30			ns
TAS1	Address setup time (An-WRB)	Fopr=10MHz	30			ns
TAS2	Address setup time (An-WRB)	Fopr=10MHz	30			ns
TRDCE	Chip enable hold time (RDB-CSB)	Fopr=10MHz	0			ns
TWRCE1	Chip enable hold time (WRB-CSB)	Fopr=10MHz	30			ns
TWRCE2	Chip enable hold time (WRB-CSB)	Fopr=10MHz	0			ns
TRFCW	Refresh command pulse width	Fopr=10MHz	200			ns
TRFD	Refresh pulse delay time	Fopr=10MHz			200	ns
TRFP1	Refresh pulse width	Fopr=10MHz	50			ns
TRFP2	Refresh pulse width	Fopr=10MHz	50			ns
TRFR	Refresh pulse recovery time	Fopr=10MHz			300	ns
Tirdh	Internal register data hold time	Fopr=10MHz	0			ns
Tirda	Internal register data setup time	Fopr=10MHz	30			ns
Tirdo	Internal register read access time	Fopr=10MHz	60			ns

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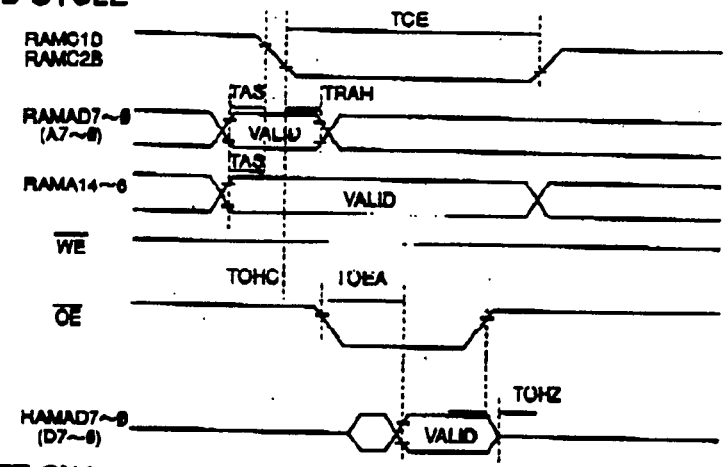
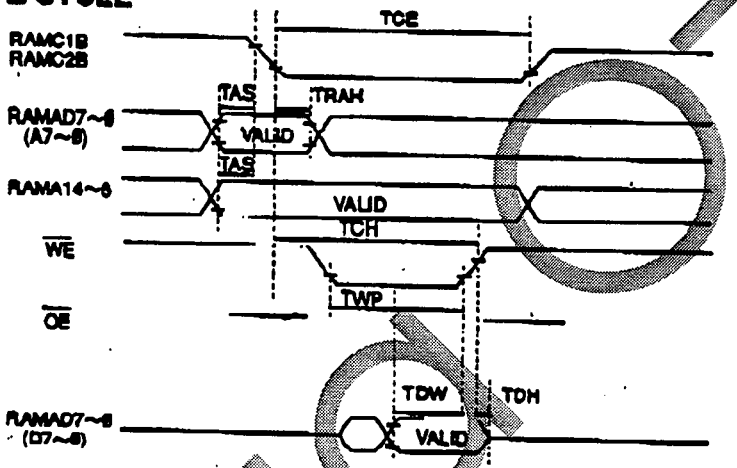
7 TIMING CHART

7.1 Pseudo SRAM I/F

● READ CYCLE

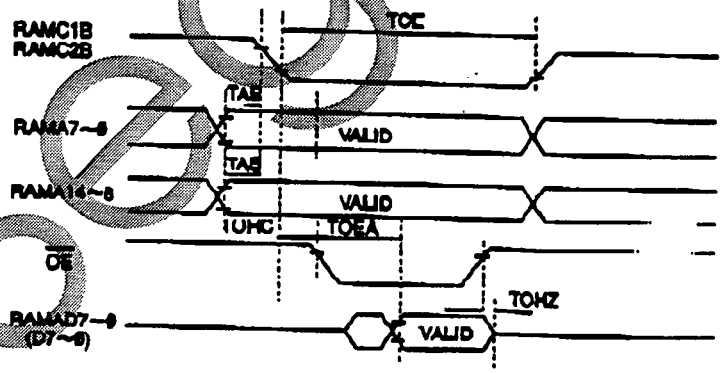


● WRITE CYCLE



7.2 MASK ROM I/F

● READ CYCLE



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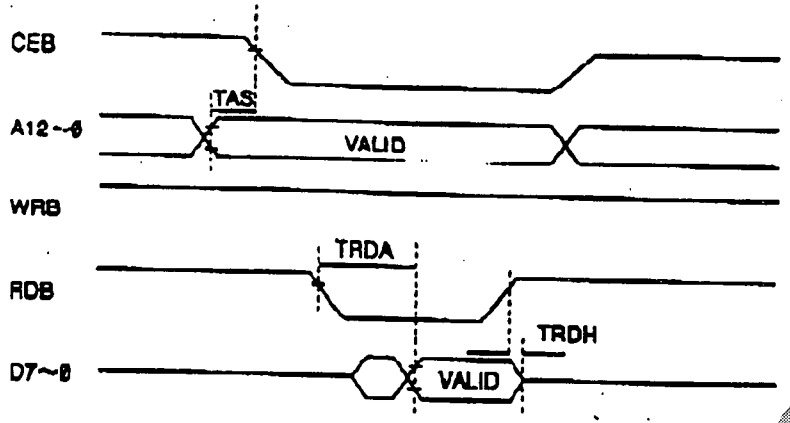
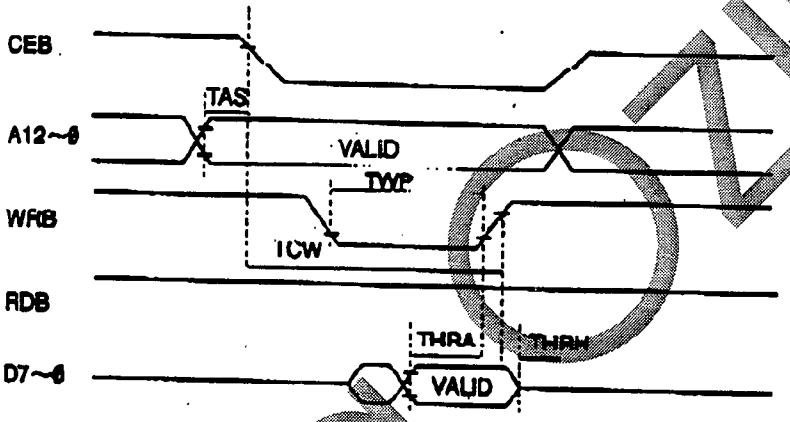
7.3 CPU I/F

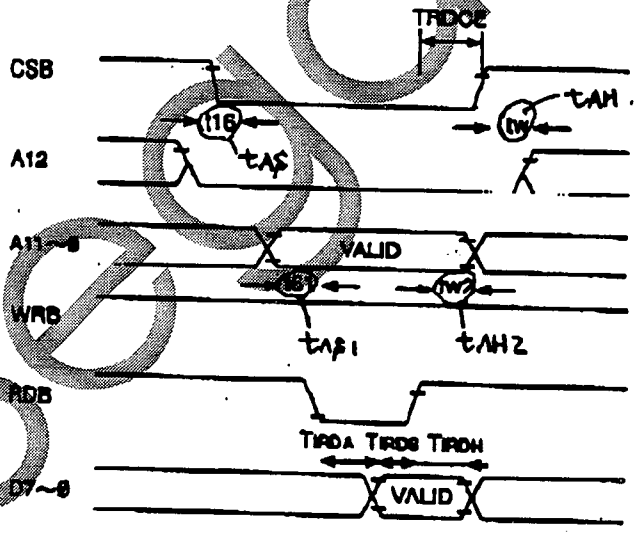
● READ CYCLE



● WRITE CYCLE



● Internal register read cycle (0010~001FH)



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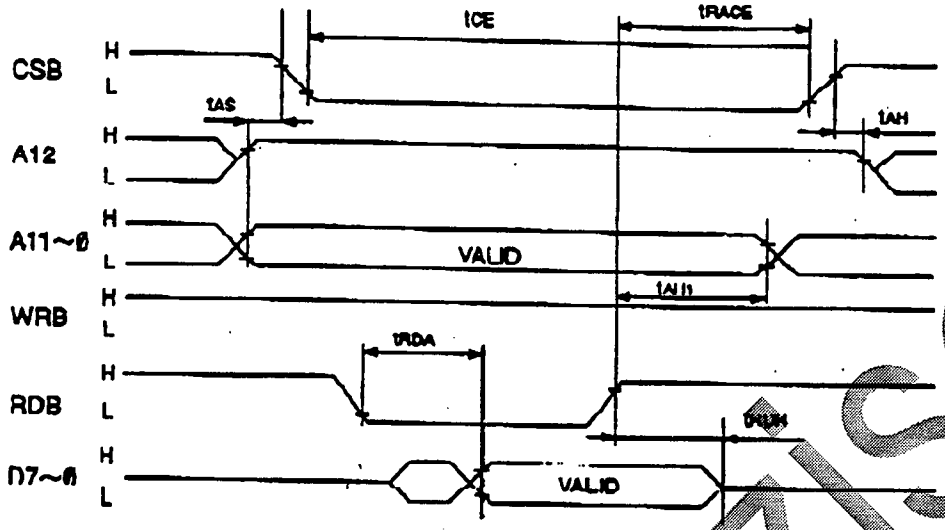
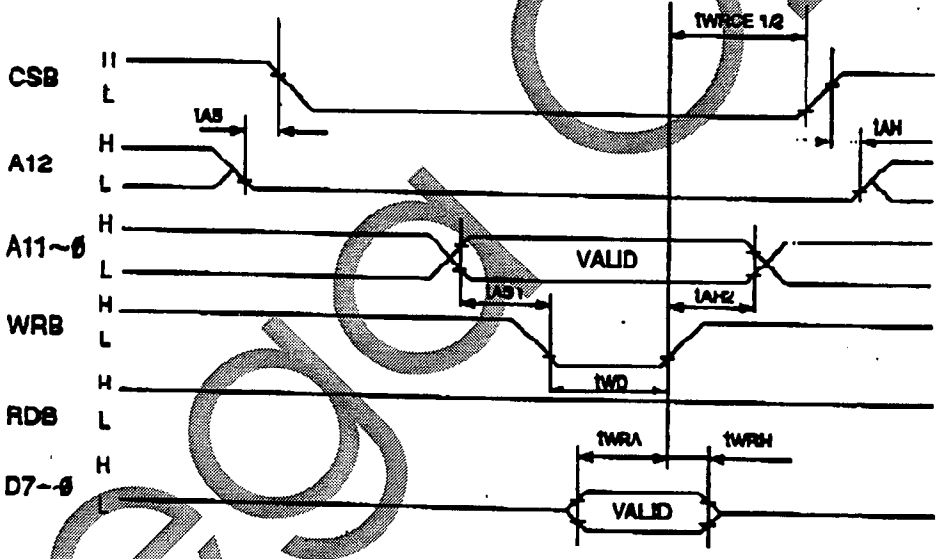
7-4 CPU INTERFACE

● CPU ← Wave memory read cycle (while sounding suspended)



● CPU → Internal register write cycle (while sounding/sounding suspended)



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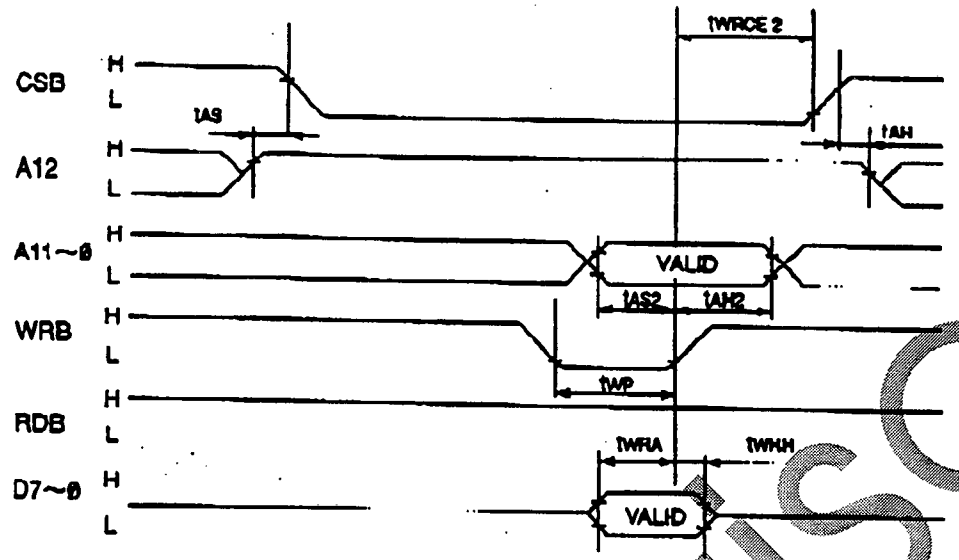
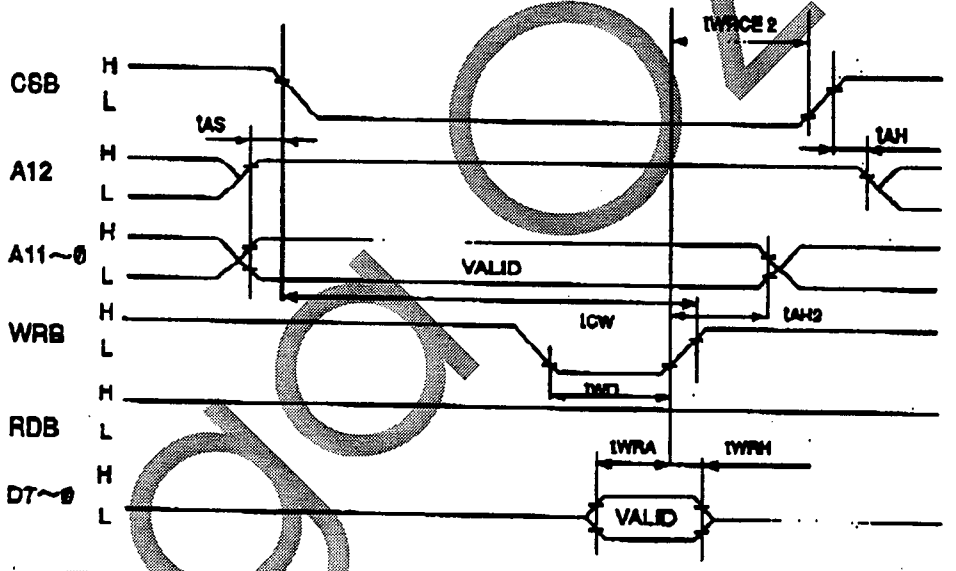
● **CPU → Wave memory write cycle (while sounding)**



● **CPU → Wave memory write cycle (while sounding suspended)**



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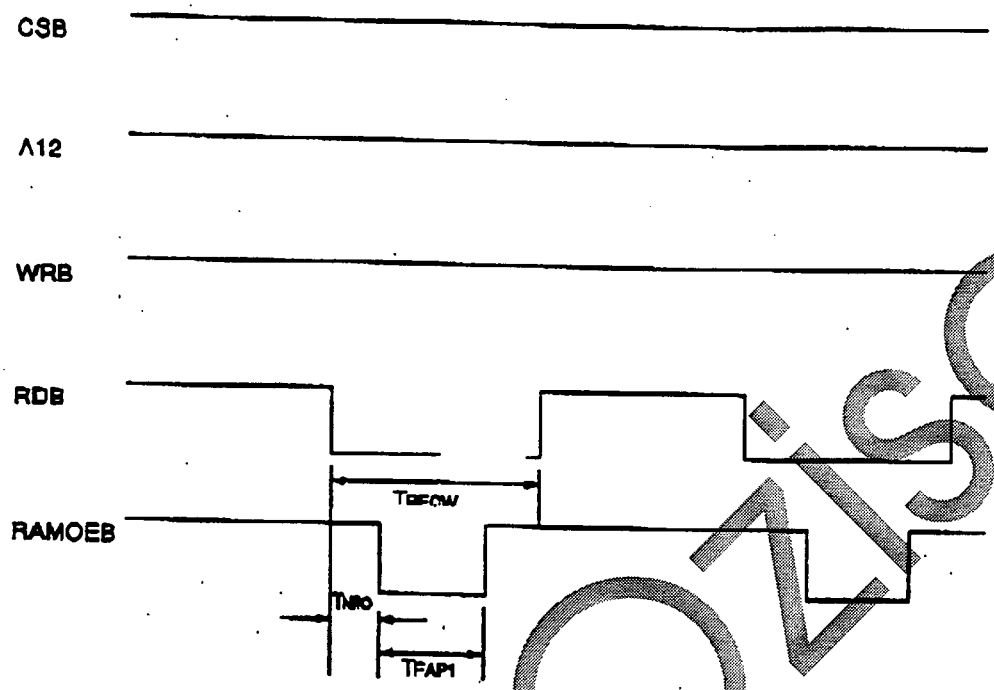
CONFIDENTIAL #161 PROPERTY OF SEGA

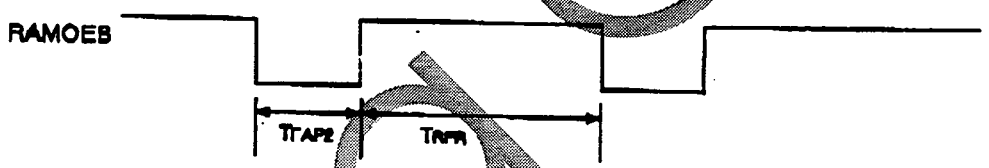
7.5 Pseudo SRAM I/F

● REFRESH CYCLE

■ While sounding suspended (automatic refresh)



■ While sounding



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