TimingGen

File: TimingGen.kicad_sch

LFO

File: LFO.kicad_sch

REG

File: REG.kicad_sch

PG0

File: PG0.kicad_sch

PG1

File: PG1.kicad_sch

PG2

File: PG2.kicad_sch

PG3

File: PG3.kicad_sch

EG0

File: EG0.kicad_sch

EG1

File: EG1.kicad_sch

EG2

File: EG2.kicad_sch

OP0

File: OP0.kicad_sch

OP1

File: OP1.kicad_sch

OP2

File: OP2.kicad_sch

NOISE

File: NOISE.kicad_sch

ACC0

File: ACC0.kicad_sch

ACC1

File: ACC1.kicad_sch

TIMER

File: TIMER.kicad_sch

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YM2151 schematics

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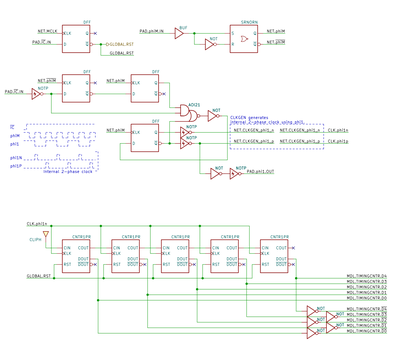
Sheet: /

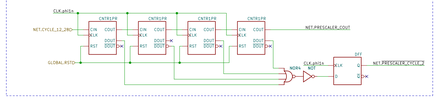
File: YM2151.kicad_sch

Title: YM2151

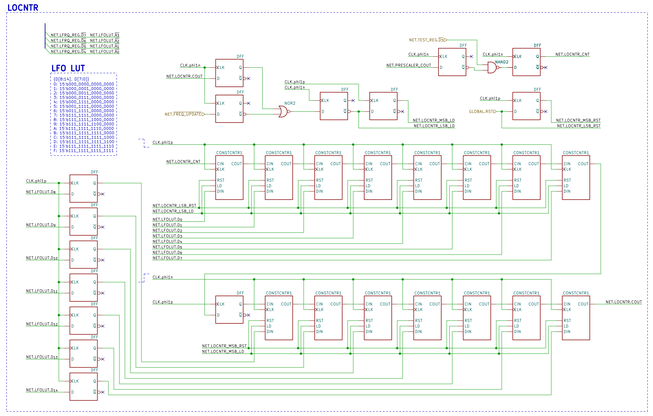
Size: A0	Date: 2023-08-05	**Rev: v1.3**
KiCad E.D.A. eeschema (6.0.7)		Id: 1/18


NET.MCLK
PAD.fF_in
GLOBAL_RST
PAD.phi_in
NET.phiM
NET.fDIV
CLKGEN generates
phiV/H1,2 phase_clock using phiL
NET.CLKGEN_phiV_a
NET.CLKGEN_phiV_b
CLK.phiV
NET.CLKGEN_phiH_a
NET.CLKGEN_phiH_b
CLK.phiH
PAD.phi1.OUT
phiV
phiH
phiL
Internal 2-phase clock
CLK.phiV
CLPH
GLOBAL_RST
MDL.TIMINGCNTR.D4
MDL.TIMINGCNTR.D3
MDL.TIMINGCNTR.D2
MDL.TIMINGCNTR.D1
MDL.TIMINGCNTR.D0
MDL.TIMINGCNTR.D5

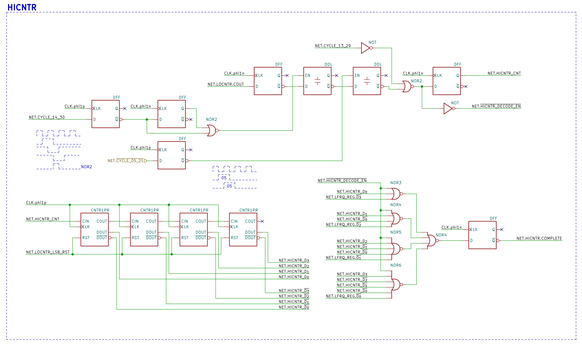
Prescaler



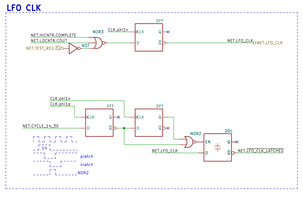
LOCNTR



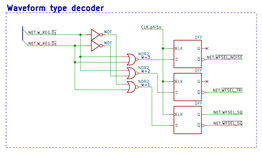
HICNTR



LFO CLK

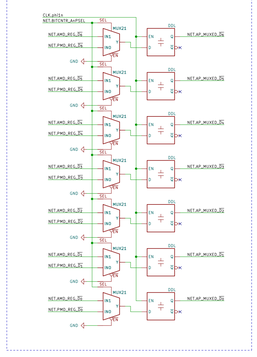


Waveform type decoder

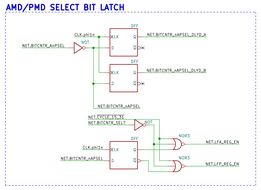


SIGN BIT LATCH

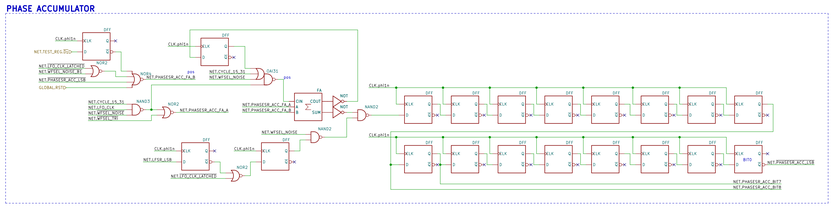
AMD/PMD MUX



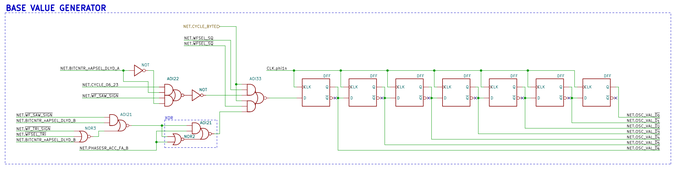
AMD/PMD SELECT BIT LATCH



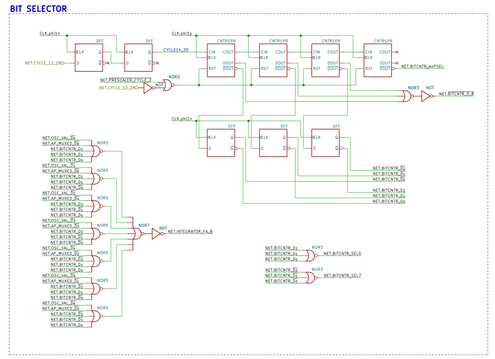
PHASE ACCUMULATOR



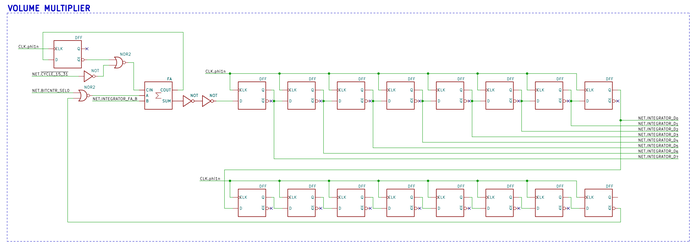
BASE VALUE GENERATOR



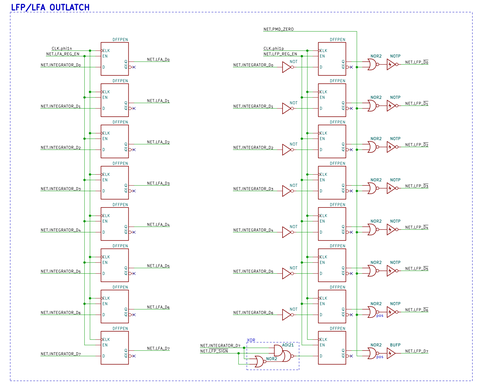
BIT SELECTOR



VOLUME MULTIPLIER



LFP/LFA OUTLATCH



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YM2151 schematics

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Sheet: /LFO/

File: LFO.kicad_sch

Title: YM2151

Size: A0	Date: 2023-08-05	**Rev: v1.3**
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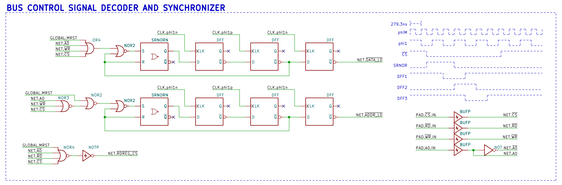
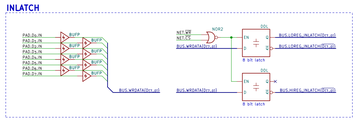
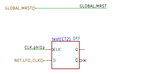
BUS CONTROL SIGNAL DECODER AND SYNCHRONIZER

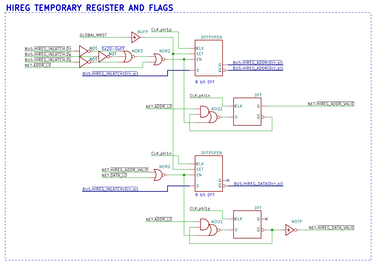


INLATCH

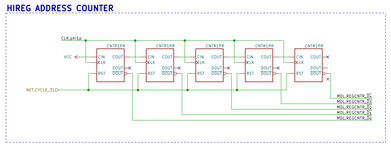


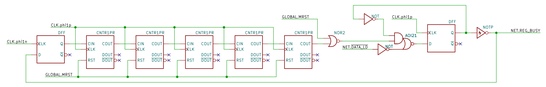


HIREG TEMPORARY REGISTER AND FLAGS



HIREG ADDRESS COUNTER





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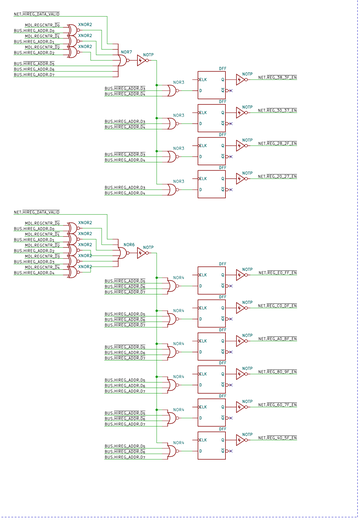

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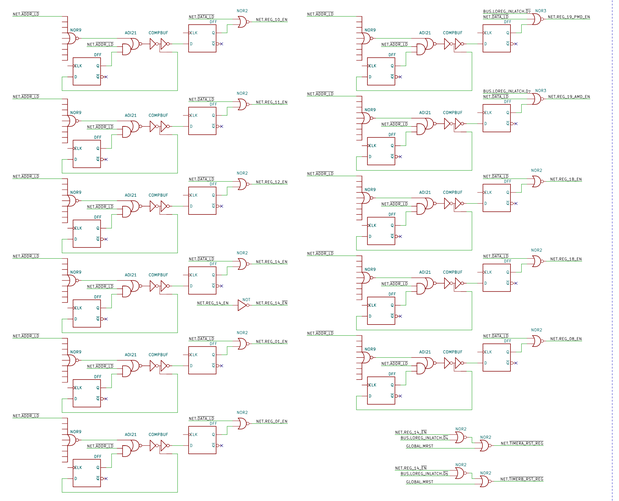

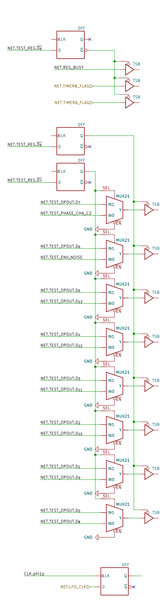

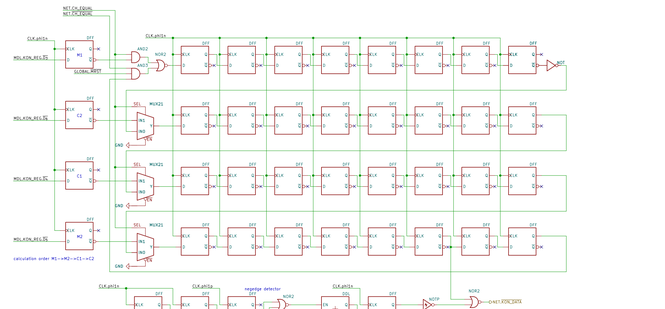

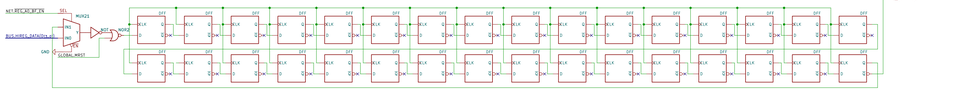

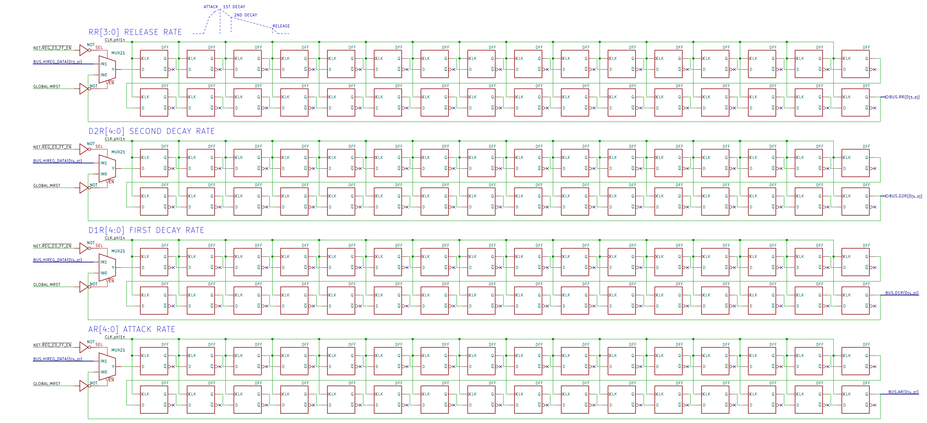

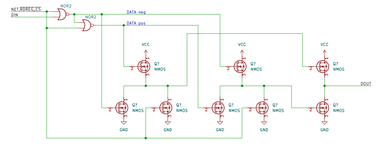

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YM2151 schematics

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File: REGLatch.sch

Title: YM2151

Size: A0	Date: 2023-08-05	**Rev: v1.3**
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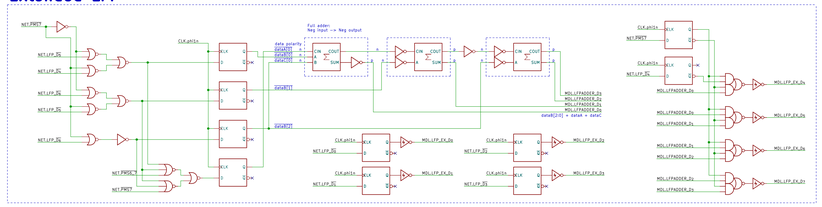
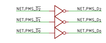
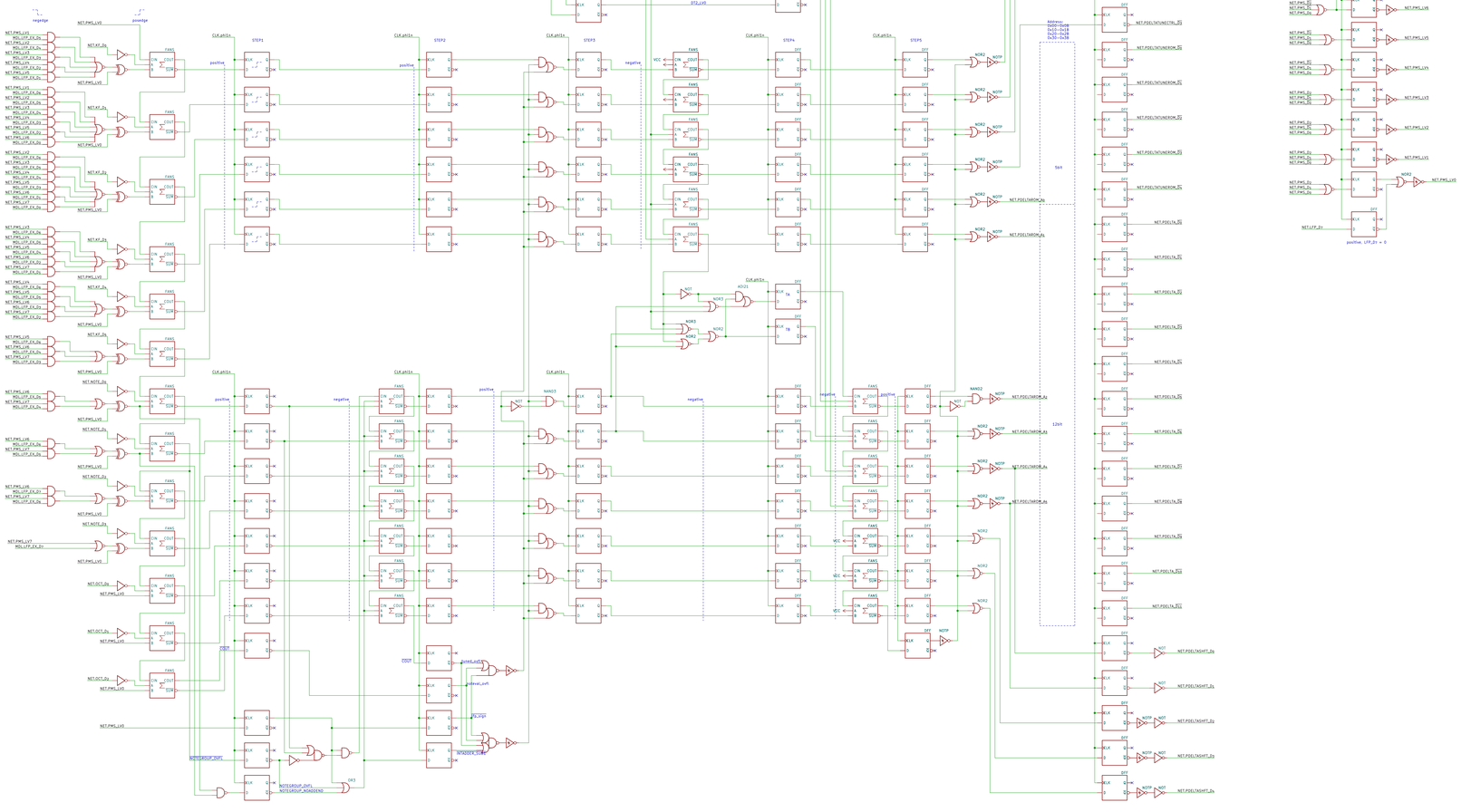
Extended LFP







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YM2151 schematics

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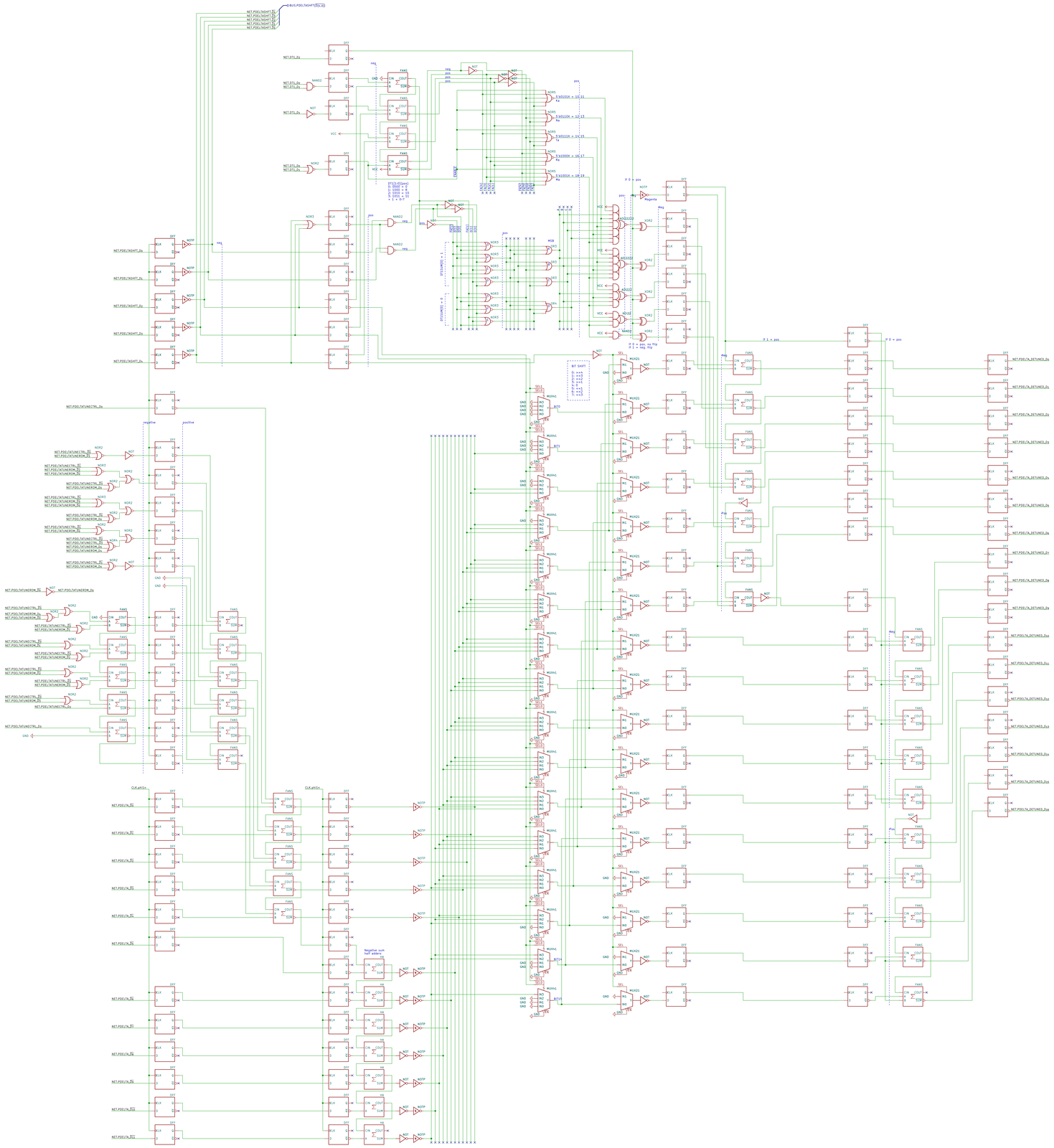
Rev: v1.3	
Id: 1/18	



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IKA Victor Co., Inc.
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Size: A0	Date: 2023-08-05	**Rev: v1.3**
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YM2151 schematics
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Sheet: /PG2/
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Size: A0 | Date: 2023-08-05 | **Rev: v1.3**
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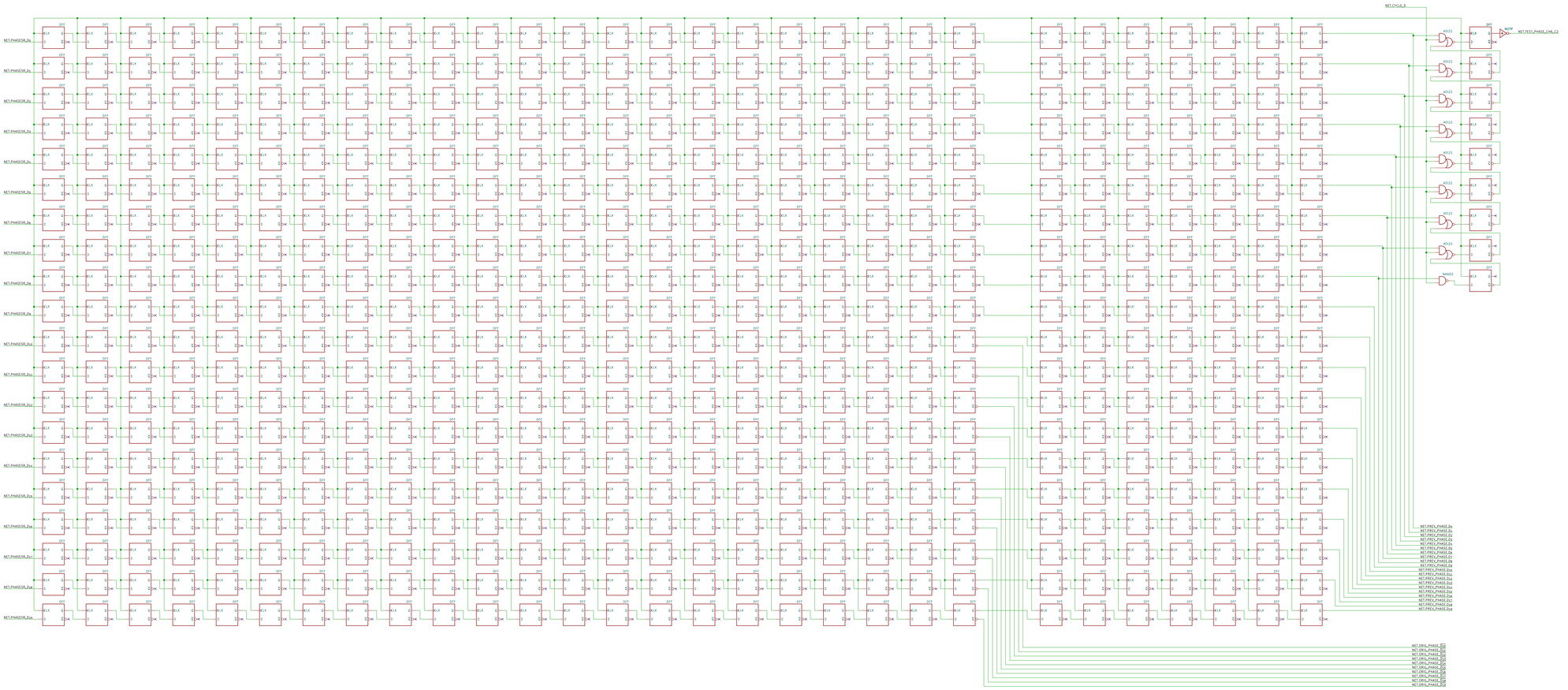

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YM2151 schematics
IKA Victor Co., Inc.
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File: PG2.kicad_sch

Title: YM2151

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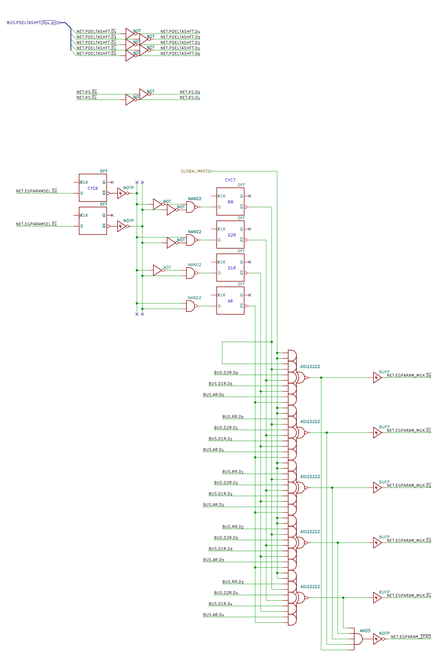

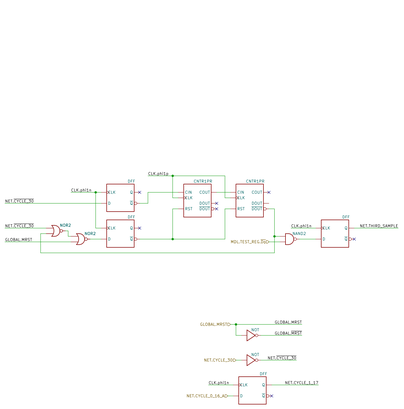

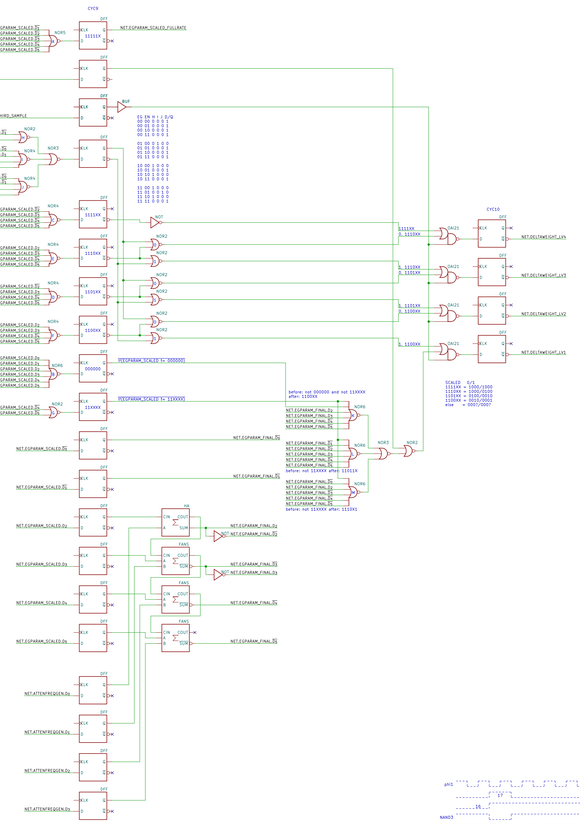

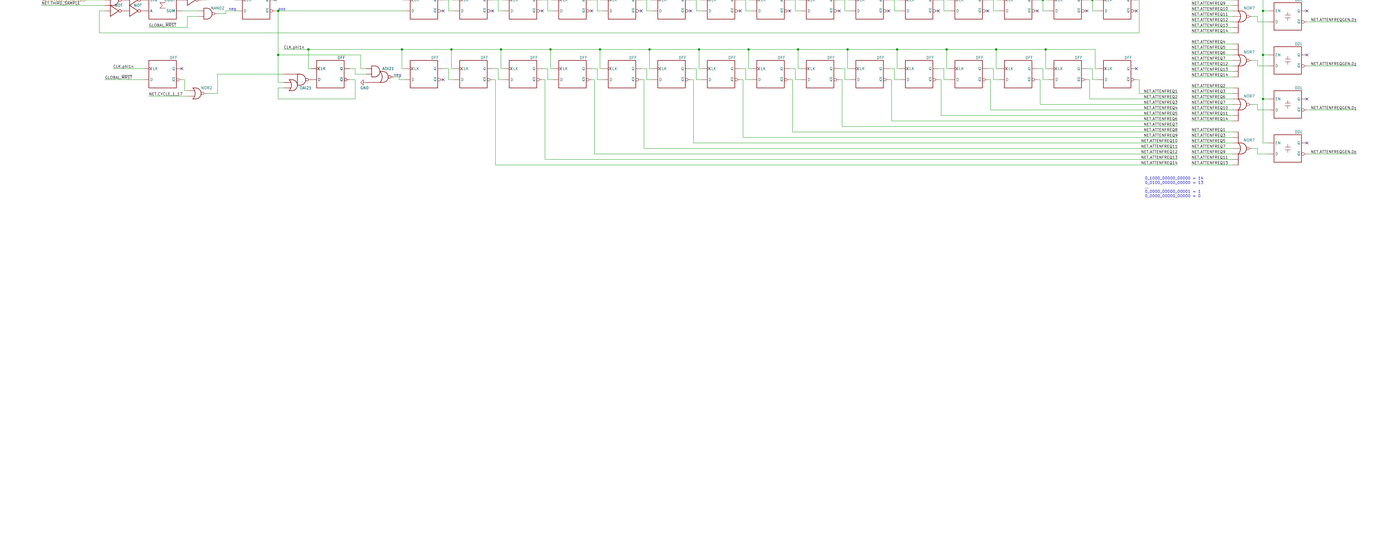

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YM2151 schematic

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File: EG07.kicad_sch

Title: YM2151

Size: A0	Date: 2025-08-05	**Rev: v1.3**
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ATTACK
LV1 [7:5]:111 -[8:5]- [3]
LV2 [7:5]:111 -[8:5]- [4] -[3:1]
LV3 [7:5]:111 -[8:5]- [5] -[4:2] -[1:0]
LVN [7:5]: -[8:5]- [6] -[5] -[4] -[3] -[1:0]

DECAY/RELEASE
[8:5]0000000: LV1, LV2, LV3

111111111X = after max(reset value)
000000000X = after min

VCC
NET.ENVDELTA_WEIGHT_LV1
NET.ENVDELTA_WEIGHT_LV2
NET.ENVDELTA_WEIGHT_LV3
NET.ENVDELTA_WEIGHT_LVN
AO3332
AO3333
NOT
FADC
XOR21
NOR3
AND2
DFF
CYC1
CYC2
CYC3
CYC4
CYC5
CYC6
CYC7
CYC8
CYC9
CYC10
CYC11
CYC12
CYC13
CYC14
CYC15
CYC16
CYC17
CYC18
CYC19
CYC20
CYC21
CYC22
CYC23
CYC24
CYC25
CYC26
CYC27
CYC28
CYC29
CYC30
CYC31
CYC32
CYC33
CYC34
CYC35
CYC36
CYC37
CLK_phi1n
CLK_phi2n
NET.ENV_DRIL_D0
NET.ENV_DRIL_D1
NET.ENV_DRIL_D2
NET.ENV_DRIL_D3
XOR2
DRWIRE3
NOR6
NOR8
NET.ZTTEC_WIN
NET.ZTTEC_WIN2
NET.FIRST_DECAY_END
MOL-RES_D1_D0
MOL-RES_D1_D1
MOL-RES_D1_D2
MOL-RES_D1_D3
NOTP
AND5
FIRST DECAY
NOT LV1[7] MAX
NOT FIRST_DECAY_END
NOT KON_DETECTED

SECOND DECAY or RELEASE
NOT LV2[7] MAX
NOT KON_DETECTED

ATTACK
KON_ENABLED
NOT LV3[7] LEVEL MAX
NOT FULLSAT1

NET.KON_DETECTED
NET.FIRST_DECAY_END
NET.ATTEN_MAX
NET.ENVSTATE_CURR_D1
NOR5
NOR2
NOR4
ATTEN_INC
add reset signal here for FPGA implementation
NET.KON_DETECTED
NET.ATTEN_MAX
NET.ENVSTATE_CURR_D1
NOR5
NOR4
ATTEN_DEC
NET.EGFRAMK_SCALED_FULLRATE
NET.ATTEN_MIN
NET.KON_CURRENT
NET.ENVSTATE_CURR_D0
NET.ENVSTATE_CURR_D1
NOR5
NOT
GLOBAL_MRST
XOR2
PREATTEN_MAX
NET.FIX_ATTEN_MAX
NET.KON_DETECTED
NET.EGFRAMK_SCALED_FULLRATE
AO21
NOT
NOTP
PREATTEN_EN

release
=> start release
ENVSTATE != 0
KON_DETECTED == 0
=> underflow detected
ENVSTATE == 0
KON_DETECTED == 0
=> overflow, start first decay
ENVSTATE == 1
KON_DETECTED == 0
=> running first decay
=> running second decay
ENVSTATE == 1
KON_DETECTED == 1
=> start second decay
NET.KON_DETECTED
NET.ATTEN_MIN
NET.ENVSTATE_CURR_D0
NET.ENVSTATE_CURR_D1
NET.FIRST_DECAY_END
NET.ENVSTATE_CURR_D0
NET.ENVSTATE_CURR_D1
NOR5
NOR6
NOR8
NOR9
NET.ENVSTATE_NEXT_D0
NET.ENVSTATE_NEXT_D1
NET.KON_DETECTED
NET.KON_CURRENT
NET.ENVSTATE_CURR_D0
NET.ENVSTATE_CURR_D1
NET.FIRST_DECAY_END
NET.KON_DETECTED
NET.ATTEN_MAX
NET.ATTEN_MIN
NET.ZTTEC_WIN
NET.KEY_PRESSED
NET.FC_RESET_RST
GLOBAL_MRST
prev = 0
now = 1
kesin positive edge detector
NET.KON_DATA
NOT
AND2
NOR2
reg
NOTP
prev = 0
now = 1
kesin positive edge detector
NET.KON_DETECTED
NET.KON_PREV
NOR2
prev
now
NOTP
NET.KON_CURRENT
NET.EGFRAMSEL_D0
NET.EGFRAMSEL_D1
NAND29
BUF
NET.ENVSTATE_CURR_D0
NET.ENVSTATE_CURR_D1
NET.FIRST_DECAY_END
NET.KON_DETECTED
NET.ATTEN_MAX
NET.ATTEN_MIN
NET.ZTTEC_WIN
NET.KEY_PRESSED
NET.FC_RESET_RST
GLOBAL_MRST
NOT

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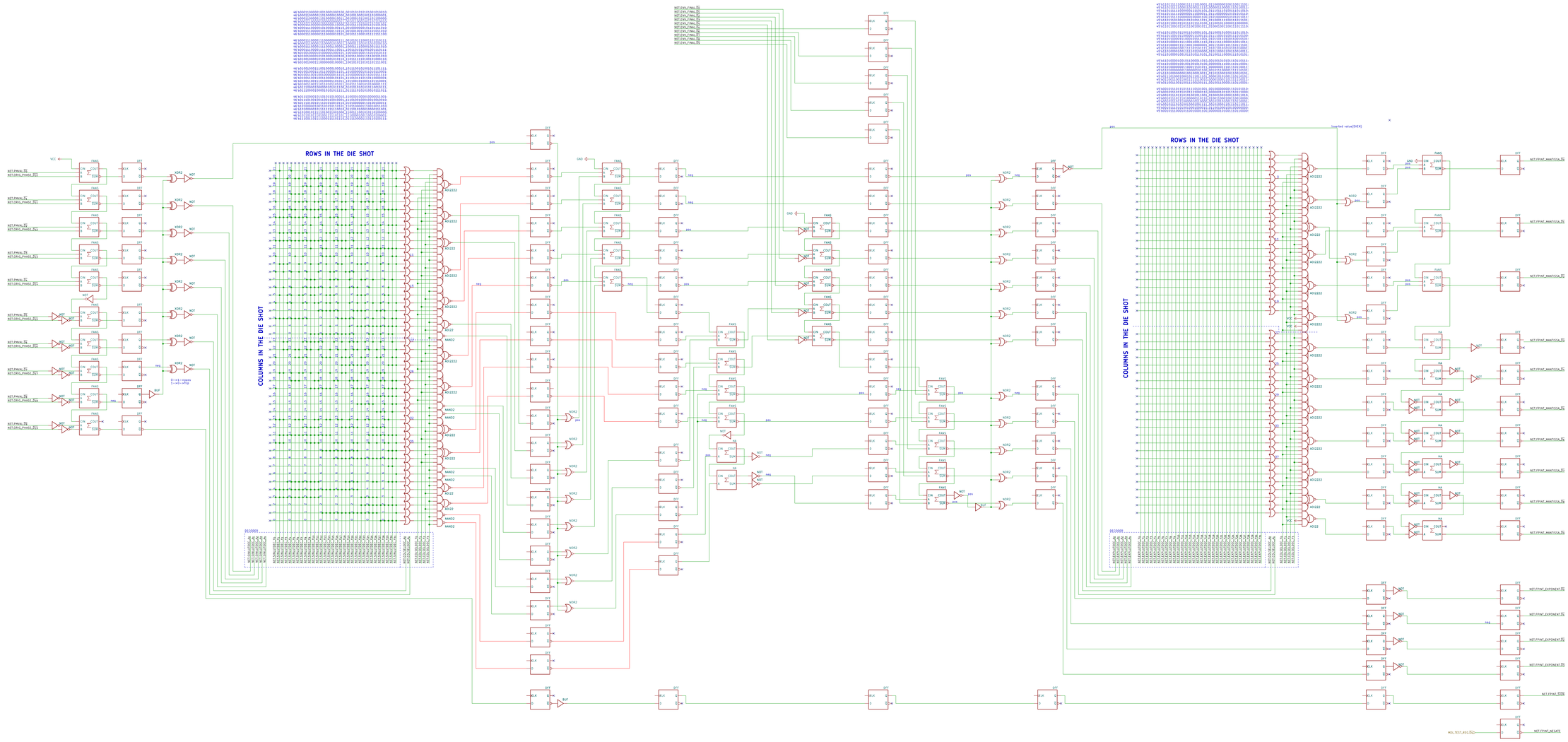
YM2151 schematics
HUA Victor Co., Inc.
Sheet: /TOJ/
File: fit_wrap.sch

Title: YM2151	
Size: A0 | Date: 2023-08-05	**Rev: v1.3**
KiCad E.D.A. eeschema (6.0.7)	Id: 9/19



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YM2151 schematics
IKA Victor Co., Inc.

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File: OPD.kicad_sch

Title: YM2151

Size: A0	Number: 1	Date: 2023-08-05	Rev: v1.3
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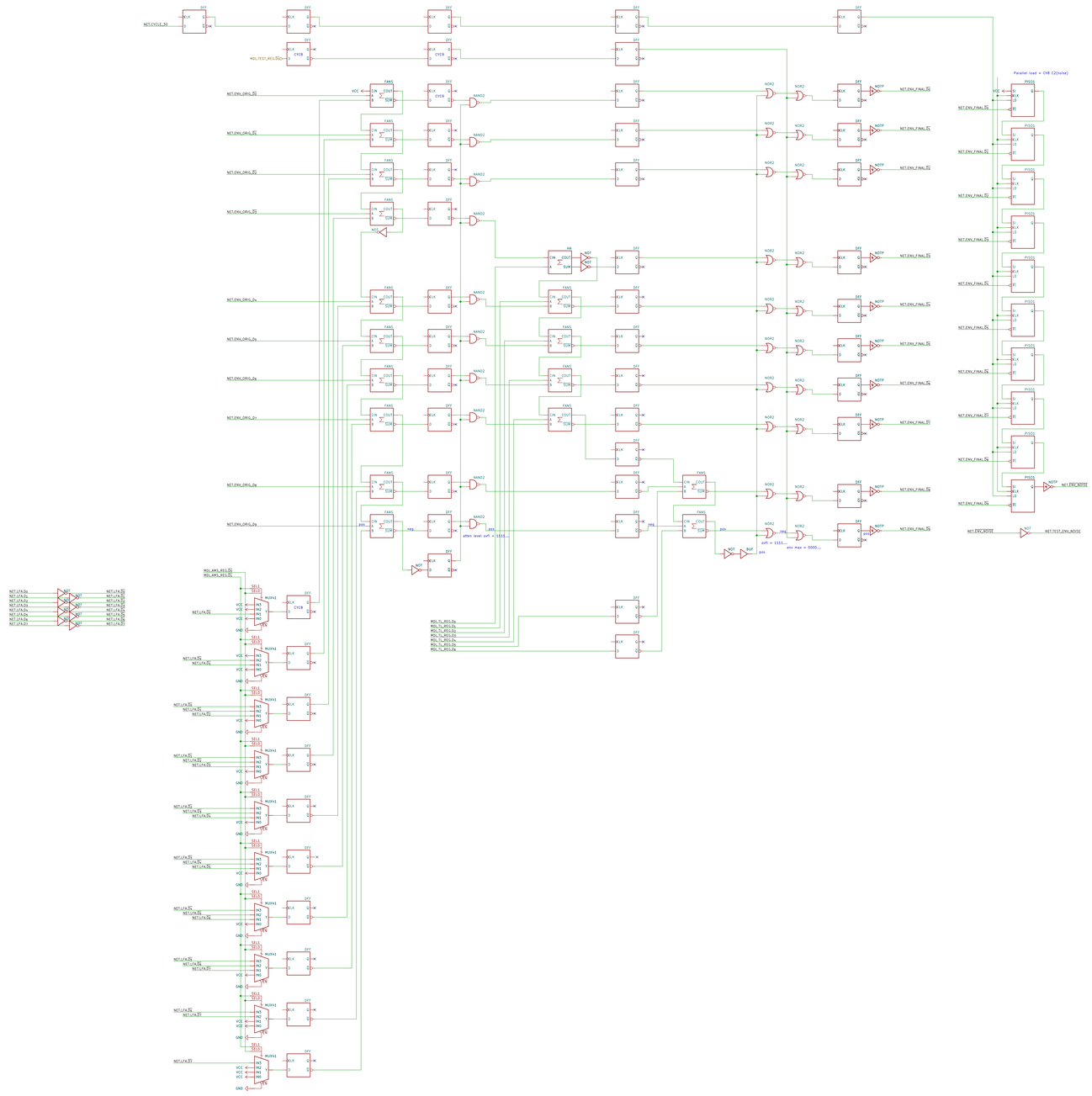

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YM2151 schematics

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Sheet: /EG2/

File: EG2.kicad_sch

Title: YM2151

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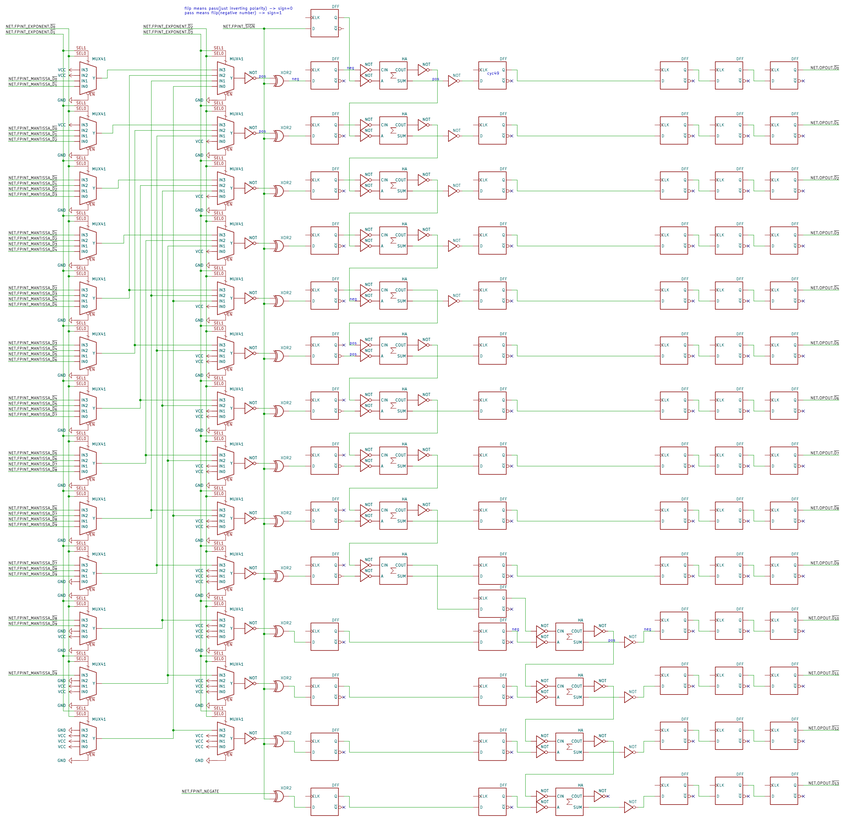

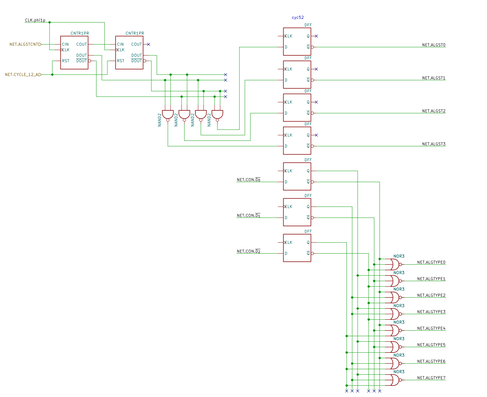

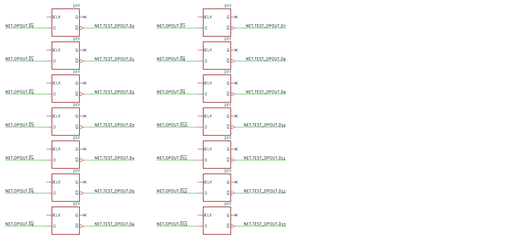

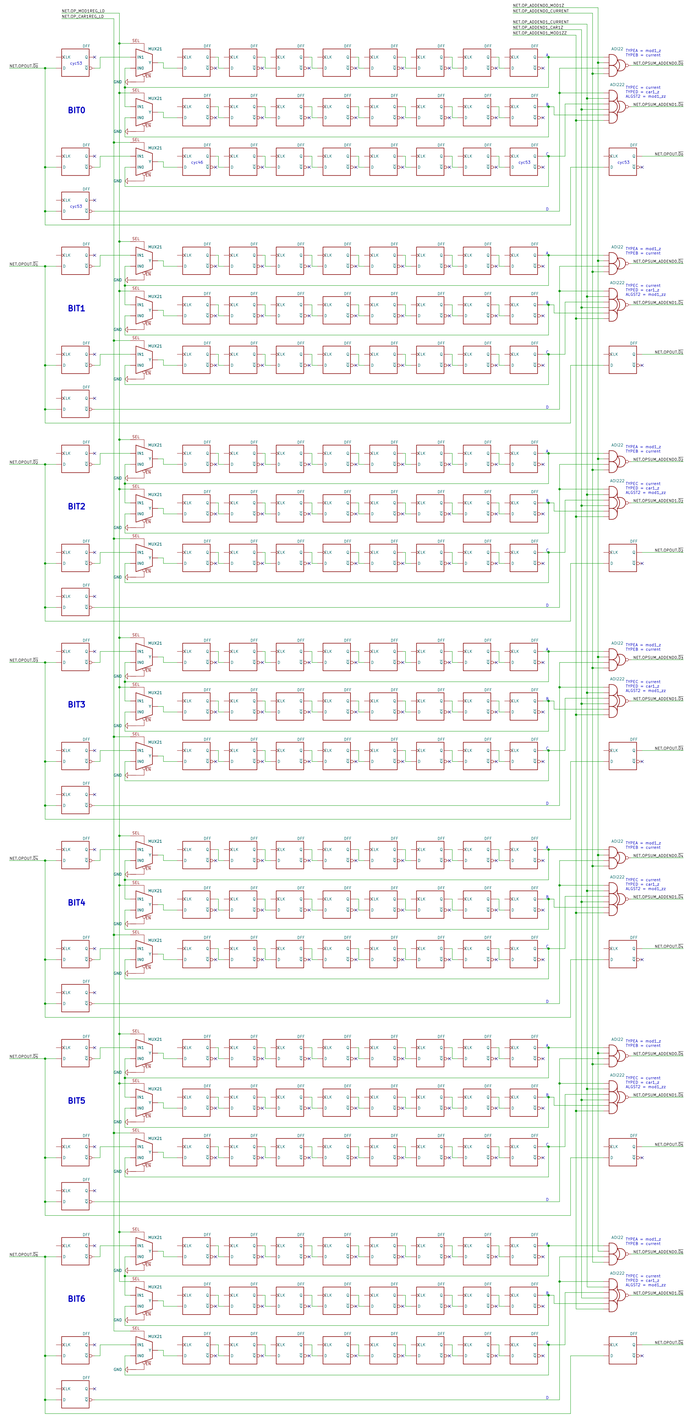

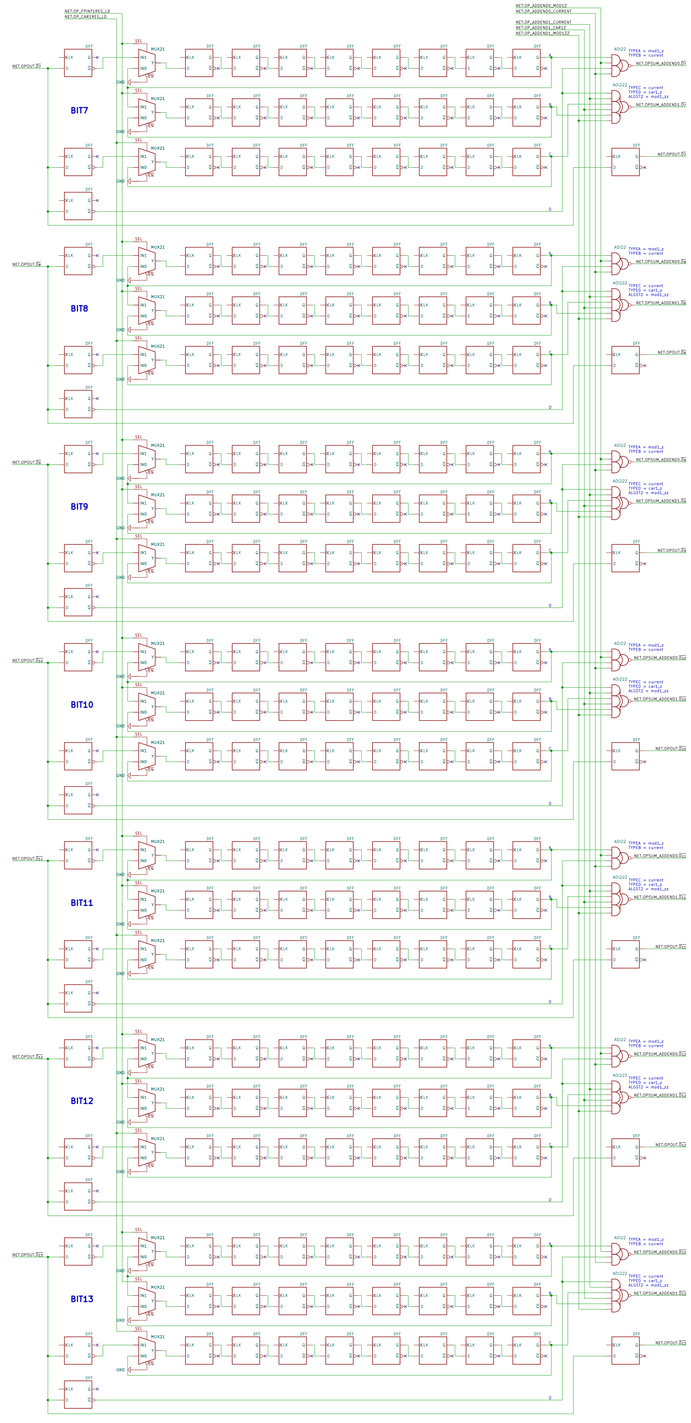

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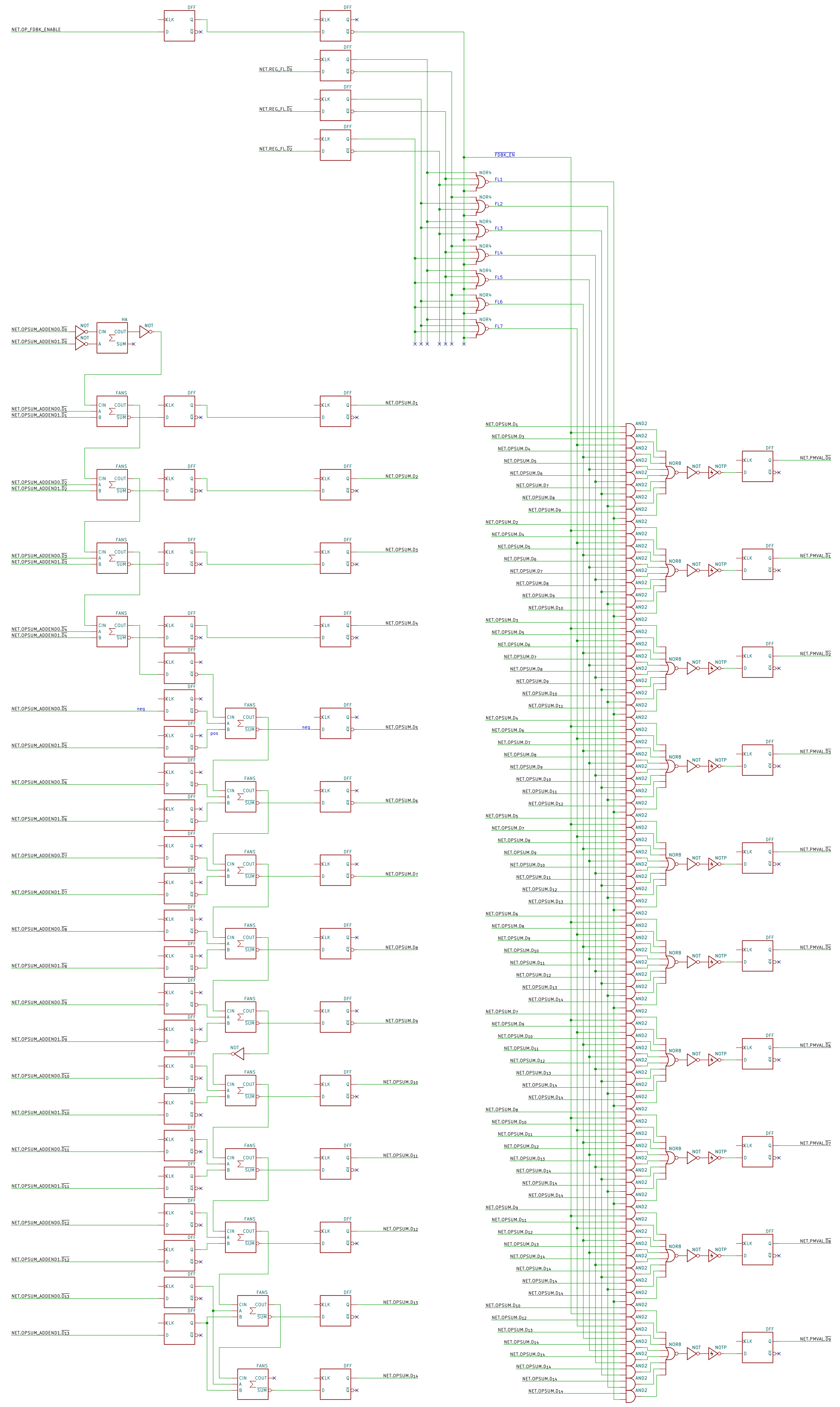

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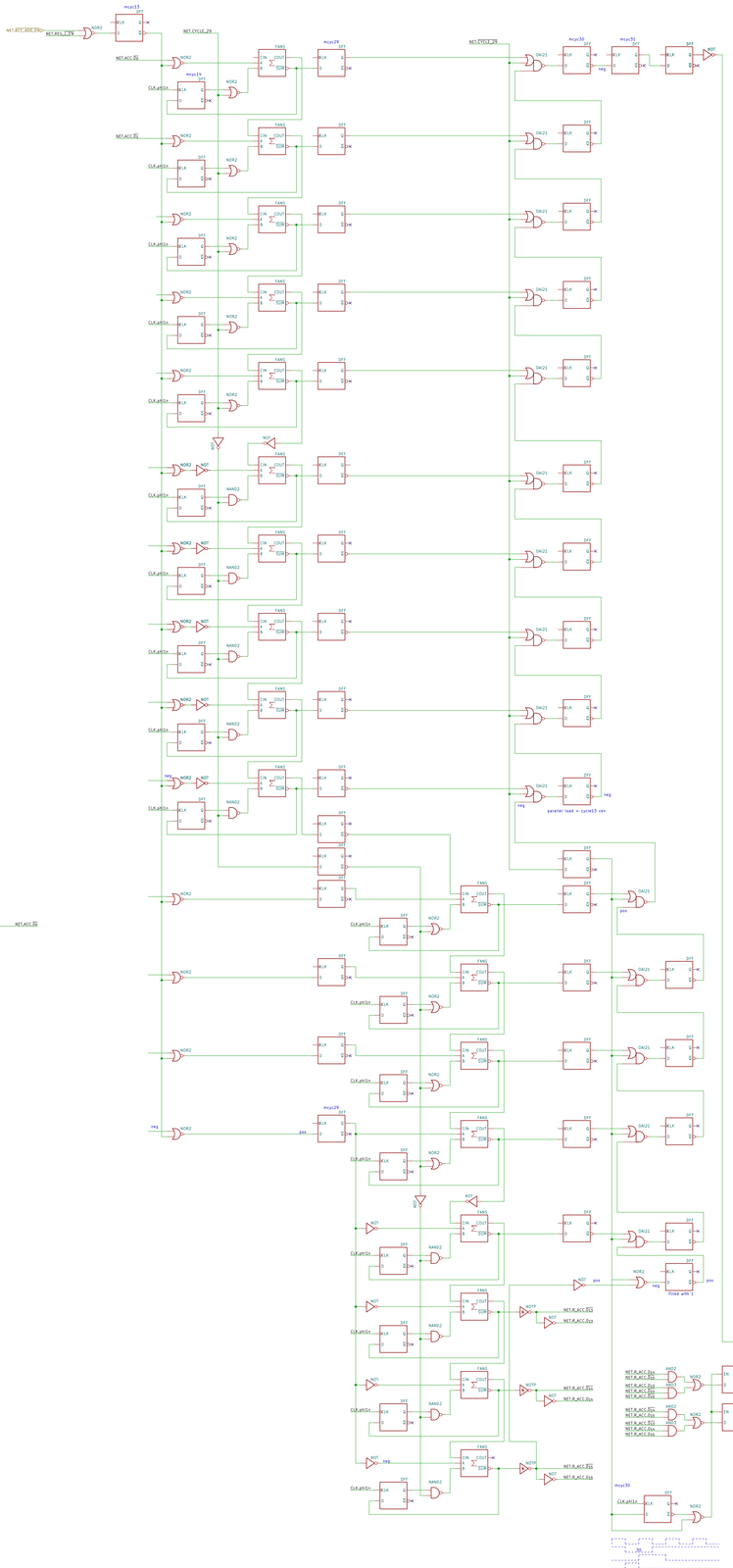

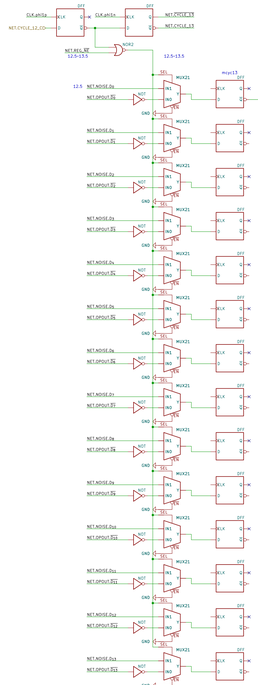

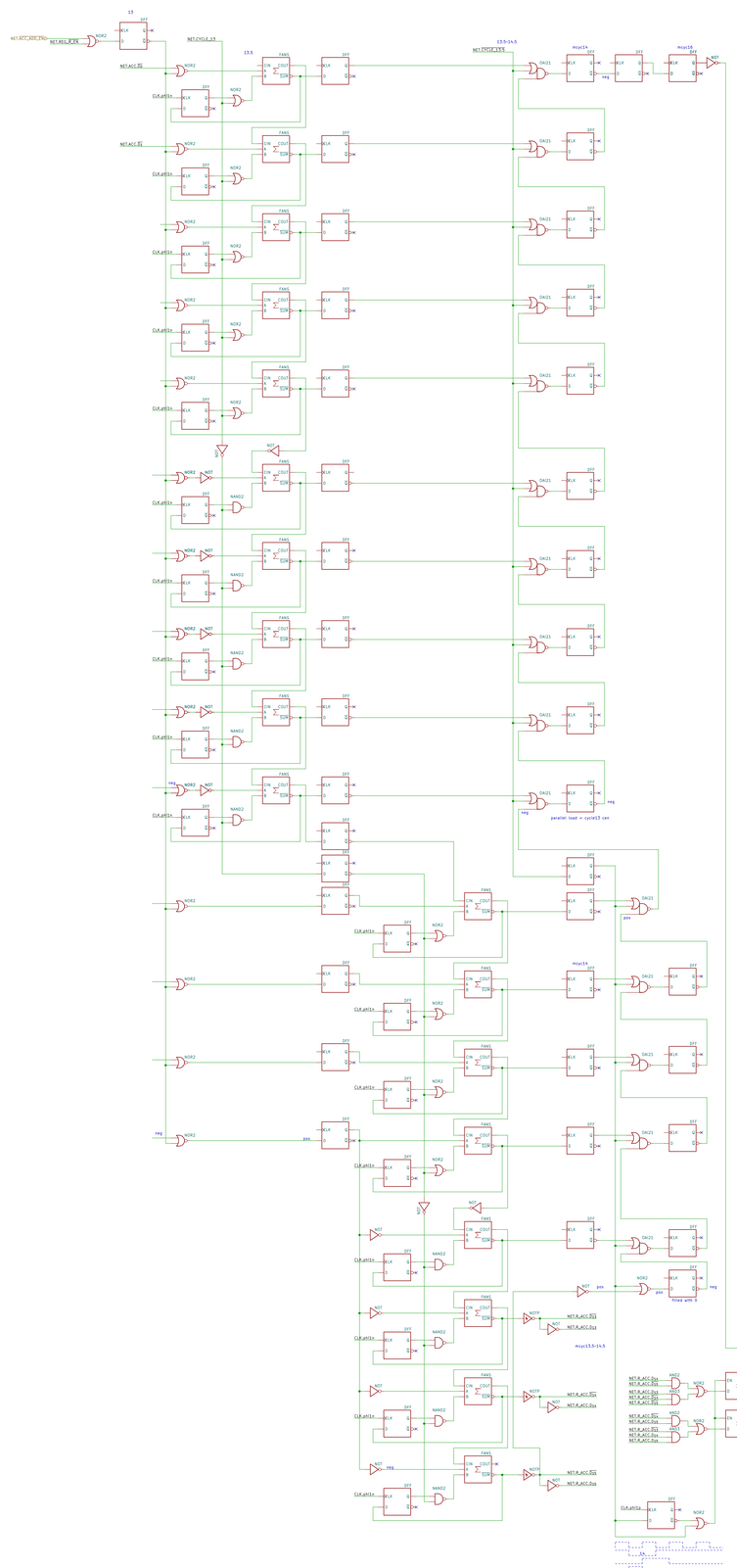

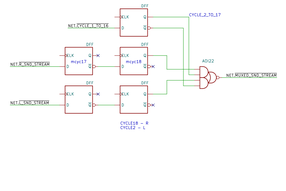

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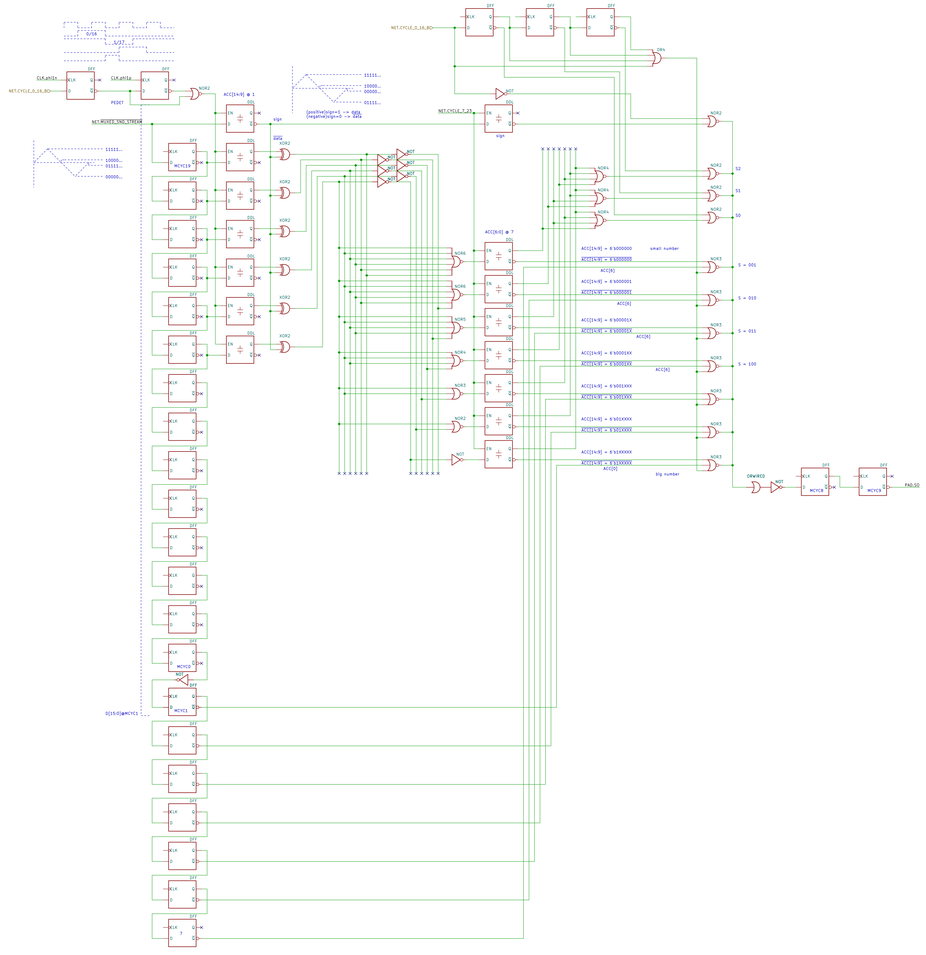

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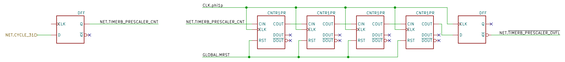

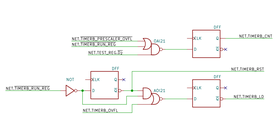

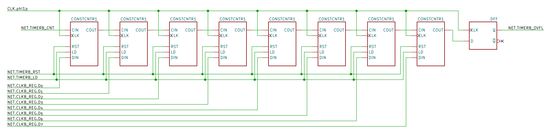

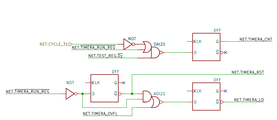

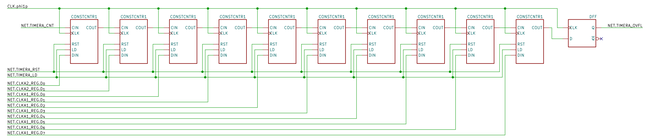

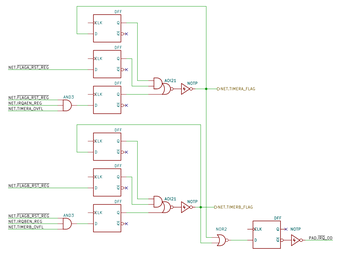

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